COMBINED LOW- AND HIGH-FREQUENCY NONLINEAR CHARACTERIZATION AND MODELING

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Jury

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Abstract

Accurate characterization and modeling of transistors are essential for the successful design of electronic circuits. In many microwave circuit applications, transistors experience high-frequency electrical signals with large excursions. These signals drive the devices into a nonlinear regime of operation. With the introduction of new materials in the transistor fabrication process, additional effects, such as low-frequency dispersion, must be taken into account for a more complete investigation of transistor characteristics.

This work has aimed in the first place at characterizing transistors through nonlinear vector measurements. A time-domain based high-frequency large-signal network analyzer (LSNA) has been extended towards the low-frequency range. When modulated excitations are applied, the low-frequency part operates synchronously with the core RF LSNA. Otherwise it can work like a stand-alone low-frequency LSNA. With this instrument, low-frequency dispersive effects under large-signal operation can be captured more accurately than before.

Next, the calibrated large-signal voltage and current waveforms acquired by the combined low- and high-frequency LSNAs have been exploited to generate nonlinear transistor models. Furthermore a waveform based nonlinear de-embedding procedure has been developed. This technique can be adapted for improving waveform engineering techniques aimed at the design of high-frequency power amplifiers. Both the modeling and the de-embedding procedure are independent of the investigated transistor technology and therefore can be - in principle - adopted for any type of active device.

Samenvatting

Nauwkeurige karakterisering en modellering van transistoren zijn essentieel voor het succesvol ontwerp van elektronische schakelingen. In veel microgolftoepassingen worden transistoren onderworpen aan hoogfrequente, elektrische signalen met een grote zwaai. Deze signalen drijven de componenten in een niet-lineair werkingsregime. Met de introductie van nieuwe materialen in het productieproces van de transistoren moeten bijkomende effecten, zoals laagfrequente dispersie, in rekening gebracht worden, voor een meer volledig onderzoek van de eigenschappen van de transistoren.

Dit werk is in de eerste plaats gericht op de karakterisering van transistoren met behulp van niet-lineaire vectormetingen. Een tijdsdomein-gebaseerde, hoogfrequente, grootsignaal-'network analyzer' (LSNA) is uitgebreid naar het laagfrequente gebied. Wanneer gemoduleerde excitaties worden gebruikt, werkt het laagfrequente gedeelte synchroon met het basisinstrument voor hoogfrequente signalen. Overigens kan het ook gebruikt worden als een autonome, laagfrequente LSNA. Met dit instrument kunnen laagfrequente, dispersieve effecten bij grootsignaalwerking op een meer nauwkeurige manier gemeten worden dan voorheen.

In een volgende stap worden de grootsignaalspanningen en -stromen, die gemeten zijn met de gecombineerde laag- en hoogfrequente LSNA, gebruikt om niet-lineaire transistormodellen te genereren. Bovendien is een op-golfvormen-gebaseerde niet-lineaire 'de-embedding' procedure ontwikkeld. Deze techniek kan aangepast worden voor de verbetering van golfvorm-engineeringtechnieken, bedoeld voor het ontwerp van hoogfrequente vermogenversterkers. Zowel de modellering als de 'de-embedding' procedure zijn onafhankelijk van de onderzochte transistortechnologie en kunnen daarom – in principe – aangepast worden voor elk type actieve component.

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List of symbols

a_i	Incident voltage wave at the i-th port of a N-port network	[V]
A_p	Peak value of AC current	[A]
b_i	Scattered voltage wave at the i-th port of a N-port network	[V]
C_{DS}	Drain-source capacitance	[F]
C_{GD}	Gate-drain intrinsic capacitance	[F]
C_{GS}	Gate-source intrinsic capacitance	[F]
C_{p1}	Gate-pad parasitic capacitance	[F]
C_{p2}	Drain-pad parasitic capacitance	[H]
F	Frequency	[Hz]
f_0	Carrier or fundamental frequency	[Hz]
f_1	Lower frequency component of a two-tone signal	[Hz]
f_2	Upper frequency component of a two-tone signal	[Hz]
f_m	Modulation frequency	[Hz]
f_S	Sampling frequency	[MS/s]
f_t	Cut-off frequency	[GHz]
I	In-quadrature component of a modulated signal	[V]
I_{dSS}	Saturation current	
I_{ij}	Voltage controlled current source	
i_{ij}	Total instantaneous current	[A]
i_{ij}	Current AC component	[A]
I_{ij}	Current spectral component	[A]
L	Gate length	[m]
L_D	Extrinsic drain inductance	[H]
L_G	Extrinsic gate inductance	[H]
L_S	Extrinsic source inductance	[H]
P	Electrical power spectral component	[W]
P	Electrical instantaneous power	[W]
$P_{IN,av}$	Available power at the input port of a two-port network	[W]
P_{OUT}	Output active power	[W]
Q_{ij}	Voltage controlled charge source	
R_D	Extrinsic drain resistance	[Ω]
R_G	Extrinsic gate resistance	[Ω]
R_S	Extrinsic source resistance	[Ω]
S_{ij}	Scattering parameter	

T	Junction temperature	[^oC]
T_C	Base-plate or substrate temperature	[^oC]
T_m	Length of the memory-time	[s]
V_{BD}	Inverse breakdown voltage	[V]
V_{DS0}	Average value of the drain-source voltage under dynamic condition	[V]
V_{DSDC}	DC drain-source voltage	[V]
V_{GS0}	Average value of the gate-source voltage under dynamic condition	[V]
V_{GSDC}	DC gate-source voltage	[V]
v_{ij}	Total instantaneous voltage	[V]
v_{ij}	Voltage AC component	[V]
V_{ij}	Voltage spectral component	[V]
V_K	Knee voltage	[V]
V_p	Peak value of AC voltage	[V]
W	Gate width	[m]
Z_d	Impedance at the drain node	[Ω]
Z_L	Load impedance	[Ω]
τ	Time delay	[s]

List of acronyms

ADC	Analog-to-Digital converter
AlGaN	Aluminum gallium nitride
ANN	Artificial Neural Network
AWG	Arbitrary waveform generator
BW	Bandwidth
CGP	Current Generator Plane
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous wave
DUT	Device Under Test
EP	Extrinsic Plane
ESG	Vector signal generator
EVM	Error Vector Magnitude
FET	Field-Effect-Transistor
GaAs	Gallium arsenide
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IF	Intermediate frequency
IMD	Intermodulation distortion
IMn	n-th order intermodulation product
IP	Intrinsic Plane
I-V	Current-voltage function
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LF	Low frequency
LSNA	Large-Signal Network Analyzer
LUT	Look-up table
MOVF	Multivariate Orthonormal Vector Fitting
NQS	Nonquasi-static
NVNA	Nonlinear Network Vector Analyzer
pHEMT	Pseudomorphic High Electron Mobility Transistor
QS	Quasi-static
Q-V	Charge-voltage function
RBW	Resolution Bandwidth
RF	Radio frequency
Si	Silicon

SiC	Silicon Carbide

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Chapter 1

Introduction and outline of the work

1.1 Maxwell, Fourier, and the invention of the transistor

In 1864 J.C. Maxwell presented a set of differential equations which describe the interaction of electromagnetic waves with the matter [1]. The original formulation consisted of twenty equations which have been then reduced to the famous four *Maxwell's equations*. A bit earlier, but in the same century between 1807 and 1811 J.J. Fourier introduced the *Fourier series* which was primarily applied to solve problems related to heat propagation. It may sound simplistic yet fascinating, but these theoretical breakthroughs constitute the cornerstones of a large part of the modern electronic for communications systems. Actually, in this picture one part is missing. It was in 1947 and researchers of the Bell Laboratories developed the first transistor, which nowadays represents the hearth of electronics.

When information is exchanged in its various forms, either voice, or text message, or images, it is firstly converted into electromagnetic waves which travel very quickly, with a speed of c.a. 300.000.000 m/s, backward and forward from the points the information is transmitted and received. Simply speaking, before reaching the receiver these waves undergo several modifications in order to allow a clear and undistorted transmission.

Conceptually, a transmission/receiver chain can be represented by several cascaded blocks (e.g., electronic circuits) each with a different functionality [2]. These blocks process and modify the physical traveling waves, which can be mathematically represented by signals or functions. The Fourier series constitutes the bridge between the physical electromagnetic waves and their abstract description in mathematical terms. It is not an overstatement to claim that, amongst others, these concepts have indirectly revolutionized the economical and social context of societies. Therefore these concepts are indissoluble from the huge and exponential technological development in the area of communication systems which we witness these days. Clearly, this will continue also thanks to the

development of the hardware, such as transistors, which a communication system is built of.

One of the most essential functionalities in any transmission/receiver chain is definitely amplification. Thanks to amplification the electrical power of the electromagnetic wave –or signal- to be transmitted is boosted up in order to enable the transmitted information to reach long distances. Transistors enable amplification and due to the dramatic evolution of technology these days it is possible to achieve high power density over a small area. Evidently, it is necessary that the amplification process does not alter the information content. Unfortunately, the amplification process is not ideal and distortion is unavoidably present after it.

This work is devoted to the characterization and the modeling of some of the distortion mechanisms introduced by transistors employed in the modern communication systems. Some basic concepts related to the characterization of distortion in high-frequency transistors are shortly outlined in the following parts of this Introduction.

1.2 *Non-linear* distortion in high-frequency electronics

"[…]It would be an overstatement to say that the 1960s' research on nonlinearity was forgotten; it is accurate, however, to note that it was little used. By the late 1980s, the development of digital mobile telephones introduced complex communication systems into consumer electronics […]. Distortion of complex signals again became a serious problem, and nonlinearity became an important research subject […]". This is the extract from the preface of the book 'Intermodulation distortion of microwave and wireless circuits' (J.C. Pedro and N. Borges Carvalho, Artech House 2003) written by Dr. S. Maas, Applied Wave Research (AWR).

Indeed, the number of researchers involved in subjects related to the analysis of nonlinear distortion in high-frequency circuits has significantly grown [3]. The increased interest in this complex topic is surely linked with the exponential growth of the market of wireless devices. The latter have permeated the daily life and there is an increasing demand of new applications and functionalities. Moreover high speed connectivity and long life batteries are surely preferred among consumers. Among microwave designers, this translates into the need to design high-frequency electronic circuits with a minimized level of distortion and highly energy efficient wise. The term distortion is here referred to the nonlinear phenomena which are intrinsic to any electronic circuit. Differently from the distortion introduced by

linear electronic circuits, such as filters, nonlinear distortion is responsible for the generation of energy at frequencies not present in the original information to be transmitted [4]. Commonly this type of distortion is not preferred although in microwave applications the nonlinearity is a key characteristic which enables fundamental functions, such as frequency shifting or signals amplification. Nevertheless, whether nonlinearity is beneficial or detrimental, both nonlinear modeling and nonlinear characterization of high-frequency electronic components are essential.

1.3 Down to transistor level

The transistor is the hearth of today's electronics. The more and more stringent requirements in terms of area consumption, power requirement, and speed of electronic circuits, necessarily drive the continuous development of transistor technology. Depending on the application, either new transistor architectures are explored or new materials are introduced in the fabrication process. For instance, for applications based on silicon Complementary Metal Oxide Semiconductor (CMOS) technology, the 'fin' field-effect-transistor (FinFET) represents, among other solutions, an alternative to continue dimensions scaling down to the nanometer range while not degrading transistor performance [5]. As regarding RF applications, instead, new materials [6] (see Figure 1-1) are investigated to meet the requirements in terms of deliverable power, bandwidth, and linearity. As an example, for the fabrication of transistors enabling high-power operation, the use of wide band gap materials, such as gallium-nitride (GaN), has represented a necessary step in order to overcome the limitations reached with the well-established gallium-arsenide (GaAs) based technology.

In RF electronic systems, transistors are at the core of power amplifiers. These electronic circuits experience high-frequency signals with complex modulation schemes [7] which are often employed to minimize the available bandwidth usage. When such signals pass through a power amplifier, the generated frequency spectrum widens due to the effects of the nonlinearity. Decreasing the power level of the signal exciting power amplifiers would reduce the level of nonlinear distortion but, on the other hand would dramatically reduce the power efficiency. Therefore, commonly power amplifiers operate at very high power levels and design techniques are needed to minimize the distortion. As a consequence, the designers must have accurate power amplifier models in order to control and reduce the nonlinear distortion. This leads to the development of accurate models [8] of the transistors used in the design of power amplifiers. Next to modeling,

characterization is a fundamental step as well especially when new semiconductor materials are explored for transistors fabrication process.

In this work silicon-, GaN-, and GaAs-based transistors are investigated for both characterization and modeling purposes. An overview about these transistor architectures is given in the next Section.

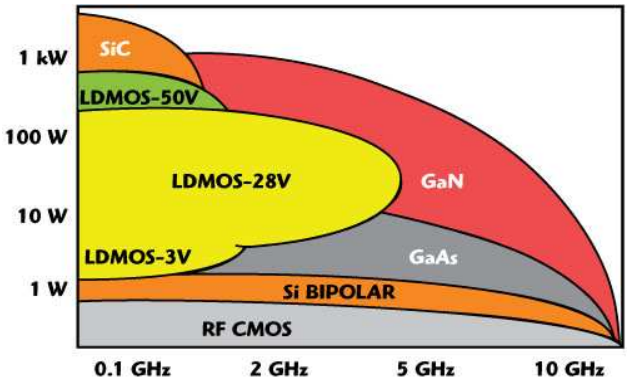

Figure 1-1 Overview of transistor technologies for RF applications (in Microwave Journal vol. 52, no. 6, June 2009– courtesy of NXP semiconductor).

1.4 Transistor architectures: an overview

1.4.1 High Electron Mobility Transistor

In Figure 1-2 the structure of an AlGaN/GaN high-electron mobility (HEMT) transistor [9], [10] is shown.

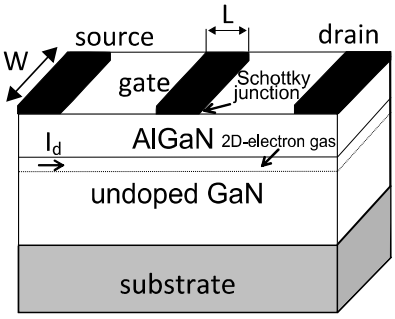

Figure 1-2 Structure of HEMT. For GaN based HEMTs, common substrate materials are sapphire, silicon-carbide (SiC), and silicon. L is the gate length, W the gate width, and I_d the current flowing between the source and drain terminals.

The same structure but slightly modified can be adopted for GaAs based HEMTs [6]. The conductive channel is formed at the interface between the AlGaN alloy and the undoped or GaN layer. Due to the energy-band mismatch and the spontaneous piezoelectric effect, a high-density two dimensional (2D) electron gas gets created near the interface in the undoped GaN layer. Moreover, due to the wide band gap of the AlGaN and GaN materials, the breakdown electrical field is significantly higher than other semiconductor materials. Therefore, wide band gap enables high-voltage operation that, along with high current density makes the GaN based transistor the most suitable candidate for high-frequency high-power applications. Typical values of power density range between 6-9 W/mm [9]. It is noteworthy that the wide band gap ensures also stable high-power operation at higher temperatures and this aspect is fundamental when dealing with high-power densities.

Some of the properties of GaN material are reported in Table 1-I and compared with the GaAs-based HEMT:

	Unit	GaN/GaAs	Pros
Saturation velocity	10^7 cm/s	1.5/1	high-frequency
Breakdown electric field	MV/cm	3.5/0.7	high-power
Band gap	EV	3.4/1.43	high-temperature
Thermal conductivity	W/cm*K	1.7**/0.46	high-temperature, high-power

**This value changes depending on the substrate material

Table 1-I Properties of GaN material and comparison with GaAs [6].

The current flowing in the layer of the 2D-electron gas is controlled by the gate-source and drain-source voltage. The charge accumulated in the channel is modulated by the gate voltage through the Schottky junction, which is formed between the gate metal and the AlGaN layer. When the gate voltage is set equal to 0 V and the source is grounded, current flows in the channel when drain voltage is applied. The channel is completely depleted of free carriers when the gate voltage exceeds the threshold voltage which is negative for this normally-on transistor.

Despite the excellent features of the GaN material, performance of GaN HEMT are degraded by the presence of defects in the interface and substrate materials, mainly due the imperfections in their growth processes. These defects constitute a key issue as they have a direct influence on the high-frequency performance of GaN based RF transistors, as outlined in Subsection 1.4.3.

In this work two GaN-based transistors and two GaAs-based pseudomorphic HEMTs (pHEMT) are investigated, with the dimensions and electrical characteristics reported in Table 1-II.

	Unit	GaN		GaAs	
Gate length(L)	µm	0.7	0.25	0.35	0.25
Gate width (W)	µm	800	200	1440	400
Power density	W/mm	5	5-7	NA	1
Saturation current (I_{dss})	mA/mm	~625	900	300	300
Cut-off frequency (f_t)	GHz	NA	32	NA	55
Breakdown voltage (V_{BD})	V	-80	-70	-22	-15

Table 1-II Dimensions and electrical characteristics of the HEMT investigated in this work.

1.4.2 Multiple-gate Field Effect Transistor (MuGFET)

Along with GaN and GaAs transistors, also a silicon based n-type FET has been considered in this work. The investigated device has been fabricated at imec, in Belgium. The structure of the transistor is illustrated in Figure 1-3.

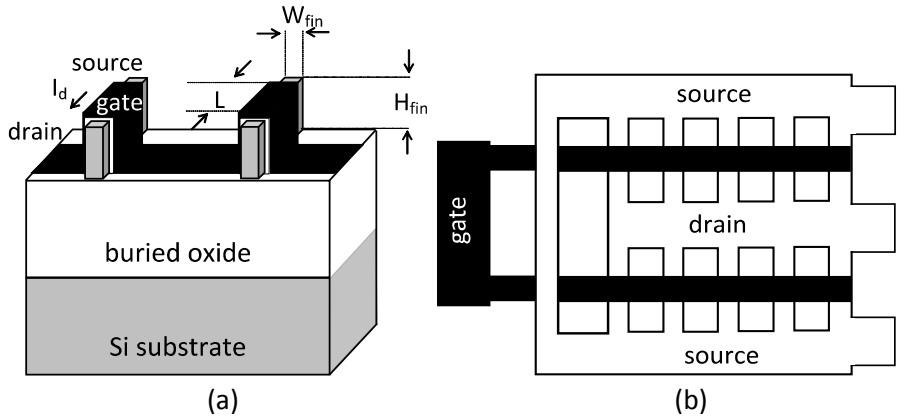

Figure 1-3 (a) Structure of a triple-gate transistor with two fins. I_d is the current flowing from the source to the drain terminal. (b) Top view of a two-finger structure and five fins per finger. This figure is purely for illustrative purposes.

The FinFET is an example of multiple-gate transistor [11]. The gate contact is wrapped around the silicon body and separated from the conductive channel by a thin oxide layer which results in the 'fin' shape. The total gate width of the triple-gate structure in Figure 1-3, where two fins are shown, is $W = 2H_{fin}+W_{fin}$, where

H_{fin} and W_{fin} are the height and the thickness of the silicon body, respectively. The transistor considered in this work has a multi-finger structure with gate length (L) equal to 60 nm and total gate width (W) of 45.6 μm.

Although this transistor is not suitable for power applications, in the context of this work it is exploited as a device-under-test in order to assess the nonlinear characterization system as well as for the analysis of alternative modeling approaches, as reported in detail in Chapter 4.

1.4.3 Low-frequency dispersion in compound-based transistors

Low-frequency dispersive phenomena have become a serious issue, especially for RF transistors built of compound semiconductors. Low-frequency dispersion is often referred to charge trapping mechanisms and thermal effects. Actually, thermal effects impact the physical parameters of any type of transistor. Charge trapping mechanisms, instead, have a strong impact on the behavior of transistors based on compound semiconductors and may strongly affect the RF performance. Traps originate from defects present at both the surface or in the substrate materials [12], [13], as depicted in the simplified cross-section in Figure 1-4.

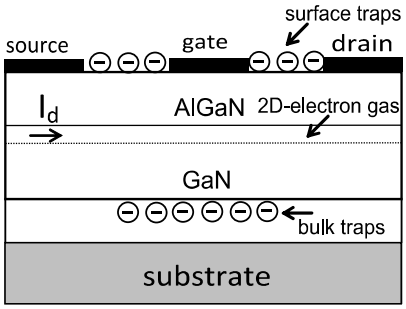

Figure 1-4 Simplified cross section of a AlGaN/GaN HEMT. Traps can be located at both the surface and in the bulk materials.

Evidently, when electrons or holes get captured or released, the defects get electrically charged or discharged and this influences the electric field distribution in the semiconductor, thus affecting the current which flows in the channel. The occupation state, the location, and the dynamics of traps depend, among others, on the voltages applied to transistor terminals. As reported in literature, trapping mechanisms, as well as thermal effects manifest over time scales ranging from ~msec to ~μsec which are much longer than the time-period of signals involved in RF applications. Nevertheless, although under RF continuous-wave (CW)

operation the traps configuration can be assumed to be frozen to the steady state condition, the occupation state strongly depends on the static voltages applied along with the RF signals. Similarly, although the junction temperature can be assumed to be constant under RF CW condition, it depends on the RF power level and it affects physical parameters, such as the mobility of the carriers, and the traps configuration as well. The situation is slightly different when modulated signals are involved. In fact, the envelope of these signals beats at frequencies comparable with the inverse of the characteristic time-constants of dispersive effects. In this case both traps and thermal state cannot be assumed to be frozen but they can vary within the signal swing. As a result, the intermodulation performance of the transistor can change as a function of the modulation frequency and this can have serious implications for applications for which high-linearity is a major concern [14], [15].

Dispersive effects impact the transistor behavior both under small- and large-signal operation. Frequency variation of the small-signal transconductance and the output conductance of a field-effect transistor is a well-known indication of dispersive effects [16]. Under large-signal operation, instead, dispersion manifests as knee walkout and current collapse of the pulsed- or large-signal dynamic characteristics as compared with the ones measured under static condition. It is noteworthy that knee walk-out and current collapse are critical especially for RF applications which demand to maximize output power and efficiency. Clearly, regardless of the application, dispersive effects can play an important role in RF electronic nonlinear circuits which are based on compound semiconductors. Therefore, a complete characterization system for transistors should be capable of measuring under nonlinear operating condition from near DC up to millimeter-wave frequencies. Unfortunately, such a measurement system is not available yet though huge efforts have been made in the last decades in order to develop characterization systems as completely as possible for microwave and millimeter-wave transistors.

In the next Section measurement techniques for the large-signal characterization of transistors characterization are outlined.

1.5 Nonlinear characterization of high-frequency transistors

1.5.1 Pulsed measurements

Pulsed measurement systems are widely employed to determine the dynamic characteristics of transistors for a fixed thermal state and, when present, for a 'frozen' configuration of the interface and substrate defects electrical state [17]. Basically, the transistor is firstly driven into a steady-state condition, generally determined by a quiescent point. Next, the device is excited by time-domain pulses which are short and fast enough not to affect the reached steady-state. Clearly, when the time duration of the pulses is long enough, as compared for instance to the time needed to change the thermal state, the current in the channel measured within the pulse duration indicates the evolution of the transistor characteristics as function of time.

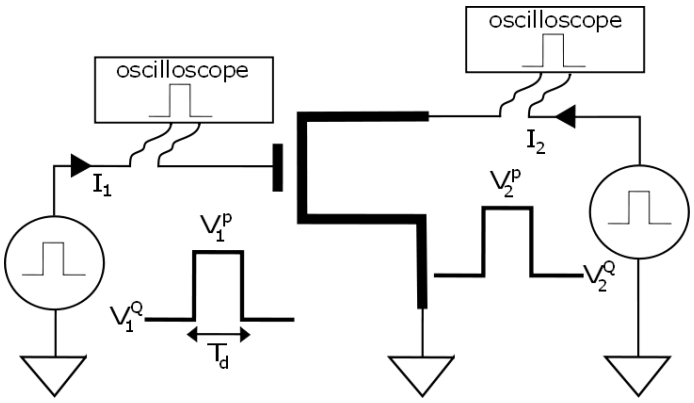

Figure 1-5 Simplified schematic for pulsed characterization of transistors. Firstly, the transistor is driven to a steady state condition by the quiescent voltages V^Q. Pulses (V^P) are then applied and the currents are acquired within the duration T_d of the pulses.

1.5.2 High-frequency large-signal network analysis

The high-frequency Large-signal Network Analyzer (LSNA) enables vector calibrated measurement in both time- and frequency-domain [18]. Basically an LSNA acquires the full spectral content of incident and scattered waves at the transistor ports, as in the simplified schematic in Figure 1-6. As the LSNA

measures also the relative phase between the frequency components of the acquired spectra, the calibrated time-domain waveforms of the electrical quantities at the transistor ports are also available. The up-to-date LSNA (or 'NVNA') operates up to 67 GHz. The LSNA enables characterization also under modulated excitations and therefore transistor can be tested under realistic conditions, though with the existing configurations only periodic excitations are allowed.

Generally there has been a growing interest in calibrated time/frequency - domain measurement systems due to the possibility to infer the transistors nonlinear behavior by direct inspection of the calibrated current and voltage time domain waveforms. For example, 'waveform engineering' [19] techniques have recently become very popular among microwave researchers and applied for both transistors characterization and power amplifier design.

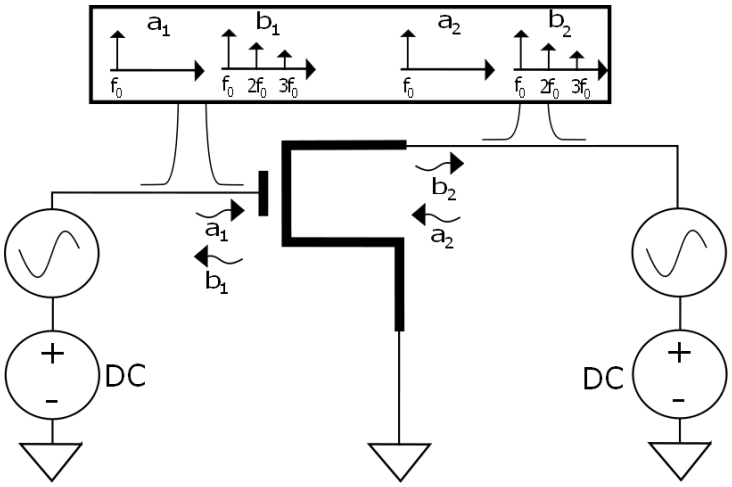

Figure 1-6 Simplified schematic for the nonlinear characterization of transistors. The incident 'a' and scattered 'b' voltage waves at the transistor ports are detected both in time- and frequency- domain.

1.5.3 Low-frequency large-signal network analysis

Differently from the high-frequency LSNA, the LF LSNA typically operates in the mega-Hertz range [20]. This system has been originally developed in order to perform a direct characterization of low-frequency dispersive phenomena. This low-frequency system enables a simplified calibration routine as compared with the high-frequency systems. On the other hand, it operates at frequencies which are significantly far from the actual high-frequency applications. The usefulness of this type of systems for the characterization of high-frequency transistors will be

extensively stressed in the next Chapter. In general, these systems can be adopted for the characterization of the nonlinear distortion of electronic circuits operating in the low-frequency range.

1.6 Thesis objectives and outline

It is clear from the previous discussion that the characterization of transistors under large-signal regime is essential. In this perspective both pulsed measurements and vector calibrated large-signal measurements represent alternative solutions to investigate transistor nonlinear dynamics. Nevertheless both approaches present some limitations. In case of pulsed measurements, it is hard to obtain time-duration of pulses comparable with the ones associated to the frequencies employed in RF applications. This limitation is overcome with high-frequency vector calibrated measurement systems which operate in the RF frequency range, both under continuous-wave and modulated excitations. However, these systems do not allow an immediate and straightforward characterization of low-frequency dispersive phenomena. To this aim, low-frequency vector calibrated systems constitutes a possible alternative but they operate at frequencies much lower than the RF ones. It is noteworthy that both the low- and high-frequency capabilities are necessary for a comprehensive characterization of transistors. For this reason, a solution to combine low-and high-frequency measurement systems is proposed in this work. The core of the proposed measurement system is a time-domain based LSNA operating in the range from 600 MHz to 50 GHz. This has represented the starting point of the activity, whose objectives can be summarized as follows:

- extension of the existing LSNA bandwidth down to low-frequencies, i.e. kHz-MHz range;

- exploiting the experimental data generated by the extended LSNA in order to:
  - accurately and completely validate nonlinear models;
  - characterize the dynamic behavior of modern transistor technologies;

- combining the low- and high-frequency vector measurements for the generation of large-signal transistor models;

- developing techniques for de-embedding high-frequency vector measurements to retrieve the actual current and voltage time-domain waveforms at transistor terminals.

In *Chapter 2* the novel nonlinear characterization system is described and the calibration aspects are outlined in a detailed way. Particularly a procedure to align the low- and high-frequency calibrations is described which is essential for the correct reconstruction of the current and voltage time-domain waveforms under modulated excitations. The core of the measurement set-up is a RF large-signal network analyzer (LSNA) which is extended further down to 10 kHz. In this way nonlinear characterization can be synchronously performed in both the low- and high-frequency ranges Practical experimental examples are reported in order to demonstrate the versatility of this novel set-up.

Chapter 3 focuses on the experimental part of the work. Although the set-up described in Chapter 2 is primarily meant to measure the complete nonlinear behavior of high-frequency electronic circuits under modulated excitations, it can be straightforwardly adapted for time-domain load-pull characterization. Load-pull techniques in time-domain provides one with a powerful 'characterization tool' to highlight the transistors nonlinear behavior. Field-effect-transistors (FETs) are investigated with particular emphasis on the dynamic response of the output current generator. The latter is a very complex 'object' as its behavior is also affected by dispersive phenomena. In this Chapter the low-frequency based load-pull system is exploited to highlight the dispersive behavior of different transistor technologies.

Chapter 4 deals with linear and nonlinear modeling of field effect transistors. Measurements-based modeling techniques are adopted. It is demonstrated that low- and high-frequency nonlinear measurements can be successfully combined to extract full nonlinear transistor models. The nonlinear model parameters are determined by numerical optimization combined with semi-empirical formulations.

As regarding the linear part, a behavioral modeling technique, originally developed for passive electromagnetic structures, is adapted for the modeling of the linear microwave behavior of a silicon FET.

In *Chapter 5* a technology independent technique aimed at the de-embedding of large-signal high-frequency measurements is described. This technique allows one to retrieve the actual current and voltage waveforms at the output current generator

terminals starting from any high-frequency large-signal measurement. The main advantage of this approach relies on the fact that the modeling of the output current generator is not needed. Such a modeling constitutes a challenging task when dispersive effects are not negligible. In the Chapter, two different approaches are reported and applied for the de-embedding of large-signal measurements performed on a silicon FET and gallium-nitride high electron mobility transistor.

The last part is devoted to *Conclusions* and outlook.

It is interesting to mention that all the approaches outlined in this work are quite general and are in principle independent on transistor technology.

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Chapter 2

Characterization system

2.1 Overview

This chapter is devoted to the description of the characterization system employed in this work. As mentioned in Chapter 1 an accurate and complete characterization of modern microwave transistors requires a nonlinear characterization system operating over different frequency ranges. According to our knowledge, such equipment was not available when this PhD research got started. The characterization system exploited for this work partially fills the gap as it combines low- and high-frequency vector nonlinear capabilities.

2.2 LF LSNA (dynamic-bias)

2.2.1 Extending the RF LSNA to low-frequency: why?

The core of the measurement system consists of an RF LSNA. The latter enables calibrated vector measurements of four RF signals, in case of a two-port measurement instrument, in the 600 MHz-50 GHz range and with up to 20 MHz bandwidth (BW). Traveling waves are detected at the fundamental frequency and the harmonics, including the intermodulation products induced around each harmonic when modulation is applied. The RF LSNA employed in this work has a time-sample based architecture [1] which, differently from the recently developed mixer based architecture [2], [3] operates in time domain by exploiting the harmonic sampler principle and handles only periodic CW or modulated signals [1]. A simplified block diagram of the RF LSNA is illustrated in Figure 2-1. It encompasses broadband directional couplers with 50 MHz-50 GHz BW to sense the traveling waves at RF PORT1 and RF PORT2; a down-converter which shifts the high-frequency waves into the intermediate frequency (IF) BW; a receiver front-end to sample and digitize the down-converted waves. All the parts of the system are synchronized with a 10 MHz reference clock signal. RF excitations are applied at the coupler input IN either directly or through RF bias-tees when the DC supply path is not separated by the RF one.

The outstanding capabilities of such instrument have been already demonstrated in many works [5]-[7]. Nevertheless, the device used as phase reference for the calibration of the instrument (see Subsection 2.3.1) limits the lowest measurable frequency component to 600 MHz and this constitutes a restriction especially for the characterization of nonlinear electronic circuits excited by modulated signals. The latter have strongly entered the characterization and modeling phase in the last years, thus forcing the development of measurement systems as complete as possible to provide deeper insight in the investigation of nonlinearity. For instance, the second order intermodulation product generated by a nonlinear system when it is excited by a two-tone signal [8] would fall outside the RF LSNA BW resulting in incomplete measured waveforms. This was the main reason which drove the extension of the existing RF LSNA down to the LF range. In addition, the LF extension adds a valuable feature when characterizing transistors which are prone to dispersion and memory-effects which mainly manifest at very low-frequency scale as compared with the frequencies of RF applications. In fact, the LF measurement set-up can be uniquely exploited to highlight these slow dynamics.

In order to overcome the RF LSNA frequency limitation, different solutions have been developed, which are mainly dedicated to specific applications and measurement systems [9]-[13]. Recently a general low-frequency extension has been released for an RF LSNA [14], [15]. The first prototype has been proposed by the NMDG company in 2008 and now it is commercially available as a stand-alone LF LSNA (Figure 2-2). The system is also called *dynamic-bias* since the intermodulation product at f_2-f_1 appears as an LF modulation of the static bias point as compared to the RF carrier frequency of the signals. Following the prototyping phase of the core set-up and the development of the calibration procedures in collaboration with the NMDG company, further development of the measurement system has been carried out within the PhD activity. Particularly, both software and hardware extensions have been applied to the original system configuration in order to perform combined low- and high-frequency time-domain load-pull.

In the following, the architecture of the LF LSNA is described in more detail.

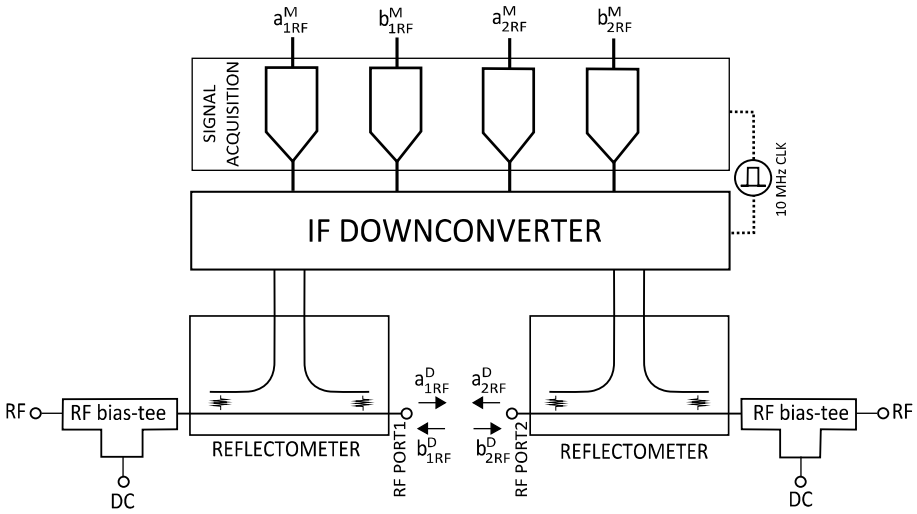

Figure 2-1 Block diagram of a sampler-based RF LSNA.

2.2.2 System architecture

A block diagram of the dynamic-bias is illustrated in Figure 2-2. Similarly to the RF LSNA architecture it encompasses coupler-like signal separation boards (LF sensing modules in Figure 2-2) to sense and separate voltages and currents at the LF PORT1-2 and an acquisition section for signal sampling and digitization.

The separation and sensing of the LF signals can be done either with couplers [9]-[11] or DC-blocked sensing resistor techniques [12], [13]. LF couplers usually present low insertion losses but their technology limits the lowest frequency range to hundreds of kilo-Hertz. Inversely, the DC-blocked sensing resistor techniques allow one to measure low-frequency contents as low as a few kilo-Hertz, but the selection of the sensing resistor value will impact both the insertion loss and the measurement accuracy. In this work the second solution is adopted in order to extend the lowest measurable frequency down to the kilo-Hertz range. Moreover, to obtain higher measurement accuracy, the measured LF spectral content must be separated from the DC voltage and current at the inputs of the LF data acquisition system, to increase the dynamic range that is otherwise hampered by presence of a large superimposed DC level.

The sampling and digitization can be performed by a dedicated oscilloscope [9] or analog-to-digital (A/D) converters [14]. Alternatively, the LF quantities can be re-directed to the RF large-signal analyzer front-end, by an analog recombination of the LF and RF waveforms [9], [10] or by time-sharing the receiver inputs [11],

[12]. The measurement system of this work is equipped with 12-bits A-to-D converters whose sampling frequency (f_s) is 60 MS/s with the minimum value of the resolution bandwidth (RBW) equal to 28.61 Hertz.

The system is also provided with dedicated LF bias-tees which are necessary to enable the separation between the DC and the LF terminations thus allowing, for example, passive and active control of the LF input and output impedances since any DC voltage (current) source would present a short (open) circuit to the LF components, at least at very low frequencies. Actually the selection of the LF bias-tee constitutes a critical point since it impacts the BW of the measurement system. Issues related to LF bias-tee design will be detailed in Section 2.5.

Not shown in Figure 2-2, a test-set has been developed. This test-set is mainly composed of switches and it can be used either in the measurement and or in the calibration mode. In the latter configuration, the calibration of the LF hardware set-up is simplified by routing automatically the signal used for the calibration (omitted in Figure 2-2) at the LF sensing modules' input IN. In this mode, the LF bias-tees are automatically disconnected in order to apply automatically the LF calibration signal or the internal 50 Ohm termination to the sensing modules' input ports without requirement of user manipulation. In measurement mode, the test-set connects the LF bias-tees to the sensing modules' input ports and gives access to an external port which can be passively terminated or connected to a LF signal source in order to perform active signal injection. More practical details about the test-set connections are provided in the Appendix A.

In the current version, the LF LSNA enables vector corrected measurements of devices embedded in text-fixtures or fabricated on-wafer. The bandwidth of the system ranges from 10 kHz to 24 MHz and it detects LF spectral components up to +/-30V_p and +/-2A_p and can sense LF voltages and current down to 20 μV and 3 μA. DC voltages and current limits are +/-60V and +/-2A, respectively.

The lower and upper frequency limits are set by the cut-off frequency of the LF bias-tees and the sampling frequency of the A/D converters, respectively. Extension of the frequency range is clearly possible just employing faster converters and customized bias-tees which can be straightforwardly embedded in the set-up.

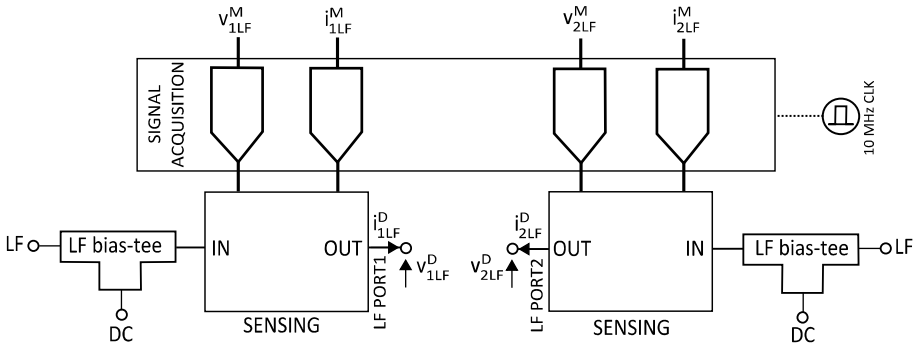

Figure 2-2 Block diagram of the LF LSNA architecture.

2.2.3 LF LSNA configurations

2.2.3.1 Low-frequency large-signal network analyzer

With the configuration illustrated in Figure 2-2 the LF LSNA offers the possibility to perform nonlinear characterization at low-frequency scale. As an application, such configuration can be adopted for time-domain active load-pull measurements which are widely exploited especially for on-wafer nonlinear characterization (Chapter 3). Note that if the level of the exciting signals is properly controlled, the system of Figure 2-2 becomes a linear network analyzer [17]**.**

2.2.3.2 Combined low- and high-frequency nonlinear characterization

As said in Subsection 2.2.1, the LF LSNA is originally conceived to extend the BW of the RF LSNA. Therefore, the set-ups separately shown in Figures 2-1 and 2-2 are combined to synchronously perform LF and RF nonlinear characterization.

Depending on the application and the device under test (DUT), the LF and RF signal paths can either be common or physically separated. The latter situation is quite standard for RF integrated circuits embedded in coaxial test-fixtures which typically include their own RF matching networks and DC bias circuits (see Subsection 2.4.1). In this case, though the set-ups in Figures 2-1 and 2-2 operate synchronously, no hardware modifications are required. On the other hand, when the DUT is directly fabricated on-wafer or does not embed its own matching and bias circuits, it is necessary to combine the DC, LF, and RF signals at the same reference plane while to separate and route them to the RF and LF signal acquisition sections. For this purpose, classical RF bias-tees are not suitable since

they typically include dumping capacitors on the DC path for noise decoupling. These capacitors would act as filters also for the LF currents and voltages induced by the DUT. Consequently, one needs to use either customized bias-tees with a broadband DC path [8]-[12] or diplexers with a sufficiently wide LF bandwidth [16] including also a DC path, and with an RF bandwidth that covers the application bandwidth. In the measurement system of this work a commercial broadband diplexer has been adopted and is placed as illustrated in Figure 2-3. The LF and RF bandwidths of the diplexer cover respectively from DC to 25 MHz and from 90 MHz up to 45 GHz. An example of DUT with the DC, LF, and RF signals applied at the same reference plane is discussed in Subsection 2.4.2.

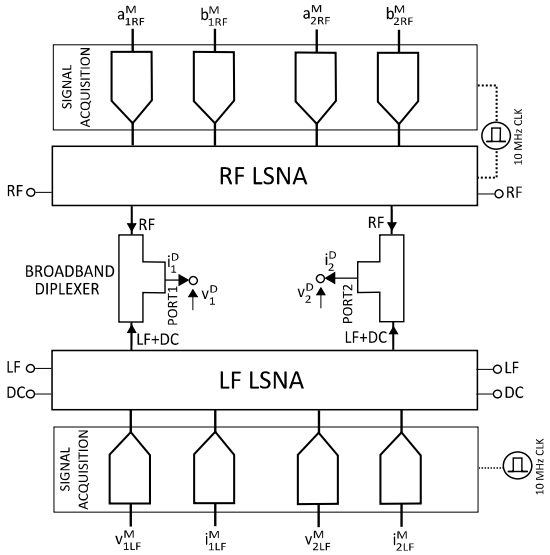

Figure 2-3 LF-RF LSNA for characterization of a DUT with the RF, LF, and DC spectral components at the same reference plane.

2.3 Calibration

This section focuses on the description of the calibration procedures of the measurement systems.

Calibration is an unavoidable step to properly retrieve the traveling waves (or voltages and currents) at the DUT ports from the raw measured quantities detected by the signal acquisition front-end. With reference to any of the set-ups previously sketched, the voltages and currents or the traveling waves with subscript index ‘D’ indicate the quantities at the DUT ports (RF PORT1-2 and LF PORT1-2) whereas

the subscript index 'M' is used for the measured quantities. Subscript indexes '1' and '2' indicate the port number.

A linear error model can be assumed for both the LF and RF measurement paths. In case of the LF part, the test-set includes only passive electronic components, such as switches, whose electrical characteristic can be reasonably considered independent from the amplitude of the signals applied to them. For the RF part, step-attenuators (omitted in Figure 2.1) are placed in front of the IF down-converter. These attenuators are adjusted, depending on the power levels, in order to keep the amplitude of the signals applied at the input of the down-converter sufficiently small to satisfy the assumption of linearity. Therefore, under the hypothesis of linearity of the measurement paths, the measured quantities at the receiver output and the errorless quantities at the DUT ports are related by as in eq. (2.1):

$$\begin{bmatrix} a^i_{1D} \\ b^i_{1D} \\ a^i_{2D} \\ b^i_{2D} \end{bmatrix} = \left|K^i\right| e^{j\varphi^i} \begin{bmatrix} 1 & \beta^i_1 & 0 & 0 \\ \gamma^i_1 & \delta^i_1 & 0 & 0 \\ 0 & 0 & \alpha^i_2 & \beta^i_2 \\ 0 & 0 & \gamma^i_2 & \delta^i_2 \end{bmatrix} \begin{bmatrix} a^i_{1M} \\ b^i_{1M} \\ a^i_{2M} \\ b^i_{2M} \end{bmatrix} \tag{2.1}$$

where '*i*' is the integer harmonic index of the frequency grid selected for the calibration. Note that a similar relationship could be written by replacing the traveling waves with the voltages and the currents, though traveling waves are more suitable quantities when dealing with high-frequency. In eq. (2.1) it is assumed that the electrical coupling between the input and output ports is negligible over the whole frequency range of operation. For this reason eight terms of the matrix in eq. (2.1) are set equal to zero.

In this work, both the LF and RF hardware are separately calibrated by employing standard calibration techniques (Subsections 2.3.1 and 2.3.2). After the computation of the coefficients of the error model (eq 2.1), the RF and the LF LSNA can be exploited as stand-alone systems for independent LF and RF nonlinear characterization. An additional step is instead needed when the RF and the LF LSNA operate jointly, as in case of nonlinear measurements on devices excited by RF modulated signals. In fact, due to the lack of synchronization between the LF and RF calibrations, a delay difference between the RF and LF coefficients is present. As a result of this delay difference, the RF and LF waveforms generated by a nonlinear device under RF modulation, would undergo an unwanted relative phase shift which has to be corrected. A procedure to account for this delay difference is described in Subsection 2.3.3.2.

2.3.1 RF LSNA calibration

With the calibration routine, the unknown coefficients of the error model in eq. (2.1) are computed. For the RF LSNA the calibration is performed as follows:

1) the coefficients inside the matrix in (2.1) are determined with a relative calibration at the fundamental frequency and the harmonics. The number of the coefficients is reduced to seven when the cross-talk between the input and output ports is negligible and thus only β_1, γ_1, δ_1, α_2, β_2, γ_2, and δ_2 have to be calculated. In this work, the S-O-L-T (Short-Open-Load-Thru) and L-R-R-M (Line-Reflect-Reflect-Match) methods [18] are chosen for the coaxial and on-wafer calibration, respectively.

2) next, the values of 'K' and 'φ' are calculated with an absolute calibration [19] which accounts for the amplitude and phase distortion on the measurement path at each point of the calibration frequency grid. For this step a power sensor and a harmonic phase reference (HPR) are needed. The hardware of the HPR limits the lowest frequency at which calibration can be executed to 600 MHz. When RF PORT1-2 are coaxial, the absolute calibration is performed by directly connecting the power sensor and the HPR at RF PORT1. Clearly this is not possible for on-wafer calibration, for which RF PORT1-2 are at the probe tips. To overcome this problem, the calibration plane is shifted, with an additional SOL calibration, from the probe tips to an auxiliary port where the power sensor and the HPR can be connected [20].

After 1) and 2), the coefficients in eq. (2.1) are calculated at each frequency of the calibration grid. When RF modulation is applied, these coefficients are assumed to be constant over the modulation BW. This assumption is valid as long as the modulation BW is narrow as compared to the carrier frequency. Otherwise, another calibration is applied which compensates for the distortion introduced by the measurement system over the modulation BW [21]. A more detailed mathematical explanation of the RF LSNA calibration can be found in [1].

2.3.2 LF LSNA calibration

Conceptually, the same steps as for the calibration of the RF LSNA can be applied for the calibration of the LF hardware. However, whereas the RF LSNA

calibration can be performed sequentially at each point over the selected frequency grid, for the LF calibration the same approach would take a very long time. As an example, if the LF fundamental frequency is 10 kHz, one ends up with 2400 frequency points to measure in order to cover the full LF BW up to 24 MHz. Note that for the RF LSNA, even when the fundamental frequency is set to the lowest measurable value of 600 MHz, less than 100 frequency points are needed to cover the full RF BW up to 50 GHz.

To avoid a time-consuming procedure and prevent the recalibration each time the LF frequency grid is changed, the LF system is calibrated at once over its full BW and with an enough dense equally-spaced frequency grid to accurately allow interpolation. To this aim a multi-tone signal is generated by means of an arbitrary waveform generator (AWG) and used as the excitation throughout the calibration process.

The multi-tone signal is created according to a Schroeder multi-tone algorithm to obtain a low crest factor signal,

$$X(f) = \sum_{k=1}^{N} e^{j\pi \frac{k(k\ 1)}{N}} \delta(f - kf_0) \tag{2.2}$$

with f_0 = 9.956 kHz and N = 2400.

This signal, which is used during the relative calibration, serves also as the power and phase reference for the absolute part. For this reason, it has to be pre-characterized. This is accomplished by generating the Schroeder multi-tone by software and uploading it into a digital-to-analog converter (DAC) which is available as part of the receiver front-end (Subsection A1.1). Next, the DAC output is acquired with one of the channels of the receiver front-end and the measured spectrum is stored in a file as reference (which is here called PPR which stands for Power and Phase Reference). The magnitude spectrum and the time-domain waveform of the PPR are shown in Figure 2-4.

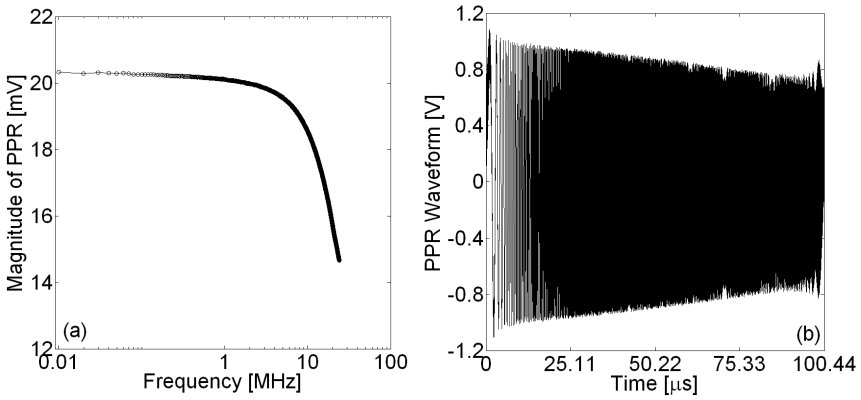

Figure 2-4 (a) amplitude spectrum and (b) time-domain waveform of a Schroeder multi-sine of 2400 tones. The first frequency point is at 9.956 kHz.

For the LF relative calibration, the signal generated by the DAC is switched through the test-set to LF PORT1 and LF PORT2 which are the reference planes where the known calibration standards are connected. For this work the S-O-L-T method is chosen. For the absolute part, the PPR is connected directly to LF PORT1 for coaxial calibration. For on-wafer calibration an LF auxiliary port is exploited and an additional LF S-O-L is performed to shift the calibration plane from the probe to the auxiliary port. After these steps, the coefficients β_1, γ_1, δ_1, α_2, β_2, γ_2, δ_2, K, and φ are known also for the LF hardware.

2.3.3 LF-RF LSNA calibration

2.3.3.1 Procedure

When the systems in Figures 2-1 and 2-2 are combined together, the calibration is performed in three steps:

1. calibration of the RF LSNA;

2. calibration of the LF LSNA;

3. alignment of the RF and LF calibrations' coefficients computed in 1. and 2.

Steps 1. and 2. are the same as described in subsections 2.3.1 and 2.3.2. The alignment procedure is explained in what follows.

2.3.3.2 RF and LF calibrations alignment

After the calibration procedures described in sections 2.3.1 and 2.3.2., the error coefficients are known both for the RF and LF measurement paths besides an unknown delay, as expressed in eqs. (2.3) and (2.4). Note that such delay affects only the phase φ, as the other coefficients are obtained from ratioed quantities.

$$\begin{bmatrix} a^i_{1D,LF} \\ b^i_{1D,LF} \\ a^i_{2D,LF} \\ b^i_{2D,LF} \end{bmatrix} = \left|K^i_{LF}\right| e^{j(\varphi^i_{LF}+2\pi i\tau_{LF})} \begin{bmatrix} 1 & \beta^i_{1LF} & 0 & 0 \\ \gamma^i_{1LF} & \delta^i_{1LF} & 0 & 0 \\ 0 & 0 & \alpha^i_{2LF} & \beta^i_{2LF} \\ 0 & 0 & \gamma^i_{2LF} & \delta^i_{2LF} \end{bmatrix} \begin{bmatrix} a^i_{1M,LF} \\ b^i_{1M,LF} \\ a^i_{2M,LF} \\ b^i_{2M,LF} \end{bmatrix} \tag{2.3}$$

$$\begin{bmatrix} a^i_{1D,RF} \\ b^i_{1D,RF} \\ a^i_{2D,RF} \\ b^i_{2D,RF} \end{bmatrix} = \left|K^i_{RF}\right| e^{j(\varphi^i_{RF}+2\pi i\tau_{RF})} \begin{bmatrix} 1 & \beta^i_{1RF} & 0 & 0 \\ \gamma^i_{1RF} & \delta^i_{1RF} & 0 & 0 \\ 0 & 0 & \alpha^i_{2RF} & \beta^i_{2RF} \\ 0 & 0 & \gamma^i_{2RF} & \delta^i_{2RF} \end{bmatrix} \begin{bmatrix} a^i_{1M,RF} \\ b^i_{1M,RF} \\ a^i_{2M,RF} \\ b^i_{2M,RF} \end{bmatrix} \tag{2.4}$$

The delay difference τ_{LF} - τ_{RF} would specifically lead to an incorrect waveforms reconstruction when modulation is applied and so both LF and RF frequency components pop up in the spectrum of the signals. A procedure to account for the delay difference, is here conceptually described and it is valid both for coaxial and on-wafer DUTs. How it is practically performed is explained in Appendix A.

A RF multi-tone signal is generated with a vector signal generator (ESG). The carrier of the signal is set equal to the fundamental frequency of the RF calibration grid whereas the modulation frequency is fixed to 100 kHz. The RF modulated signal and its in-phase (I) components are available on the panel of the generator. Afterwards, the RF and the I signals are separately connected to a reference point of the set-up and measured by triggering the A/D converters with a marker available on one of the connectors of the panel of the ESG. This marker is generated by the ESG each time the first point of the signal is applied to the IQ modulator. The measured RF and LF signals are then corrected with the RF and LF calibration coefficients of eqs. (2.3) and (2.4). Next, the delay difference is estimated by aligning the corrected and delayed waveforms with the reference signals uploaded into the ESG. The RF and I time-domain waveforms before and after alignment are reported in Figures 2-5 and 2-6.

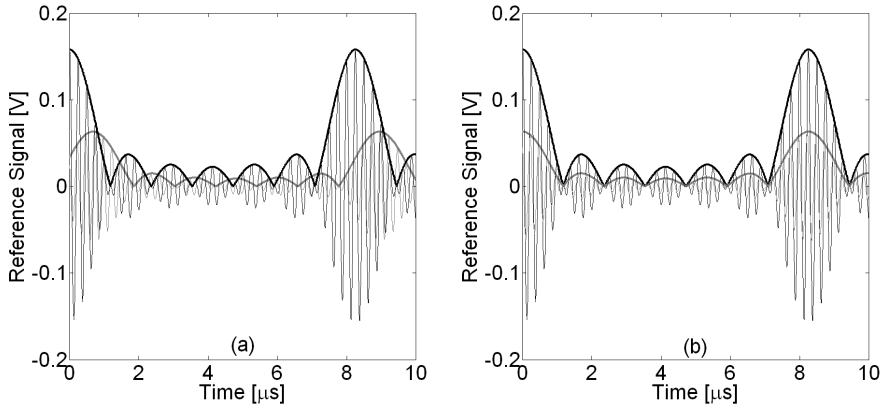

Figure 2-5 Time-domain waveforms of the measured RF signal (grey) and of the reference signal (black). (a) before alignment and (b) after alignment.

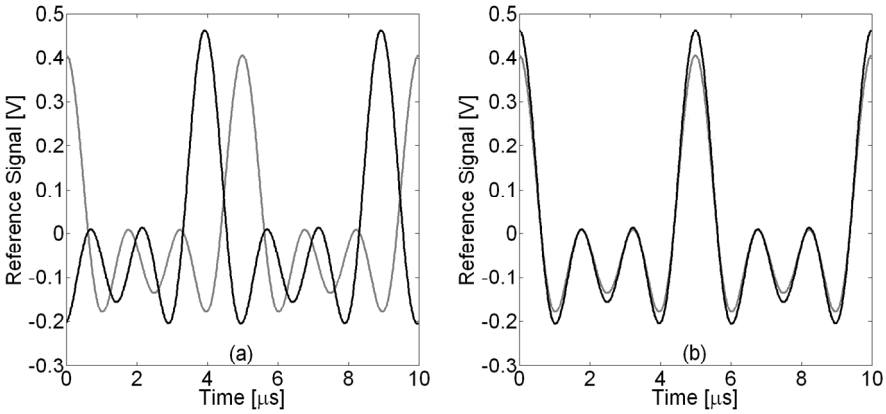

Figure 2-6 Time-domain waveforms of the measured in-quadrature signal component (I) (grey line) and of the reference signal (black line). (a) before alignment and (b) after alignment.

2.4 Examples

In order to demonstrate the system capabilities, some experimental examples are here illustrated. The RF two-tone test is performed on a power amplifier (PA) stage and an on-wafer transistor. On-wafer LF active load-pull measurements are also reported. These results have been published in [15], [22], and [23].

2.4.1 Connectorized power amplifier

Two-tone measurements are performed on a connectorized power amplifier mounted on a printed circuit board. This experiment is aimed to test the capability of the LF-RF LSNA to detect memory-effects. The bias condition is fixed as well as the power of the input tones. The spacing between the input tones is swept from 10 kHz to 400 kHz and the carrier frequency is equal to 950 MHz. A simplified schematic of the circuit is depicted in Figure 2-7. The RF and DC/LF ports of the DUT are connected to the RF and LF PORT1-2 of the set-ups in Figures 2-1 and 2-2, respectively. In order to retrieve the spectral components at the active device terminals, the calibrated quantities measured at the RF and LF ports have to be shifted up to the device plane for a meaningful comparison of voltage and current waveforms on different frequency scales. This is straightforwardly accomplished by applying ABCD transformation to the measured LF and RF spectral components. The ABCD matrices have been calculated from the available models of the matching and bias networks.

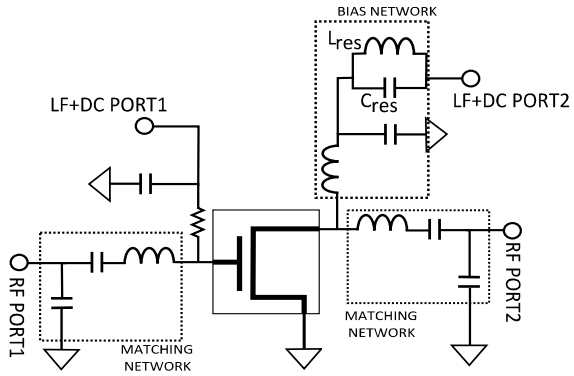

Figure 2-7 Schematic of the considered PA stage

Long-term memory effects are on purpose induced in the circuit by adding a resonant LC network on the drain bias path. Generally, circuit related memory effects, originated in this case by the frequency dependent LF output impedance [24] are more significant than the ones induced by the active device itself [25]. Moreover, the active device employed in the circuit has been characterized with pulsed measurements [26] and its dynamic characteristics do not manifest significant dispersion, at least under isodynamic conditions. Nevertheless, the selection of this circuit has been made with the sole purpose to assess the system, independently on the origin of the memory effects. Since long-term memory effects

occur at the signal envelope frequency scale (i.e., baseband) the contribution of the LF input impedance is neglected in the following analysis. Actually, the electrical behavior of the input port is mainly dominated by the transistor input capacitance which is an open circuit at the envelope frequency.

The results of the two-tone experiments are illustrated in Figures 2-8 and 2-9, where the RF output voltage and the LF output current are shown as a function of the signal tone-spacing, which is double the modulation frequency (f_m).

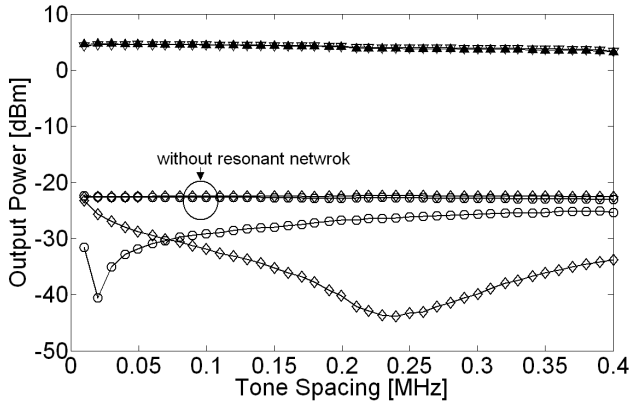

Figure 2-8 RF response of the circuit in Figure 2-7 as a function of the modulation frequency at: f_0-f_m (white triangle), f_0+f_m (black triangle), f_0-3f_m (circle), f_0+3f_m (diamond). The RF power of each of the input tones is 0 dBm and the output bias current is about 500 mA. The carrier frequency is f_0 = 950 MHz.

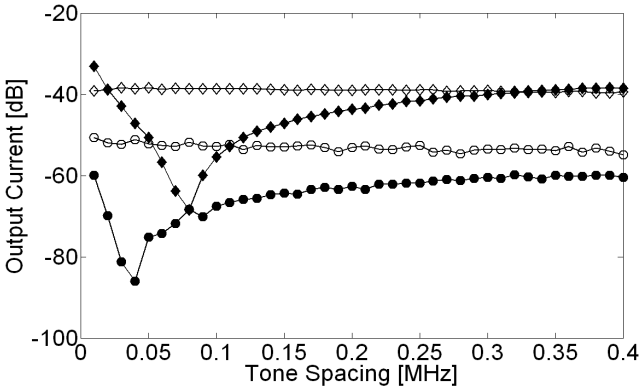

Figure 2-9 Measured second order (diamonds) and fourth order (circles) baseband intermodulation as function of the modulation frequency for the circuit of Figure 2.7 with (filled symbols) and without (white symbols) the resonant network on the bias path. The RF power of each of the input tones is 0 dBm and the output bias current is about 500 mA. The carrier frequency is f_0 = 950 MHz.

For comparison, measurements carried out on a similar circuit of Figure 2-7 but without the resonant network in the bias path are also reported.

Notably, the second order intermodulation product (IM2) and the third order intermodulation product (IM3) responses of the circuit with the resonant network manifest variation as function of the tone-spacing. A remarkable asymmetry is also observed in the IM3 response. On the other hand, when the resonant network is removed, the IM2 and IM3 show a flat response over the spanned tone-spacing. These results are in agreement with the comprehensive theoretical analysis outlined in [22] and [25], where the different vector contributions to the IM3 of the drain voltage are calculated through Volterra series expansion:

$$V_d(2f_1 - f_2) = k_1(f_1)[k_2 Z_d(f_2 - f_1) + k_3 + k_4 Z_d(2f_1)] \quad (2.5)$$

$$V_d(2f_2 - f_1) = k_1(f_1)[k_2 Z_d(f_1 - f_2) + k_3 + k_4 Z_d(2f_2)] \quad (2.6)$$

wherein Z_d is the impedance at the drain node. For the coarse analysis carried out here, all the bias-dependent 'k' coefficients are assumed constant as a function of frequency. Moreover, the frequency response of the output impedance at the fundamental frequency and the second harmonic is considered flat over the considered modulation BW. This leads to the conclusion that the baseband impedance at f_2-f_1 is the only term which is correlated with the frequency of the signal envelope, and therefore is the main source of the frequency variation of the in-band (IM3) and out-of-band (IM2) intermodulation products. The simulated response of the output impedance at the different frequency bands is here reported in Figure 2-10 and actually the assumptions previously made are verified. Moreover, as can be seen from Figure 2-10(a), the baseband impedance response is mostly determined by the resonant network since the impedance associated to L_1 = 39 nH and C_1 = 68 pF is nearly close to a short and open circuit respectively for frequencies between 10 kHz and 1 MHz. For a more detailed theoretical analysis the reader is referred to [24], [25], and [27].

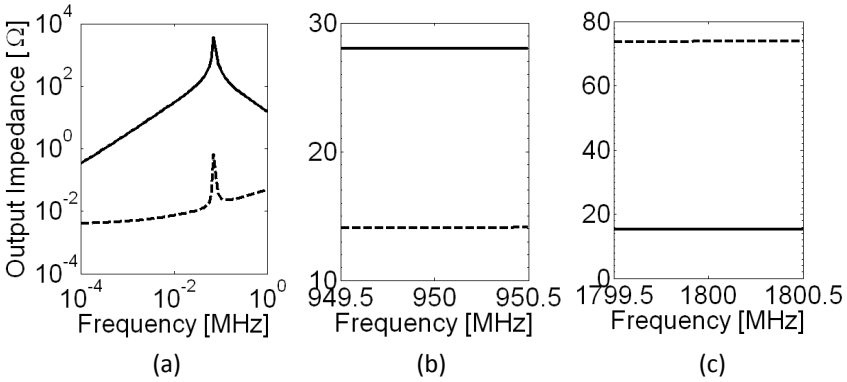

Figure 2-10 Simulated output impedance at (a) baseband, (b) fundamental, and (c) second harmonic frequencies. Magnitude (continuous line) and real part (dashed line).

For completeness also the phase response of the IM3 of the output voltage is shown in Figure 2-11 for the circuit with the resonant network on the bias path. In fact, under certain conditions, asymmetry in the IM3 phase response can be observed even if the magnitude is not asymmetric. Specifically, this can happen when the impedances at the fundamental and the harmonic frequencies are purely real whereas the one at baseband is not, as can be easily proven from eqs. (2.3) and (2.4).

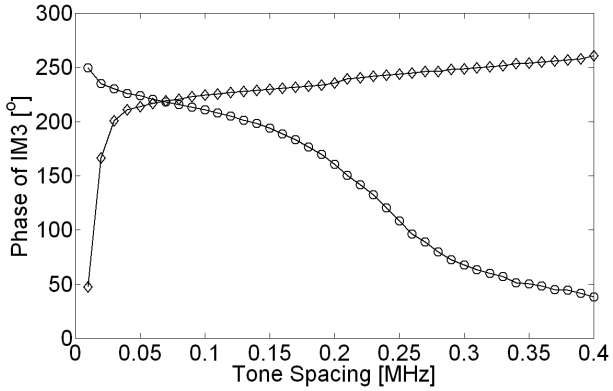

Figure 2-11 Phase response of the circuit in Figure 2-7 of lower (circle) and upper (diamond) IM3 as a function of the tone-spacing. The RF power of each of the input tones is 0 dBm and the output bias current is about 500 mA. The carrier frequency is f_0 = 950 MHz.

In this simplified analysis, the IM3 frequency dependence is mainly ascribed to the out-of-band impedances' response. In general the coefficients 'k' in eqs. (2.5) and (2.6) account for nonlinearity terms of the active devices and the gain of the circuit at the fundamental frequency [24]. Though they can be complex numbers, they are independent on the modulation frequency as also the device itself does not significantly manifest LF dispersion, as mentioned above. It is noteworthy that in [24] the device nonlinear terms account only for the nonlinear output current generator. Since the experiments here illustrated are carried out with the fundamental frequency at 950 MHz, a complete analysis should include also the distortion coefficients of the reactive nonlinearities [27]. However, it has been verified by simulation that in the present case the reactive nonlinearities do not significantly influence the variation of the IMD vector as function of the tone-spacing, and thus all the previous considerations still hold. Finally, the full analysis should account for also the higher-order nonlinearities which generate spectral components at multiple frequencies of the tone-spacing and can mix up with other terms and adding up to the IM3 response. In Figure 2-9 the spectral component of the output current at $2f_2$-$2f_1$ is also reported and, though lower than the dominant IM2 at f_2-f_1, should be theoretically included in the distortion analysis.

In the perspective of studying device related LF dynamics, it is worthy to mention that the output current intermodulation product at the baseband are a direct indication of the interaction of the signal slowly varying envelope with the dynamics induced at very low frequency scale. In the illustrated example, slow dynamics are mainly ascribed to the varying baseband impedance, but generally can be originated by other sources, such as traps and thermal effects.

2.4.2 On-wafer transistors

2.4.2.1 LF load-pull

As second example, LF load-pull measurements [28] on a transistor are illustrated. For this case the set-up is configured as in Figure 2-2 and the dynamic-bias operates as a stand-alone LF LSNA. Simply speaking, a signal with constant amplitude is applied at the input port and an amplitude varying signal is injected at the output port to actively sweep the output impedance. The fundamental frequency for this experiment is 2 MHz and, hence, all the reactive contributions (i.e., parasitics and reactive nonlinearities) are negligible. The dynamic I-V characteristics can directly be monitored and for instance their dependence on the bias and frequency can be investigated under large signal conditions. As an

example, in Figure 2-12 the output trajectories of an AlGaN/GaN HEMT on SiC are shown at two bias points. A noticeable drop of the dynamic current is observed when the drain bias voltage is changed from 20 V to 30 V. This is one manifestation of dispersion related to the presence of traps. A more detailed analysis is provided in Chapter 3. At this point of the manuscript it is important to remark how this type of characterization can be useful to evaluate also the RF performance under realistic conditions. Though the characterization frequency is much lower than the one employed for real applications, the RF output power is strongly related to the I-V dynamics which can be straightforwardly characterized with the dynamic-bias.

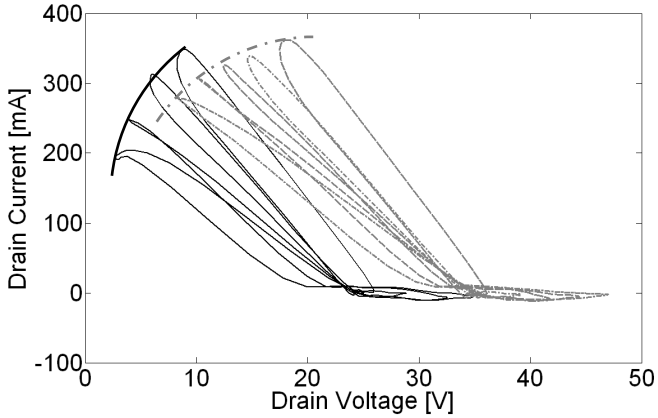

Figure 2-12 Measured dynamic I-V characteristics of an AlGaN/GaN transistor at: V_{GS0} = -4 V, V_{DS0} = 20 V (continuous line) and V_{GS0} = -4 V, V_{DS0} = 30 V (dashed line) at f_0 = 2 MHz. For illustrative purposes, the dynamic characteristics traced by the measured load-lines are also drawn.

2.4.2.2 RF modulation

For the scope of this Chapter, this example is reported to demonstrate the capability of the novel set-up to synchronously acquire the nonlinear LF and RF responses and their interaction mechanisms under large signal conditions.

The two-tone experiment is carried out on a silicon FinFET. The carrier frequency f_0 is 4 GHz and the modulation frequency f_m is swept from 10 kHz to 3 MHz. Both the power of the input tones and the quiescent point are fixed at respectively -4 dBm and V_{GS0} = 0.3 V, V_{DS0} = 0.9 V. The waveforms at the DUT terminals are acquired with the set-up in Figure 2-3 and are illustrated in Figure 2-13 for two values of the modulation frequency (the time scale in the Figure is normalized for comparison). For this particular case it emerges that the RF measured waveforms are incomplete when the LF information is not accounted for.

In Figure 2-13 the complete waveforms are also shown and as expected for the considered operating condition, the drain current clips to zero amperes when the FET is driven into pinch-off and when the displacement intrinsic current is negligible as compared with the current originated by the output current generator. Moreover, the illustrated waveforms do not show any dependence on the modulation frequency, which is one indicator of memory-less behavior.
The measured LF drain current along with the gate-source voltage RF waveforms are shown in Figure 2-14

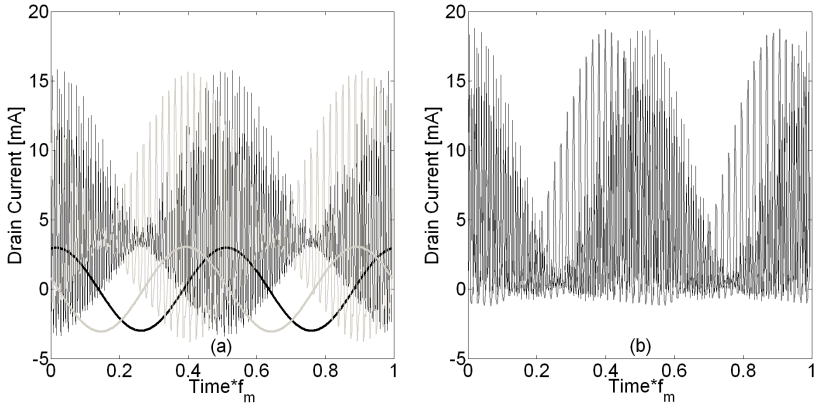

Figure 2-13 Measured RF and LF waveforms of a FinFET at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, P_{IN} = -4 dBm for each of the input tones; f_m = 10 kHz (black) and f_m = 2 MHz (grey).

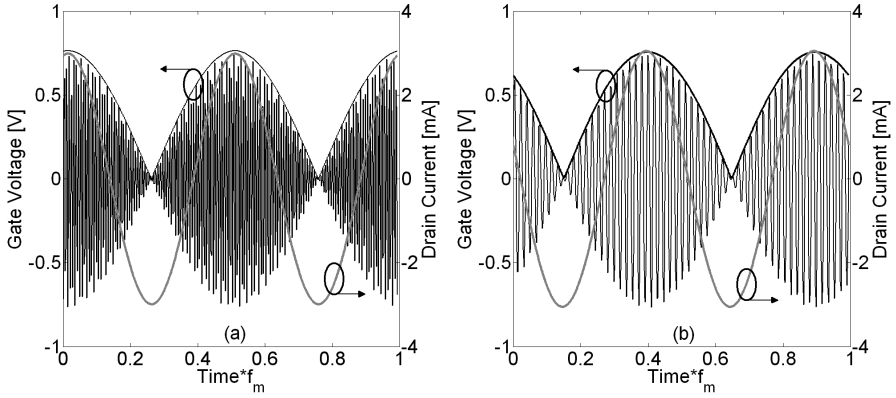

Figure 2-14 Measured LF drain current (grey) and gate-source voltage RF waveforms (black) of a FinFET at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, f_m = 10 kHz, and $P_{IN,av}$ = -4 dBm for each of the input tones. The black continuous line traces out the envelope of the RF waveform.

It is worth to observe that the LF current is correlated with the RF envelope, which is highlighted with a black continuous line in Figure 2-14. In first approximation the LF current is the result of the down conversion of the RF envelope in the baseband range. The observed alignment constitutes an indirect check of the validity of the alignment calibration step, fundamental for a correct reconstruction of the time-domain waveforms at transistor terminals.

2.5 Measurement system customization

2.5.1 Bandwidth extension

As explained in Section 2.2.2, the bandwidth limits of the dynamic-bias are imposed by the LF bias-tee and the sampling rate of the acquisition channels. While the upper boundary can be extended by making use of faster ADCs, the reduction of the lower boundary is not a trivial task when using passive reactive components for the bias-tee design. In its original version, the set-up is provided with passive LC LF bias-tees. The inductor actually sets the cut-off frequency down to 10 kHz and the further extension down to hundreds of Hertz would require a sizeable inductance which would imply more parasitics and spurious resonance. Actually the frequency response of the bias-tee may constitute an issue for the characterization addressed to highlight dispersive behavior of an on-wafer DUT as a function, for instance, of the modulation frequency. In order to isolate the sole contribution of the DUT it is then fundamental that the bias-tee response does not manifest any variation over the same bandwidth of the modulation. Note that such requirement, together with the extension down to the Hertz scale, can be straightforwardly achieved with a pure resistive network [24]. However, the resistance in the DC path may limit the characterization of power devices biased with high-voltage and high-current.

An effective solution to extend the bandwidth is proposed here by replacing the passive inductor by active components, as in the schematic circuit of Figure 2-15. As compared with the existing passive bias-tee network, the bandwidth can be significantly extended down to 100 Hz. The bias-tee response is measured with the dynamic-bias set-up configured as a LF network analyzer. The measured impedances of the active bias-tee and of the passive LC one, both loaded with 50 Ohm at the AC port, are illustrated in Figure 2-16 from 60 Hz up to 200 kHz. It is noteworthy however that, although not shown, the upper frequency limit of the active bias-tee is reduced to 5 MHz and thus that additional work is needed to cover the full bandwidth.

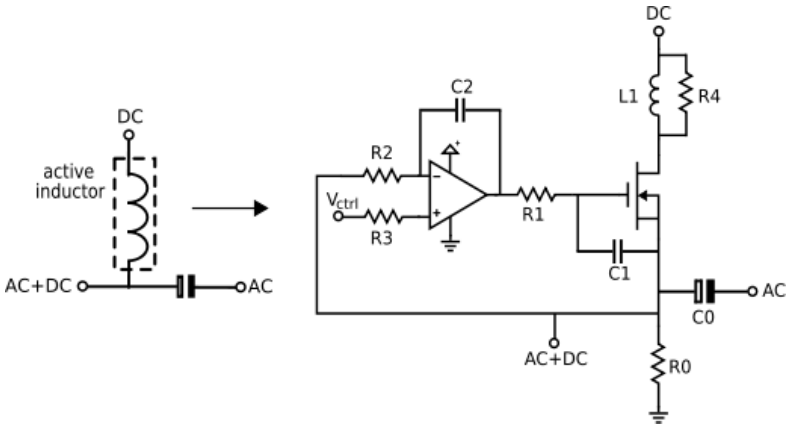

Figure 2-15 Bias-tee network based on active circuitry.

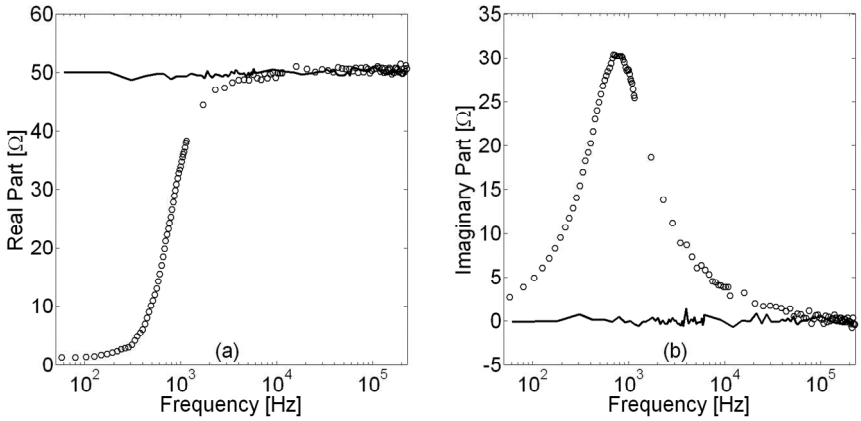

Figure 2-16 (a) real and (b) imaginary part of the measured impedance of two bias-tees terminated with 50 Ohm: LC network (circle); proposed design with active inductor (continuous line).

2.5.2 Thermal capabilities

During this work, the characterization system got equipped also with a software-controlled thermo-chuck for thermal characterization. The possibility to combine thermal characterization with on-wafer waveforms measurements is potentially relevant, also for modeling perspective. Here, in particular, the gate and drain current RF large-signal waveforms at different substrate temperatures are illustrated for a AlGaN/GaN HEMT with a 50 Ω load (Figure 2-17). Nevertheless the thermo-chuck can be used also in combination with the dynamic-bias [29].

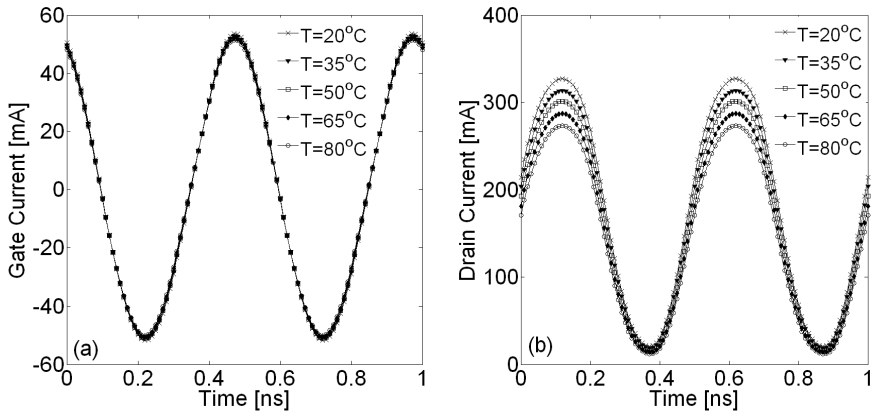

Figure 2-17 Measured (a) gate and (b) drain current waveforms of an AlGaN/GaN HEMT on SiC at different substrate (base-plate) temperatures at: V_{GS0} = -2 V, V_{DS0} = 19.5 V, and f_0 = 2 GHz.

In this example, the instantaneous drain current notably drops as expected when the substrate temperature increases whereas no significant variation is observed in the gate-current. This experimental observation has significant implications for modeling, as explained in Chapter 4. Nevertheless, the detailed investigation of thermal phenomena is out of the scope of this work.

2.6 Conclusions

A novel LF LSNA has been described in this Chapter as a solution to extend the bandwidth of an RF LSNA down to the low-frequency range. Originally the extension has aimed at complete characterization of nonlinear devices undergoing modulated excitations. In fact the LF LSNA allows detecting the intermodulation products induced at the envelope frequency scale synchronously with the RF LSNA which measures the spectral re-growth at the fundamental and harmonic frequencies. During the first part of the development phase, strongly carried out in collaboration with the NMDG company, experiments to assess the actual set-up capabilities have been performed. The possibility to detect the complete nonlinear response under modulated excitations both in frequency and time-domain is proven and highlighted. Furthermore a better insight in the interactions between the high- and low-frequency dynamics is gained.

Additionally, software and hardware modifications have been added in order to configure the dynamic-bias as a stand-alone low-frequency LSNA with time-domain load-pull capabilities. By adopting such configuration, low-frequency load-

pull experiments can be advantageously exploited to study the low-frequency dispersion of the I-V dynamics of active devices and the implication on the RF performance.

In the next chapter, a more in-depth experimental analysis is reported and the nonlinear behavior of transistors is studied under different operating conditions. It is also shown how the LF LSNA can be successfully exploited for the correct validation of high-frequency nonlinear models.

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Chapter 3

Experimental nonlinear characterization

3.1 Introduction

This Chapter is devoted to the discussion of the experimental part of the work. All the reported experiments are mostly oriented to the nonlinear characterization of different transistor technologies. More precisely, the main aim consists of highlighting dispersive effects which have become a serious issue with the introduction of new semiconductor materials for the fabrication of microwave transistors. Dispersion is commonly ascribed to physical-related phenomena, such as charge trapping and thermal effects [1]-[6]. Although these effects have dynamics which manifest with time constants much longer than the period of the signals involved in RF applications [4], [7] they can significantly influence the RF performance. Such interaction is driven by multiple mechanisms. For example, low-frequency dispersion may impair the linearity of the transistor response by affecting the in-band intermodulation products [8]- [10]. Similarly to the effect caused by a non-constant frequency response of the baseband impedance as shown in Chapter 2, device related slow dynamics may generate asymmetry between the lower and upper IM products. Generally the interaction between the low- and high-frequency responses can be straightforwardly characterized through the two-tone test by varying the offset between the two frequency carriers [11].

Dispersive phenomena have also a significant impact on the nonlinear response under one-tone CW signals or modulated signals with constant amplitude-envelope. Among others, the collapse of the deliverable output power [12]-[14] under dynamic operation constitutes a clear manifestation of dispersive effects. The origin of this phenomenon is well-researched and related to the presence of defects at the interface and bulk materials [15]. These defects act as charge trapping centers and modify the electrical field inside the semiconductor and consequently the dynamic current. Therefore it is of fundamental importance to characterize this phenomenon under conditions which are close to the real life applications. Actually, for the transistors investigated in this work, the power or current collapse has been experimentally found as the most critical effect, particularly for the GaN

technology. For this reason, a large part of the reported experiments are carried out by applying load-pull measurement techniques with the aim to highlight the transistor behavior under large-signal CW excitations.

The last part of the Chapter focuses on the thermal characterization of transistors at microwave frequencies. For this type of characterization the RF LSNA is combined with a software controlled thermal-chuck.

3.2 Modulated excitations: two-tone test

3.2.1 Two-tone experiment

The two-tone measurement is the simplest and the most widely used test to characterize the in-band distortion of nonlinear components. As regarding transistors characterization it can be successfully exploited to both investigate the nonlinear distortion related to different technologies and for the validation of nonlinear models under modulated excitation. The results of this part of the work have been reported in

G. Crupi, G. Avolio, D. Schreurs, G. Pailloncy, A. Caddemi, B. Nauwelaers, "Vector Two-Tone Measurements for Validation of Nonlinear Microwave FinFET Model," *Microelectronic Engineering*, vol. 87, no. 10, pp. 2008-2013, Oct. 2010.

A two-tone signal consists of the sum of two incommensurate CW tones [11]. In eq. (3.1) for simplicity the amplitude (A) is assumed to be the same for the two tones and the phase at the time t = 0 equal to zero degree:

$$v(t) = A\cos(2\pi f_1 t) + A\cos(2\pi f_2 t) \tag{3.1}$$

v(t) represents an amplitude modulated signal with carrier frequency f_0 and modulation frequency f_m which are defined as:

$$f_0 = \frac{f_1 + f_2}{2} \text{ and } f_m = \frac{|f_1 - f_2|}{2} \tag{3.2}$$

therefore it can be easily demonstrated that

$$v(t) = 2A\cos(2\pi f_m t)\cos(2\pi f_0 t) = V(t)\cos(2\pi f_0 t) \tag{3.3}$$

Evidently the signal in eq. (3.3) can be seen as a one-tone carrier at f_0 whose amplitude varies at the rate of the modulation frequency f_m. When such a signal

excites a nonlinear device, also the slowly varying envelope V(t) gets distorted by the device nonlinearity resulting in the generation of energy at multiple integers of f_m which actually represent the baseband signal frequency components as compared to the RF carrier f_0. As explained by Volterra series modeling approach [11], the steady-state response at baseband is determined by the interaction of the envelope V(t) with the even order nonlinearities. The latter can be described by frequency dependent kernels which account for slow dynamics either related to the active device itself or that are originated by low-frequency circuits attached to the device node, such as biasing networks. Therefore, the direct conversion of the RF envelope V(t) down to the baseband directly contains information of the interaction between the amplitude envelope of v(t) and low-frequency dynamics. In addition, due to the device nonlinearities the distorted version of the envelope appearing at the baseband may be up converted in the RF band and this generate the frequency dependence of the third order intermodulation product (IM3) vectorial response. Under certain assumptions, the frequency dependent IM3 is an indication of the up conversion of the baseband effects into the RF band. Although one is commonly interested to only in-band intermodulation products, at transistor level and from a characterization point of view it is of great interest also to look at the baseband response from which information about the low-frequency dynamics can be inferred when the device operates under large-signal condition.
As example, two-tone measurements were performed on a silicon FinFET The carrier frequency f_0 is equal to 4 GHz while the modulation frequency f_m is swept from 20 kHz to 800 kHz. The measurements are performed in 50 Ω environment. The measured second order intermodulation (IM2) component of the drain voltage at $2f_m$ is illustrated in Figure 3-1. In Figure 3-2 the measured magnitude and phase responses of the output impedance looking toward the load of the transistor are displayed.

Both the magnitude and the phase of the IM2 do not exhibit a flat response as function of the modulation frequency and a strong variation is observed at f_m = 300 kHz whose corresponding IM2 frequency component appears at 600 kHz. Nevertheless, such a significant change in the IM2 response can be primarily ascribed to the output impedance behavior (see Chapter 2, Section 2.4.1).

The change of the IM2 phase is evidently correlated to the frequency variation of the imaginary part of the LF output impedance which is determined by the measurement set-up. Similarly, the IM2 magnitude response manifests a trend which is clearly related to the magnitude response of the LF impedance. Outside the points where the impedance response varies, the IM2 exhibits a behavior independent on the modulation frequency and therefore no other sources of device

related low-frequency effects are detected. Such assumptions, namely that the transistor itself does not exhibit any LF dynamic within the investigated frequency range, are supported by the nonlinear model simulations discussed in the next Section.

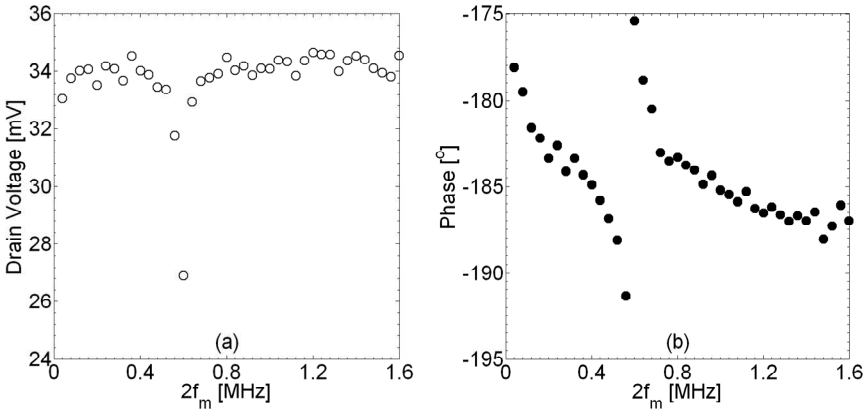

Figure 3-1 Measured IM2 spectral component of the drain voltage (at $2f_m$) for the considered FinFET as function of f_m at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, $P_{IN,av}$ = -5.8 dBm, and load impedance 50 Ω. (a) magnitude and (b) phase .

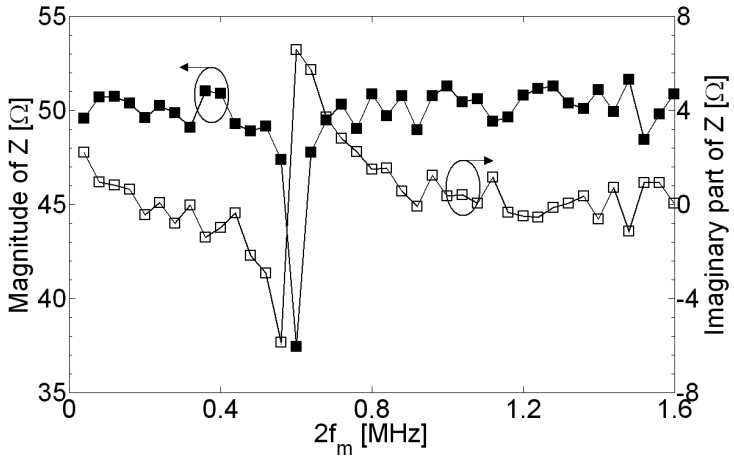

Figure 3-2 Measured magnitude (black symbols) and imaginary part (white symbols) of the output impedance determined by the measurement set-up.

3.2.2 Nonlinear model validation

▪ Modulated measurements can also be exploited to validate nonlinear models which are independently derived from other type of measurements, such as bias dependent S-parameters.

In this Section, two-tone measurements are compared with the model of the FinFET extracted as in [16]. In this model description nonquasi-static (NQS) effects are included as well. In Figure 3-3 the measured scattered wave b_2 is compared with the model predictions at the fundamental and IM3 frequencies and as function of the modulation frequency f_m, for a fixed bias condition and power level. In Figure 3-4 the simulated frequency component at $2f_m$ of the drain voltage is shown in comparison with the baseband component acquired by the LF part of the measurement set-up. The measured RF and LF frequency components exhibit good agreement with the simulated ones. Additionally, the behavior at baseband justifies the conclusion drawn in the previous section, namely the LF dynamic contribution arises only from the baseband impedance. In fact, the simulation can predict the response at baseband despite no explicit dispersive network accounting for device related dispersion had to be included in the nonlinear model formulation.

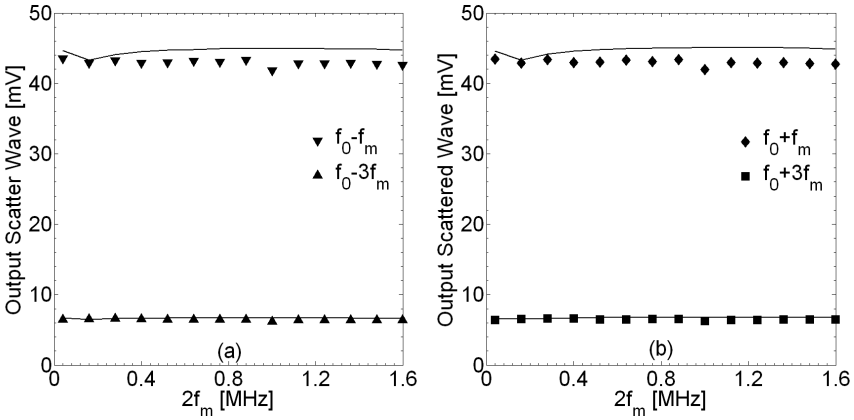

Figure 3-3 Magnitude of the output scattered wave (b_2) of the considered FinFET at the fundamental frequencies (f_0-f_m and f_0+f_m) and the IM3 frequencies (f_0-$3f_m$ and f_0+$3f_m$) at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, $P_{IN,av}$ = -5.8 dBm.

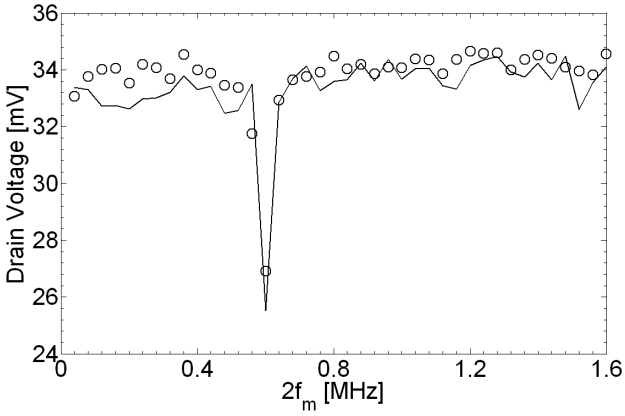

Figure 3-4 Magnitude of the drain voltage at the IM2 frequency ($2f_m$) for the considered FinFET at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, $P_{IN,av}$ = -5.8 dBm. Measurements (symbols) and simulation (continuous line).

Since the phase information is also available, experimental and simulated current and voltage waveforms are compared in Figures 3-5 and 3-6. In Figure 3-5 the measured drain current waveform is split into only the RF part, which includes the frequency components around the fundamental and harmonic frequencies, and only the LF contribution which includes the DC and the baseband even order frequency components (0, $2f_m$, $4f_m$, …, nf_m). The contribution of the LF component to the total instantaneous drain current is clearly significant, as displayed in Figure 3-5.

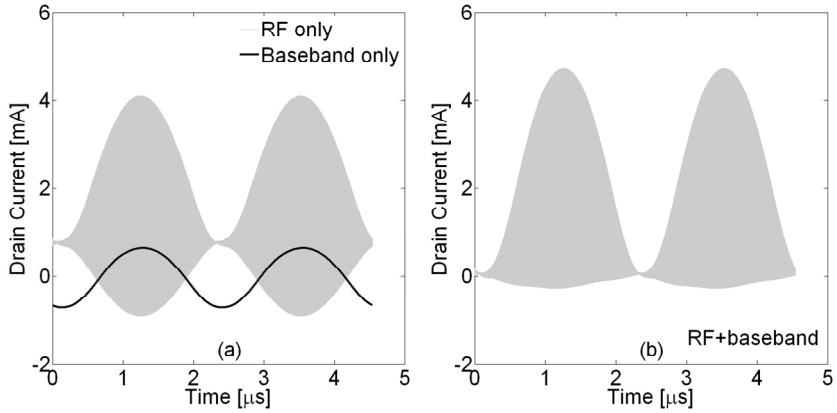

Figure 3-5 (a)-(b) Measured drain current waveform of the considered FinFET at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, f_m = 220 kHz, $P_{IN,av}$ = -5.8 dBm. (a) LF and RF contributions and (b) total instantaneous drain current is reported.

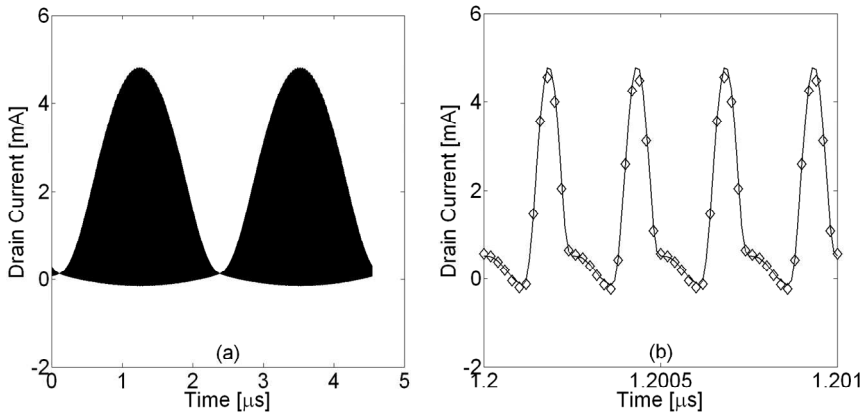

Figure 3-6 (a) Simulated drain current waveform of the considered FinFET at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, f_m = 220 kHz, $P_{IN,av}$ = -5.8 dBm; (b) snapshot within the envelope of the measured (symbols) and simulated (continuous line) drain current waveform.

In fact, only the RF current waveform instantaneously would reach negative values. Generally such behavior is originated by the intrinsic capacitances of the transistor. Nevertheless, for the considered case it is found that the capacitive contribution at the drain-source port is not very significant for the shown experimental condition and, therefore, the current response is dominated by only the drain-source current generator. This implies that the total instantaneous current cannot assume negative values when the gate voltage instantaneously crosses the points below the threshold voltage. Clearly, the LF waveforms must be added to the RF one to obtain the expected physical behavior. In Figure 3-6 the waveform predicted by the model is compared with the experimental one and the agreement is satisfactory, provided that the LF information is included.

So far it is shown that the nonlinear NQS model can reproduce accurately the nonlinear microwave measurements performed with two-tone excitation. Nevertheless, a similar level of agreement between measurements and model simulations by using the quasi-static (QS) equivalent circuit can be obtained. In fact, in Figure 3-7 it is shown that both NQS and QS nonlinear models lead to very similar and very small values of the magnitude of the vector difference D calculated as in eq. (3.4),

$$D = \left| b_2^{sim} - b_2^{meas} \right| \tag{3.4}$$

Note that this parameter accounts not only for the magnitude error but also for the phase error in reproducing the behavior of b_2. Nevertheless, it should be

highlighted that QS model allows to obtaining a significant faster convergence and simulation speed.

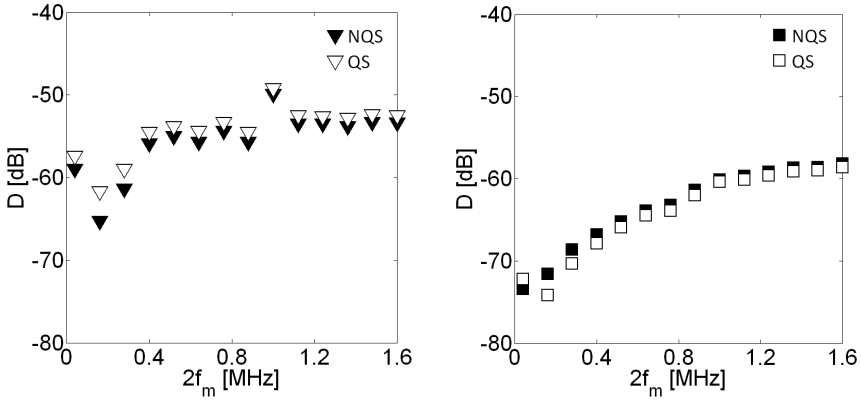

Figure 3-7 Error calculated as in eq. 3.4 at (a) f_0-f_m and (b) f_0-$3f_m$ for the output scattered wave (b_2) of the considered FinFET. The error is defined as the magnitude of the difference between the measured vector and the simulated vector with the nonquasi-static model (black symbols) and the quasi-static model (white symbols).

3.3 Load-pull

Load-pull techniques are widely employed by RF and microwave designers [17], [18]. Load-pull consists of varying the impedance at the output terminals of transistor at the fundamental and harmonic frequencies. Load-pull can be either passive or active. In the former case the impedance is varied by means of passive tuners whereas in the latter case power amplifiers are adopted. Low- and high-frequency set-ups for active load-pull measurements are schematically illustrated in Figures 3-8 and 3-9.

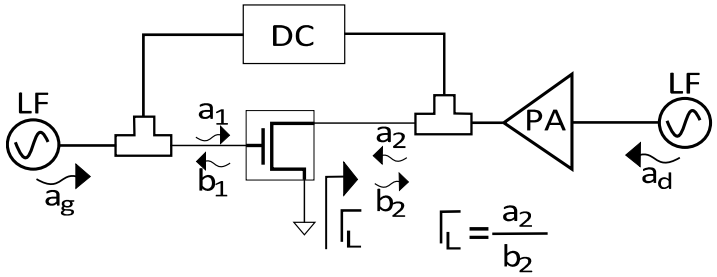

Figure 3-8 Low-frequency active load-pull set-up. Open loop configuration. Γ_L is the reflection coefficient looking toward the load of the transistor.

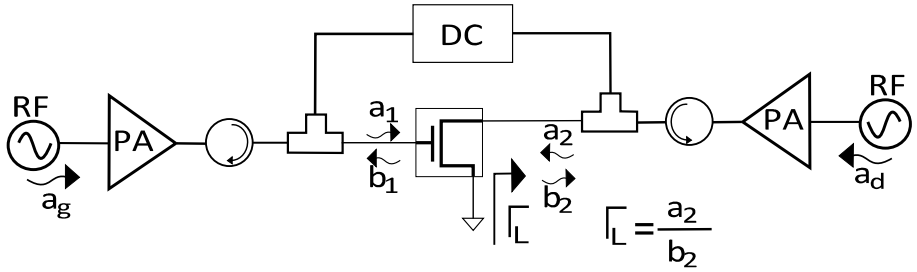

Figure 3-9 High-frequency active load-pull set-up. Open loop configuration. Γ_L is the reflection coefficient looking toward the load of the transistor.

The load impedance is related to the reflection coefficient Γ_L which is calculated as the ratio between the traveling voltage waves a_2 and b_2. In the open-loop configurations illustrated in Figures 3-8 and 3-9, the magnitude and the phase of the reflection coefficient Γ_L are changed by sweeping the amplitude and the phase of the signal injected through the power amplifier at the output port.

An application of load-pull consists of determining the constant output power contours as function of the load impedance for a fixed level of gain compression. Commonly, for such a measurement, the output power is measured with either a power sensor or a spectrum analyzer, which provide the scalar power values. However, when load-pull is performed in combination with a time-domain based acquisition system, more insight on the actual behavior of the device under test is gained since the actual current and voltage waveforms appearing at the transistor terminals are available. This aspect is extensively treated in the following Chapters. In the context of this Chapter, time-domain load-pull is exploited as a characterization 'tool'. In next Sections, load-pull techniques based on both low- and high-frequency excitations are described.

3.3.1 Low-frequency load-pull

Low-frequency based load-pull systems enable a simplified calibration and the power and frequency limitations of the external hardware components, such as power amplifiers, are not as critical as for high-frequency measurement systems. The core of the low-frequency load-pull system adopted in this work is the LF LSNA. A dual sources low-frequency load-pull system is presented in [19], though at the time of that publication it operated only above 2 MHz. The system of this work extends the lower frequency limit down to 10 kHz. In this way the large-signal characteristics of transistor can be investigated as a function of the quiescent condition and the frequency of the excitations.

3.3.2 Low-frequency large-signal transistor characterization

Under low-frequency operation, a field-effect transistor (FET) can be represented by a nonlinear current generator between the output terminals and the resistive parasitic elements. At the input terminals the FET can be approximated with an open circuit when there is no leakage in the gate oxide of silicon FET and when the gate-source and gate-drain junctions, in case of HEMT, are not driven into forward and reverse conduction. Evidently, the open circuit condition enables one to easily control the input voltage waveform. Basically, in Figure 3-8 the travelling wave a_g, which is generated by the LF signal source, will appear at the transistor input just slightly attenuated due to the insertion loss of the bias-tee and the hardware components, such as cables and the probes, placed between the device port and the signal's generator. In this way no power amplifier or tuner is required at the input port to achieve a significant voltage swing at the transistor input terminals. The situation would be different at high-frequencies (Figure 3-9), not only for the presence of reactive parasitics but also because of the impedance associated with the FET input capacitance, which can be significant for device with large gate periphery. Moreover, at low-frequencies the feedback from the gate-drain capacitance can be neglected and the input signal is affected by the output signal through only the source resistance, which is usually small. As a consequence, the gate voltage waveform can be controlled independently from the output signal and the transistor can be straightforwardly driven into strong nonlinear regime. At the output port either a passive termination can be connected or a signal source can be used in order to actively sweep the load impedance. In case of devices operating at high voltage and current, a power amplifier may be inserted between the signal source and the device under test. When the amplitude and the phase of the input signal are fixed, the load can be changed by just sweeping the amplitude and the phase of the signal injected at the output port. For the characterization purposes of this work, the control of the impedance at the fundamental frequency f_0 is sufficient. However multiharmonic control [20] can be straightforwardly included.

This kind of characterization is oriented to the investigation of the device behaviour when the exciting signals are such that the current and voltage waveforms reach the boundaries of the device operating area. Simply speaking, these boundaries are represented by the knee point (V_K in Figure 3-10), which establishes the onset of the linear region, and the high-electric field region corresponding to the high drain voltage region (V_{BD} in Figure 3-10), where reverse breakdown or impact ionization phenomena can occur. A very low value of the

knee voltage and a large value of the breakdown voltage are preferred for power amplifier design in order to maximize the swing of the signal and hence the delivered power. Therefore, all the experiments reported in this section are aimed at characterizing these boundaries as function of the device operating conditions, such as bias point and frequency. It is however worth to mention that for transistors fabricated with wide bandgap materials, the high-electric field condition may correspond to values of the gate and drain voltages which exceed the maximum ratings of the measurement system. For this reason most of the reported experiments focus on the investigation of the transistor response in the knee region.

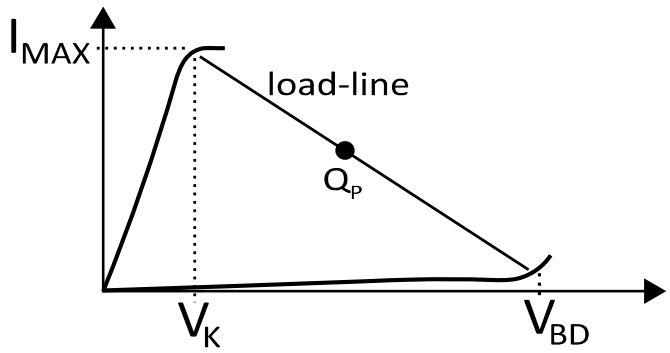

Figure 3-10 Typical voltage swing of a load line for a transistor biased at the quiescent point (QP) for class-A operation.

In Figure 3-10, the load-line is plotted on top of the transistor output I-V characteristics. When dispersion is negligible, these I-V output characteristics are replaced by the ones measured under DC conditions and remain the same regardless the point the transistor is biased at and the frequency. Said in other words, the points V_K and V_{BD} measured statically do not change under dynamic operation. On the other hand, if dispersion is significant, the DC I-V characteristics do not completely describe the actual device behaviour since depending on the bias condition, on the excitation frequency, and on the thermal state, the device dynamic boundaries can change. As a consequence, when bias point and frequency are fixed, the measured load-line must be strictly compared with the dynamic I-V characteristic measured in that particular operating condition. It is worth to mention that the I-V characteristics are the ones which strictly describe the behaviour of only the output current source of a FET. As it will be pointed out in the next Chapters, the measurement of these characteristics at very high-frequencies is not immediate and straightforward as in the low-frequency range.

3.3.3 Experimental results

The experimental activity reported in this Section has been summarized in

- G. Avolio, D. Schreurs, B. Nauwelaers, A. Raffo, G. Vannini, G. Crupi, "Bias and frequency dispersion of dynamic I-V characteristics in microwave transistors," *European Microwave Integrated Circuits Conference (EuMIC)*, pp. 93-96, 10-11 Oct. 2011,

Three types of transistors are investigated, namely a silicon FinFET (L = 60 nm, W= 45.6 um), a GaAs pHEMT (L = 0.35 um, W = 1440 um), and a GaN HEMT (L= 0.7 um, W= 800 um). As stated before, for a non-dispersive device the static and the dynamic response are coincident. This is the case of the considered silicon based FinFET, whose measured load-lines are displayed in Figure 3-11 for two quiescent conditions and at f_0 = 200 kHz and f_0 = 2 MHz. The load-lines are compared with the static output characteristic at V_{GS0} = 1.1 V and V_{GS0} = 1.2 V.

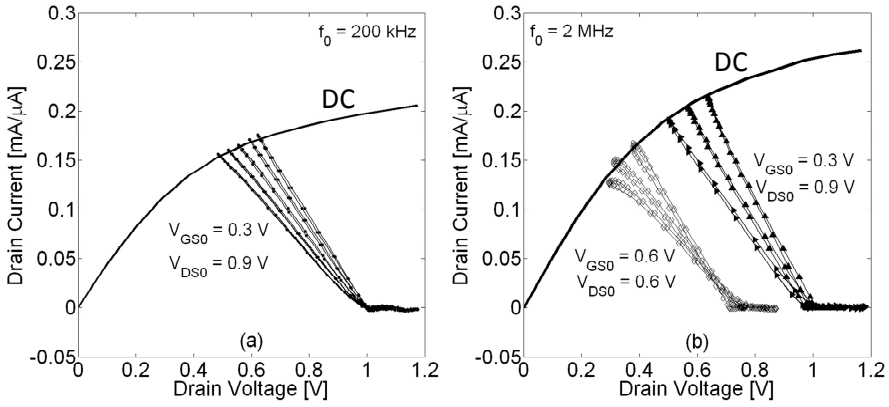

Figure 3-11 Measured load-lines (symbols) for the considered silicon FinFET at: (a) f_0 = 200 kHz, V_{GS0} = 0.3 V, and V_{DS0} = 0.9 V and (b) f_0 = 2 MHz, V_{GS0} = 0.3 V and V_{DS0} = 0.9 V and V_{GS0} = 0.6 V and V_{DS0} = 0.6 V. In (a) and (b) each measurement corresponds to a different load impedance. The I_{DS}-V_{DS} static output characteristic at (a) V_{GS0} = 1.1 V and (b) V_{GS0} = 1.2 V is also shown.

Note that for each measured load-line, the amplitude of the injected input signal is adjusted in order to obtain for the gate voltage a maximum instantaneous value equal to 1.1 V and 1.2 V respectively. Moreover, the phase shift between the injected input and output signals is kept as close as possible to 180 degrees. In this way, the instantaneous drain voltage reaches its minimum value when the gate

voltage reaches its maximum value. This allows the comparison between the dynamic and static current for the same values of the gate and drain voltages. From Figure 3.11 it emerges that, based on the definition of dispersion in this work, the FinFET does not manifest any dispersive effect, regardless the frequency and the quiescent condition which the load-lines are measured at.

The same experiment is carried out for the GaAs and GaN transistors. The measured load lines of the GaAs pHEMT are illustrated in Figure 3.12 for two bias points V_{GS0} = -0.6 V and V_{DS0} = 6 V and V_{GS0} = -2 V and V_{DS0} = 10 V, and two frequencies 20 kHz and 2 MHz. The amplitude of the injected input signal is such that the maximum instantaneous value of the gate voltage reaches 0 V. The relative phase is kept equal to 180 degrees as before. In this way minimum instantaneous value of the drain voltage occurs when the gate voltage is at the maximum for all the measured load-lines. This condition is actually satisfied as reported in the same Figure, where the measured gate and drain voltage waveforms corresponding to three measured load-lines are illustrated. The comparison between the load-lines and the static output characteristic at V_{GS0}= 0 V reveals that also the response of the GaAs transistor is not affected by dispersion related to traps. In fact the 'dynamic' knee voltage does not change as compared with the static 'knee' characteristic, regardless the quiescent condition and the frequency of the excitations. Clearly, this is valid within the investigated frequency range, which is limited by the measurement hardware. In Figure 3.12 only a slight drop of the dynamic current with respect to the static current is observed and that is ascribable to thermal effects.

Differently from the FinFET and the GaAs transistors, a strong dispersive behaviour is observed for the GaN HEMT. A clear knee-walkout is visible in Figure 3-13 and its deviation from the static characteristic increases with frequency. In fact, for a fixed bias condition, both the traps and the temperature variation cannot follow the fast variation of the signals and eventually are frozen to a steady state condition when the frequency is above the inverse of their characteristic time-constants. In Figure 3-13 the measured dynamic characteristics are reported at two frequencies, namely f_0 = 20 kHz and f_0 = 2 MHz. A significant jump is observed between the measured DC characteristic and the load-lines at 20 kHz. For values larger than 20 kHz the dynamic characteristics tend to settle at around 2 MHz. This value is in agreement with the values reported in literature for these transistors [13]. When the value of 2 MHz is reached, no significant changes in the dynamic response are observed and actually the load-lines measured at 4 MHz coincide with the ones at 2 MHz.

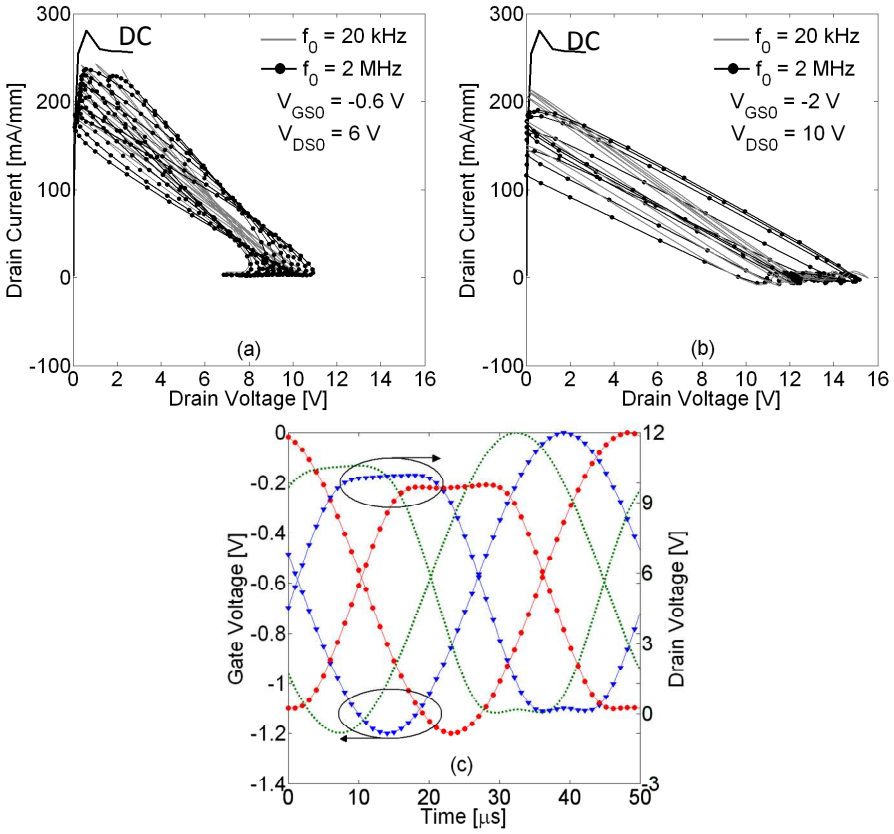

Figure 3-12 Measured load-lines for the GaAs pHEMT at: (a) V_{GS0} = -0.6 V, V_{DS0} = 6 V, (b) V_{GS0} = -2 V, V_{DS0} = 10 V, and f_0 = 20 kHz (grey line) and f_0 = 2 MHz (dotted line). DC output characteristic at V_{GS0} = 0 V (black continuous line). In (c) the measured gate and drain voltage waveforms corresponding to three measured load-lines are shown. The maximum instantaneous value of the gate voltage is aligned with the minimum instantaneous value of the drain voltage.

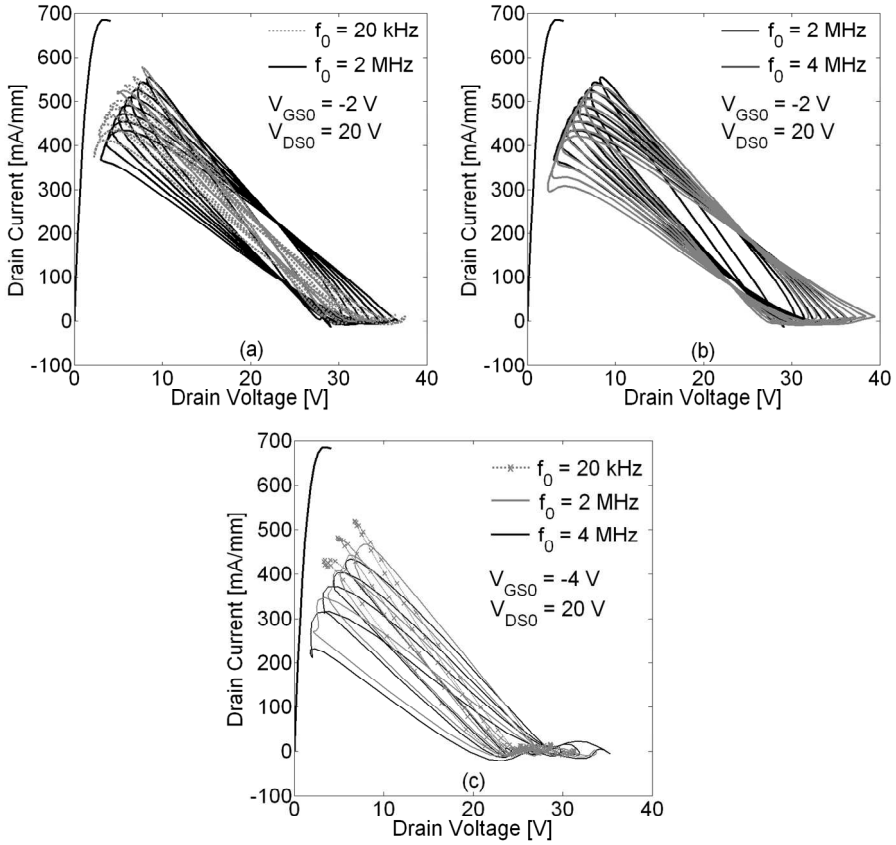

Figure 3-13 Measured load-lines for the considered GaN HEMT: (a) V_{GS0} = -2 V, V_{DS0} = 20 V, f_0 = 20 kHz, and f_0 = 2 MHz; (b) V_{GS0} = -2 V, V_{DS0} = 20 V, f_0 = 2 MHz, and f_0 = 4 MHz; (c) V_{GS0} = -4 V, V_{DS0} = 20 V, f_0 = 20 kHz (cross), f_0 = 2 MHz (black continuous line), and f_0 = 4 MHz (grey continuous line). Each measurement corresponds to a different load impedance. In all the plots also the measured static I_{DS}-V_{DS} characteristic at V_{GS0} = 0 V is shown (continuous line).

Nevertheless, it must be pointed out that although the frequency dependence vanishes above 2 MHz, the frequency independent dynamic characteristics are still dependent on the quiescent point. This condition is referred in literature as the 'above cut-off' dispersion.

3.3.4 High-frequency load-pull

A simplified open-loop configuration for active-load pull at high-frequencies is illustrated in Figure 3-9. As for the LF part, the load can be changed either by

inserting passive tuners or actively by amplifying the injected signal at the output port. At the input port the situation is similar: either a tuner or a power amplifier must be inserted at the input side when the input admittance of the transistor becomes significant at high-frequencies and, therefore, causes the drop of the amplitude of the actual controlling gate voltage. In this work high-frequency load-pull experiments are exploited for modeling purposes. As mentioned before, for characterization the LF load-pull is conveniently exploited. The schematic in Figure 3-9 represents open loop architecture and, therefore, the control of the relative amplitude and phase of the injected signals is not as straightforward as in the low-frequency range. This is due to the presence of parasitic elements and not negligible feedback at high-frequencies. Alternatively a closed loop configuration can be exploited to adjust the amplitude and phase shifted in order to achieve the desired impedance [21]. Even so, the synthesized RF load line can poorly provide direct information on the actual load line at the output current generator terminals due to the presence of parasitic elements and the intrinsic transistor nonlinear capacitances. This justifies the advantage of adopting low-frequency based characterization techniques for the investigation of devices which are primarily meant for high-frequency applications. This aspect is stressed in Chapter 4 where modeling aspects are dealt with and it is outlined how the low-frequency based characterization can be beneficially exploited for modeling purposes as well.

3.4 Thermal characterization at microwave frequencies

The investigation of microwave characteristics as function of temperature represents a key issue for active solid-state devices [22], since the operating temperature can strongly affect not only the transistor performance but also its lifetime to failure. In light of the fact that such a study is of crucial importance especially for high-power devices, this Section focuses on investigating the temperature dependent behavior of a GaN HEMT. The outcome of this study can be found in

- P. Barmuta, G. Avolio, D. Schreurs, A. Raffo, G. Crupi, K. Czuba, “Temperature dependent vector large-signal measurements,” *Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC)*, pp. 21-24, Vienna, Austria, 18 - 19 April 2011,
- G. Crupi, G. Avolio, A. Raffo, P. Barmuta, D. Schreurs, A. Caddemi, G. Vannini, “Investigation on the thermal behavior of microwave GaN HEMTs,” *Solid-State Electronics*, vol. 64, no. 1, pp. 28-33, Oct. 2011.

The microwave performance is studied by using both scattering (S-) parameter measurements up to 40 GHz and large-signal measurements carried out with a fundamental frequency of 2 GHz. Although the investigated frequencies are above the cut-off frequency of the low-frequency dispersive effects, the device behavior at such high-frequencies strongly depends on the impact of traps and thermal phenomena on the associated DC quiescent point, as extensively explained in the previous Sections. For the large-signal characterization at high-frequencies, the RF LSNA is combined with a software controlled thermo-chuck [23]. A user-friendly home-made software has been developed for measurement automation. Issues such as drift and calibration have been investigated over the considered temperature range. Under high-frequency large-signal conditions, the constant junction temperature (T) is determined by the base plate temperature (T_C) and the average value of dissipated power (P_D) as expressed in eq. (3.5):

$$T = T_C + R_{TH} P_D \tag{3.5}$$

where R_{TH} is the thermal resistance. It is worth to observe that the model in eq. (3.5) is a simplification and it is here reported only for explanatory purposes. In this work, in order to modify the junction temperature, the base plate temperature T_C is swept. The value of P_D depends instead on the DC dissipated power and the RF power transferred to the load of the transistor.

The fundamental frequency was set equal to 2 GHz, the bias at V_{GS0} = -2 V and V_{DS0} = 19.5 V whereas both the available input power and the ambient temperature were swept. As expected, a clear dependence on the temperature is observed in the large-signal gain response whose magnitude drops as the substrate temperature increases as shown in Figure 3-14. This is in agreement with the experimental observations of the small-signal gain (see inset of Figure 3-14).

In order to gain a deeper insight into the influence of the temperature on the dynamic large-signal operation, the measured load lines at the 1 dB compression point are shown in Figure 3-15. Clearly, the more the temperature increases the lower the swing of the load line is, and hence a reduction of the output power can be observed as reported in Table 3-I.

Table 3-I Measured values of the input and output power at 1-dB compression point and for different substrate temperatures (T). The operating condition is the same as in Figure 3-15.

T (^{o}C)	20	35	50	65	80
$P_{IN,av}$ (dBm)	13.9	13.8	13.8	13.8	13.7
P_{OUT} (dBm)	28.0	27.6	27.4	27.0	26.6

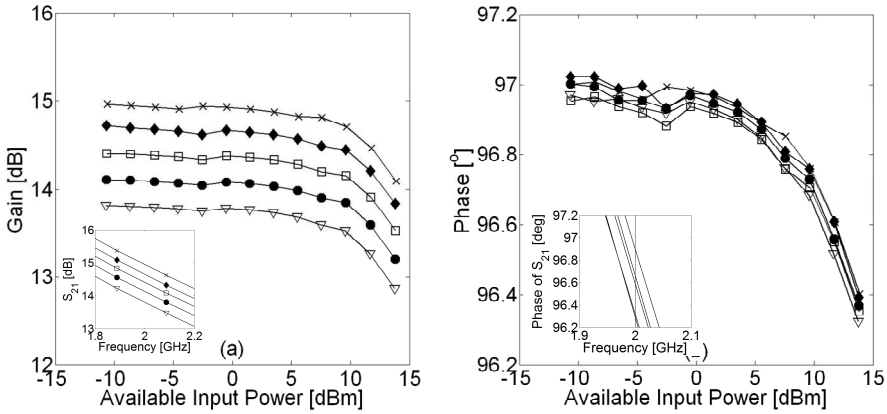

Figure 3-14 Measured (a) magnitude and (b) phase response as function of the input power of the considered GaN HEMT at: f_0 = 2 GHz, V_{GS0} = -2 V, and V_{DS0} = 19.5 V. The substrate temperature is swept T = 20 °C (crosses), T = 35 °C (diamonds), T = 50 °C (squares), T = 65 °C (circles), and T = 80 °C (triangles). In the inset the (a) magnitude and (b) phase at 2 GHz of the small-signal parameter S_{21}.

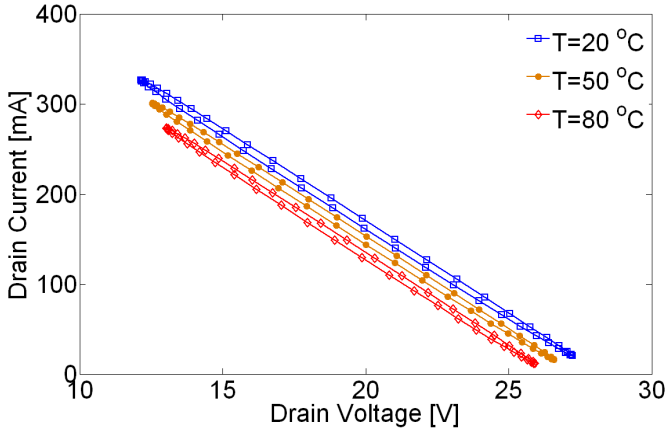

Figure 3-15 Measured load-lines for the considered GaN HEMT at: f_0 = 2 GHz, V_{GS0} = -2 V, V_{DS0} = 19.5 V, $P_{IN,av}$ ≈ 13.8 dBm, and load impedance = 50 Ω.

It is interesting to observe that the temperature change has more visible effect on the magnitude of the gain response rather than on the phase, and this in both the large- and small-signal condition. The phase rotation of S_{21} as function of frequency is caused by both the transistor intrinsic capacitance and the parasitic elements due to transistor layout. The fact that the phase rotation remains the same regardless the temperature variation in first approximation indicates that the values

of both the transistor capacitances and the layout parasitics do not change with temperature. This can be deduced also looking at the large-signal time-domain waveform of the gate current, which is mainly generated by the input transistor capacitances and which does not exhibit any dependence on the substrate temperature (see Figure 2-17 in Chapter 2).

3.5 Conclusions

This Chapter reports on the experimental activity aimed at the nonlinear characterization of solid-state active devices. All the reported and discussed experiments were oriented to investigate the effect of low-frequency dispersion on the large-signal characteristics of the considered transistors. It has been found that for the investigated devices and within the operating bandwidths of the characterization system, the knee walk out and current collapse under dynamic condition are the most significant evidences of dispersion, especially for the GaN technology. These phenomena have been highlighted by performing time-domain active load-pull measurements in the low-frequency range for different bias and frequency conditions. When the dynamic response is compared with the static one (i.e., measured under DC condition) the knee of the output characteristics of transistor strongly walks out. Eventually the knee does not longer shift when the excitation frequency reaches the cut-off of low-frequency dispersive phenomena. The advantage of using low-frequency excitations even for transistors mainly conceived for high-frequency applications is also highlighted. It is worth to observe that this part of the work has been carried out in view of the part related to modeling (Chapter 4), where the experimental current and voltage waveforms are directly exploited to identify nonlinear transistor models.

Along with load-pull, an example is reported to demonstrate the importance of acquiring the full current and voltage time-domain waveforms at transistor terminals under modulated excitations. The time-domain waveforms including both the low- and high-frequency information are necessary both for nonlinear models validation and for simultaneously monitoring low- and high-frequency dynamics and their interaction under large-signal condition.

Finally, the large-signal characteristics of a GaN HEMT are characterized at different substrate temperatures and at high-frequencies. So far, the operating condition of the transistor has been assumed to be set primarily by the signal power, the bias, and the frequency. Nevertheless, when dealing with high power density transistors the temperature effect cannot be disregarded. Therefore, it is

required to characterize the dynamic behavior of the transistor also when the operating temperature is swept. This part of the work is purely experimental and, as future work, it can be relevant to exploit the temperature dependent current and voltage waveforms for the extraction of nonlinear models which accurately account also for the thermal dependence of the transistor characteristics. This implies also the characterization and the modeling of the thermal resistance and of the time-constant associated with thermal phenomena.

In the following Chapter, linear and nonlinear modeling of transistors is dealt with.

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Chapter 4

Linear and nonlinear modeling of transistors

4.1 Introduction

This Chapter focuses on measurements-based modeling techniques for microwave active devices. The first part of the Chapter is devoted to the modeling of the linear microwave behavior of transistors. This part has been developed in the framework of a joint activity with the INTEC group (Department of Information Technology) of the University of Ghent, where a macro modeling technique has been developed for the modeling of high-frequency electromagnetic passive structures. This technique is successfully adapted for modeling of the small-signal microwave behavior of transistors and can be easily implemented in a commercial circuits simulator. As an example, the procedure is applied to the modeling of a FinFET.

The second part of the Chapter deals with the identification of nonlinear transistor models. An approach based on the use of low- and high-frequency large-signal experimental waveforms is described. The main feature of the proposed modeling technique relies in the use of large-signal measurements at different frequencies to determine the nonlinear and linear parts which compose a transistor nonlinear model. Several modeling examples are reported to demonstrate how nonlinear measurements can be exploited to identify the most significant transistor nonlinearities, such as the current-voltage (I-V) and charge-voltage (Q-V) characteristics [1]. In principle, the outlined identification technique is applicable independently on the type of active device.

4.1.1 Measurements based linear and nonlinear modeling

In what follows, the most common measurements-based modeling approaches are briefly described. It is a given that linear and nonlinear models derived directly from experiments have hugely attracted the interest of researchers and for this reason a short overview is provided in the following subsections.

4.1.1.1 Bias-dependent small-signal models

Typically, equivalent circuit models (ECM) [2] or compact models (CM) [3] are employed to predict the microwave small-signal behavior of active devices and both approaches are based on multi-bias multi-frequency S-parameter measurements. In an ECM, the bias dependent elements describing the transistor equivalent circuit are derived from measurements after de-embedding the contribution of the parasitic elements. Next, the intrinsic bias dependent elements are either replaced by a look-up-table (LUT), thus obtaining a table-based model, or alternatively, the intrinsic bias dependent elements can be approximated by analytical functions whose parameters are empirically estimated. Compact models are derived starting from the equations describing device physics and geometry. Both ECM and CM are commonly scalable and can be also used to provide feedback about a given technology. Conversely, black-box or behavioral models can be completely independent on the device physics and technology. The device to be modeled is replaced by a black-box which approximates the input output relationship with properly defined analytical functions whose parameters are estimated by optimization algorithms. Artificial neural networks (ANNs) represent an example of black-box approach exploited to describe the microwave linear behavior of transistors [4].

4.1.1.2 Large-signal models

Nonlinear models can be constructed either starting from small-signal measurements or directly from large-signal measurements. In the former case, the transistor nonlinearities, described by the current (I-V) and charge (Q-V) functions, are derived from the bias-dependent small-signal transistor parameters which are extracted, for instance, from S-parameter measurements. These small-signal parameters are then used to build the large-signal I-V and Q-V models. The large-signal models are generated by applying mathematical integration to the bias-dependent small-signal parameters [5], [6], and [7]. The values of the I-V and the Q-V functions, which depend on the instantaneous intrinsic voltages, are then stored in a LUT. It is noteworthy that the result of the mathematical integration may not be unique as the values of the I-V and Q-V functions may be dependent on the selected path of integration. Therefore the conversion of a small-signal model into a large-signal one requires also a proper selection of the integration path. Alternatively, large-signal measurements can be directly exploited [8]-[11]. Also in this case, the I-V and Q-V relationships can be either represented by a table [8]-

[10] or described by means of analytical expressions whose parameters are estimated directly from large-signal measurements [11]. The use of large-signal experiments is definitely convenient for two reasons: firstly and importantly because the models are extracted from data obtained with the device operating close to real-life. In this case one can benefit of a more accurate identification step as especially the I-V and Q-V functions give an approximate description of phenomena which are intrinsically nonlinear. Secondly, the number of experiments needed for models identification can be significantly reduced, though this aspect has to be counterbalanced with the cost of the available measurement equipment. Finally, it is worth to mention that the use of large-signal excitations allows one to instantaneously reach operating regions of the active device without incurring any degradation of the device electrical characteristics.

4.2 Linear modeling

This section deals with the modeling of the small-signal microwave behavior of active devices. Small-signal modeling is required not only to assess the microwave characteristics of new technologies but also because in a common transceiver chain many circuits, such as gain blocks or low-noise amplifiers, operate in a linear way. The approach adopted in this work belongs to the behavioral modeling category. More precisely the use of a multi-parameter rational fitting technique called multivariate orthonormal vector fitting (MOVF) [12] is investigated. This method, developed by the INTEC group (Department of Information Technology) of the University of Ghent, was originally designed for the macromodeling of passive linear systems. Nevertheless it can be promisingly applied to the modeling of active devices, as demonstrated in

- D. Deschrijver, G. Avolio, D. Schreurs, T. Dhaene, G. Crupi, L. Knockaert, "Microwave small-signal modeling of FinFETs using multi-parameter rational fitting method," *Electronics Letters*, vol. 49, no. 19, pp. 1084-1086, Sept. 2011.

4.2.1 Multivariate orthonormal vector fitting (MOVF)

Multi-parameter fitting techniques represent a successful strategy to approximate the behavior of structures and devices in the high-frequency range. Hence, the multi-bias scattering parameters S_{ik} are approximated by a parameterized multivariate model, expressed as in eq. 4.1:

$$S_{ik}(f, V_{GS0}, V_{DS0}) = \frac{N(\theta, f, V_{GS0}, V_{DS0})}{D(\theta, f, V_{GS0}, V_{DS0})} = \frac{\sum_{n_1=1}^{P_f}\sum_{n_2=1}^{P_{VG}}\sum_{n_3=1}^{P_{VD}} c_{n_1 n_2 n_3}\Phi_{n_1}(f)\Psi_{n_2 n_3}(V_{GS0}, V_{DS0})}{\sum_{n_1=1}^{P_f}\sum_{n_2=1}^{P_{VG}}\sum_{n_3=1}^{P_{VD}} \hat{c}_{n_1 n_2 n_3}\Phi_{n_1}(f)\Psi_{n_2 n_3}(V_{GS0}, V_{DS0})} \quad (4.1)$$

The numerator N and the denominator D are function of the vector of the model parameters (θ), frequency (f), and two electrical parameters, the DC gate (V_{GS0}) and drain (V_{DS0}) voltages, and are expressed in terms of the rational basis functions Φ and ψ, which are defined as in [11]. The basis functions Φ and ψ describe the frequency-dependent and parameter-dependent characteristics of the data, respectively. Note that the number of basis functions (P) is chosen for each variable independently, according to the dynamic variation of the data. To identify the unknown model parameters $\theta = \{c,\hat{c}\}$ in eq. (4.1), the method in [12] is applied. It starts from an initial guess of model parameters and computes updated values in successive iteration steps (t = 0,…,K with K equals to the number of iterations) by solving several least-squares problems:

$$\arg\min_{\theta^t}\left|\frac{N(\theta^t, f, V_{GS0}, V_{DS0})}{D(\theta^{t-1}, f, V_{GS0}, V_{DS0})} - \frac{D(\theta^t, f, V_{GS0}, V_{DS0})}{D(\theta^{t-1}, f, V_{GS0}, V_{DS0})} S_{ik}(f, V_{GS0}, V_{DS0})\right| \quad (4.2)$$

As the iteration proceeds, model in eq. (4.1) becomes an increasingly accurate approximation of the data. This process is repeated until convergence is reached. The procedure is well-known in literature as the Sanathanan-Koerner iteration, which is explained in a detailed way in [12] and [13]. By combining eq. (4.2) with a suitable weighting scheme, the mean relative error per bias point can be minimized,

$$E_{ik}(V_{GS0}, V_{DS0}) = \frac{1}{N_f}\sum_{freq}\left|\frac{S_{ik}^{meas}(f, V_{GS0}, V_{DS0}) - S_{ik}^{model}(f, V_{GS0}, V_{DS0})}{S_{ik}^{meas}(f, V_{GS0}, V_{DS0})}\right| \quad (4.3)$$

where N_f corresponds to the number of the measured frequency points.

4.2.2 Modeling results

The investigated device is a triple gate finFET fabricated in fully depleted silicon-on-insulator nMOSFET technology with a 60 nm gate length and a 45.6 μm

gate width. Multi-bias and multi-frequency S-parameters are measured with a vector network analyzer. The frequency is swept from 500 MHz to 50 GHz and both the DC gate and drain voltages are varied from 0 V to 1.2 V. The extracted model has been implemented and simulated with the Advanced Design System© (ADS) circuit simulator. Model simulation and measurements are compared at two bias points in Figure 4-1. In Figure 4-2 one of the input parameters is fixed whereas the other is swept. In both figures an excellent agreement is achieved. The accuracy of the model is further indicated by the values of the error calculated as in eq. (4.3) and whose average and maximum values are reported in Table 4-I and 4-II respectively. In the same tables the same errors are evaluated for an ANNs based model [14]. The artificial neural-network is trained with the same measurements set used to estimate the parameters of the model in eq. (4.1).

It is worth to note that the MOVF approach can be adopted alternatively to the most standard table-based approaches. Commonly, the bias-dependent small-signal parameters, in the form of Y- or S-matrix, are stored in a table which is then indexed and read within the circuit simulator. Possibly, the measured S-parameters can be directly loaded into the circuit simulator. Evidently, the size of the table, and thus the model memory usage, dramatically increases when the measurements are performed over a very wide range of bias voltages. For the MOVF, instead, only the model coefficients have to be stored in the simulator.

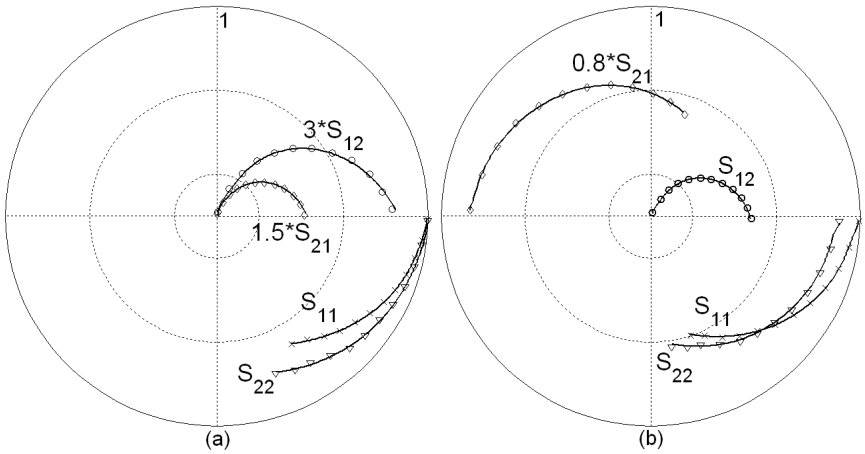

Figure 4-1 Measured (symbols) and simulated (lines) S-parameters of the investigated FinFET at (a) V_{GS0} = 0 V and V_{DS0} = 0 V and (b) V_{GS0} = 0.6 V and V_{DS0} = 0.6 V (b). The frequency is swept from 500 MHz up to 50 GHz.

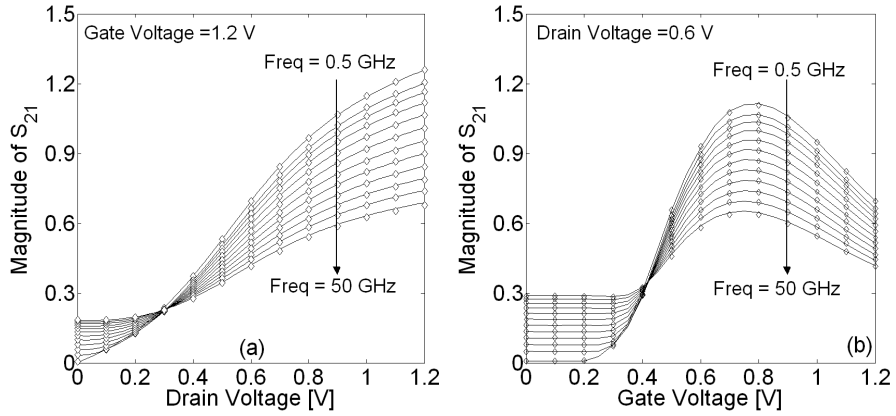

Figure 4-2 Measured (symbols) and simulated magnitude of S_{21} of the FinFET at (a) V_{GS0} = 1.2 V and V_{DS0} swept from 0 V to 1.2 V and (b) V_{DS0} = 1.2 V and V_{GS0} swept from 0 V to 1.2 V.

Table 4-I Maximum value of the error expressed as in eq. (4.3).

	E11 [%]	E12 [%]	E21 [%]	E22 [%]
MOVF	0.8	2.5	5.6	3.3
ANN	1.3	2.7	7.6	3.7

Table 4-II Average value of the error expressed as in eq. (4.3).

	E11 [%]	E12 [%]	E21 [%]	E22 [%]
MOVF	0.5	1.0	1.1	0.7
ANN	0.5	1.0	1.3	0.6

4.3 Nonlinear modeling

The identification of accurate models for nonlinear active devices is fundamental for the correct design of high-frequency circuits, such as power amplifiers. Generally the latter represent critical blocks of the transceiver chain as they operate under large-signal conditions. Consequently, the active devices used for the design of power amplifiers experience electrical signals which drive them to operate as nonlinearly. In this Section nonlinear modeling examples are reported for GaN based transistors and, therefore, the model topology depicted in Figure 4-3 is adopted. The main nonlinearities for a HEMT are commonly approximated with voltage controlled current sources (I-V functions) and voltage controlled charge sources (Q-V functions) which describe conduction and charge variation

mechanisms inside the active area of the transistor. The nonlinear current source I_{DS} describes the conduction in the channel. The I_{GS} and I_{GD} sources model the conduction in the gate Schottky junction (see Chapter 1, Section 1.4). The charge below the gate terminal is accounted for with the Q_{GD} and Q_{GS} sources, whereas the capacitor C_{DS} represent the coupling between the drain and source contacts. C_{DS} is commonly considered as a constant, being mainly a metallization capacitance [15]. In first approximation, the instantaneous response of the nonlinear current and charge sources depends on the instantaneous value of the voltages $v_{GS}(t)$ and $v_{DS}(t)$ at the intrinsic input and output ports. The latter are terminated by frequency dependent networks which incorporate the parasitics due to the device layout, and possibly package, and the frequency dependent matching and bias networks. In many practical cases all these elements are assumed to be linear. All the linear and nonlinear parts of the circuit in Figure 4-3 have their own dynamics which can cover a broad range of time constants. Commonly, fast time-constants (in the nanosecond range) are associated with the active device capacitances, parasitic elements, and matching networks. 'Slow' time-constants (ranging from ms to μs) are commonly associated with the biasing networks or with low-frequency dispersive phenomena. The latter mainly affect the response of the current source I_{DS} [16]. Under nonlinear operation the effects of these phenomena manifesting at different time scales mix together contributing to the overall response, as explained in the following Section.

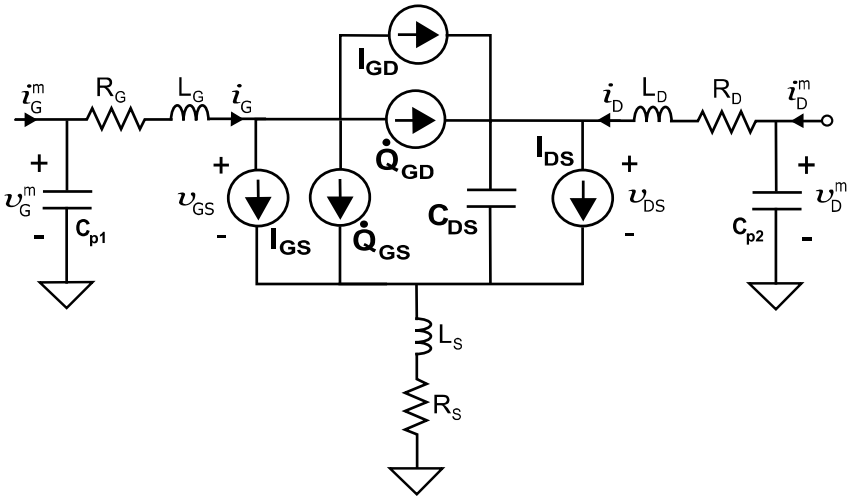

Figure 4-3 High-frequency nonlinear model of FET. In this model, the capacitor between the intrinsic drain and source terminals (C_{DS}) is assumed to be linear.

4.3.1 Nonlinear model mathematical description

The nonlinear behavior of the intrinsic part of a transistor model can be described by the following expressions:

$$I_{GS}(t) = I_{GD}(t) \sim 0 \tag{4.4}$$

$$I_{DS}(t) = f_D(v_{GS}(t), v_{DS}(t), X(t), T(t)) \tag{4.5}$$

$$Q_{GS}(t) = f_1(v_{GS}(t), v_{DS}(t)) \tag{4.6}$$

$$Q_{GD}(t) = f_2(v_{GD}(t), v_{DS}(t)) \tag{4.7}$$

wherein $I_{DS}(t)$ represents the instantaneous values of the current associated with the drain-source current generator. $I_{GS}(t)$ is assumed to be zero for all the investigated cases in this work and, for this reason, the gate-source and gate-drain current sources are omitted in Figure 4-3. The intrinsic displacement component of the gate and drain currents is simply the time derivative of the instantaneous charge and, according to the model in Figure 4-3,

$$i_G^{disp}(t) = \dot{Q}_{GS}(t) + \dot{Q}_{GD}(t) \tag{4.8}$$

$$i_D^{disp}(t) = \dot{Q}_{GD}(t) + C_{DS}\dot{v}_{DS}(t) \tag{4.9}$$

Therefore, the total intrinsic currents are

$$i_G(t) = i_G^{disp}(t) \tag{4.10}$$

$$i_D(t) = I_{DS}(t) + i_D^{disp}(t) \tag{4.11}$$

The intrinsic voltages $v_{GS}(t)$ and $v_{DS}(t)$ are determined by the impedances at the input and output intrinsic nodes through linear dynamic functions (h_G and h_D in eqs. (4.12) and (4.13)) of the measured voltage and current waveforms (indicated with the superscript 'm' in Figure 4-3):

$$v_{GS}(t) = h_G(v_G^m(t), i_G^m(t)) \tag{4.12}$$

$$v_{DS}(t) = h_D(v_D^m(t), i_D^m(t)) \tag{4.13}$$

The following assumptions are made in this work:

- the instantaneous value of the intrinsic drain current component associated with the I_{DS} generator is a nonlinear function of the intrinsic instantaneous voltages, $v_{GS}(t)$ and $v_{DS}(t)$, and of two other variables, T and X [16], [17]. The former represents the instantaneous temperature T which sets the thermal state and which affects, among others, the mobility of the carriers in the channel. The variable X accounts for the instantaneous electrical state of the traps, originated by the defects in the interface and substrate materials. In the most general case, the instantaneous value of the variable X depends on the value of the applied voltages $v_{GS}(t)$ and $v_{DS}(t)$, and their past value (see eq. (4.14)). The junction temperature T is instead expressed as in eq. (4.15), where a linear dynamic relationship between the instantaneous dissipated power and the temperature raise is assumed.

$$X(t)=f_X(v_{GS}(t-\tau), v_{DS}(t-\tau)) \tag{4.14}$$

$$T(t) = T_C + h_T(t) \otimes [P_{DC}-P_{RF}(t)] \tag{4.15}$$

  In eq. (4.15) τ represents the memory-time associated with trapping mechanisms and it ranges from 0 to ∞. Nevertheless, practically the value of τ is truncated to the finite time T_m [15]. In eq. (4.15) T_C is the base plate temperature, h_T the impulse thermal response, and P_{DC} and P_{RF} the power supplied by the DC sources and the RF power delivered to the load respectively. It is noteworthy that X and T are similar to the 'hidden' variables adopted in the formulation in [8] for the modeling of low-frequency memory effects;

- the instantaneous electrical charge between the device terminals is set by only the instantaneous value of the total intrinsic voltages regardless the value of X and T. This approximation is found reasonable in many practical situations [16], [17] especially when the device is not pushed under very extreme conditions, such as a significant thermal stress. Moreover, the functions f_1 and f_2 in eqs. (4.6) and (4.7) are here approximated with static, or frequency independent relationships as the charge responds instantaneously to signal variations when the frequency of the excitations are much lower than the inverse of the time constants associated with generation and recombination phenomena inside the semiconductor materials [18].

4.3.2 Large-signal model extraction

In literature several approaches aimed at nonlinear model extraction are reported, which exploit either directly large-signal measurements or the combination of large- and small-signal measurements. The approaches proposed by Schreurs *et al.* in [11], [19] and by Curras-Francos *et al.* [20], [21] rely on using only high-frequency vector calibrated nonlinear measurements. The values of the nonlinear currents and charges in the model of Figure 4-3 are calculated as function of the intrinsic voltages $v_{GS}(t)$ and $v_{DS}(t)$ starting from the experimental time-domain waveforms. More precisely, in [19] high-frequency CW one-tone signals are injected at both input and output ports with a slight shift in frequency. In this way an optimal coverage in the $v_{GS}(t)$-$v_{DS}(t)$ plane, over which the values of the I-V and Q-V functions are calculated, is achieved. In [19] and [20], instead, the amplitude and the phase of the signals injected at the input and output port is varied in order to obtain a non-looping $v_{GS}(t)$-$v_{DS}(t)$ characteristic at the intrinsic plane. Therefore, for a fixed pair of values ($v_{GS}(t)$, $v_{DS}(t)$), the value of both the I-V and Q-V functions can be computed. Alternatively, in [11] the I-V and Q-V functions are approximated by ANNs whose parameters are determined by numerical optimization. An ANN based nonlinear model is also proposed in [22] and the model parameters are identified on the basis of DC, small-, and large-signal measurements. All these approaches are very robust although they are limited in many cases as they do not account for low-frequency dispersion and their extrapolation capability might be inaccurate outside the range of the data set the model is extracted from.

In order to account for dispersive phenomena, an ANN based modified formulation is proposed in [23] and the I-V and Q-V model parameters are extracted starting from a very large number (~8500) of large-signal measurements performed under several bias, power, and load conditions. An alternative approach based on low-frequency large-signal measurements is proposed by Raffo *et al.* in [24]. The LF experimental waveforms can be directly exploited for the identification of only the I-V functions whereas the Q-V relationships are replaced by a LUT obtained from multi-bias small-signal measurements.

4.3.3 Moving towards low-frequency

The use of low-frequency large-signal excitations is especially beneficial for the modeling of the I-V relationships of transistors. The I-V response can manifest

dynamics over a broad frequency range, starting from the near-DC up to hundreds of megahertz due to thermal variations and charge trapping mechanisms. Clearly, the higher the frequency the less the traps state variation or the temperature can follow the swing of the electrical signals. On the other hand the higher the frequency, the more significant is the contribution of the charge sources and the fast dynamics of the electrical networks connected at the device terminals. As a consequence when the I-V relationships are measured in the RF range, they may poorly provide direct information about the actual I-V response. For this reason, one can exploit low-frequency excitations in order to isolate only the dynamics related to the current source (see Chapter 3) whose nonlinear response is assumed to be frequency independent when the measurement frequency is set above the cut-off of the LF dynamics. In addition, the LF operation differently from the HF one allows one to neglect the effect of the charge sources and of any other reactive element as compared to the contribution of the current sources and the frequency independent resistive parasitics. Evidently, the frequency limit below which such simplification is valid depends on the device technology.

In this work, low- and high-frequency large-signal measurements, and small-signal measurements are combined together to identify the linear and nonlinear parts of the model in Figure 4-3, as proposed in [25]. The I-V dynamic characteristics, which are the most sensitive to dispersive phenomena, are identified on the basis of either low-or high-frequency large-signal measurements. The nonlinear charge sources are determined either directly from high-frequency large-signal measurements or from multi-bias small-signal measurements. In the former case a semi-empirical analytical formulation [26] is adopted whereas in the latter case the charge functions are replaced by LUTs. As regarding the I-V functions either empirical or semi-empirical expressions are adopted for all the investigated cases. The use of semi-empirical analytical formulation improves the extrapolation capability of the model, whose parameters are determined through numerical optimization as detailed in the following. The results of this part of the activity have been published in

- A. Raffo, V. Vadalà, D. M. M.-P. Schreurs, G. Crupi, G. Avolio, A. Caddemi, and G. Vannini, "Nonlinear dispersive modeling of electron devices oriented to GaN power amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 4, pp. 710-718, Apr. 2010.
- G.Crupi, A. Raffo, D. Schreurs, G. Avolio, V. Vadalà, S. Di Falco, A. Caddemi, and G. Vannini, "Accurate GaN HEMT nonquasi-static large-signal model

including dispersive effects," *Microwave and Optical Technology Letters*, vol. 53, no. 3, pp. 710-718, March 2011.

▪G. Avolio, D. Schreurs, A. Raffo, G. Crupi, I. Angelov, G. Vannini, and B. Nauwelaers, "Identification technique of FET model based on vector nonlinear measurements,", *Electronics Letters*, vol. 47, no. 24, pp. 1323-1324, Nov. 2011.

▪G. Avolio, D. Schreurs, A. Raffo, I. Angelov, G. Crupi, G. Vannini, and B. Nauwelaers, "Waveforms-based large-signal identification of transistor models," accepted for oral presentation at the *IEEE MTT-S International Microwave Symposium (IMS)*, 17-22 June 2012, Montreal, Canada.

4.3.4 Model parameters estimation procedure

The parameters of the nonlinear models proposed in this Chapter are estimated through least-squares based numerical optimization. The numerical optimization is performed in combination with a harmonic-balance solver in the Advanced Design System (ADS©) environment. The optimization problem is straightforwardly formulated in order to minimize the error function (E), defined as follows:

$$E = \sum_i E_i \tag{4.16}$$

$$E_i = s_k \sum_k \left| w(t)_k^{meas} - w(\underline{P}, t)_k^{sim} \right| + r_{kh} \sum_{k,h} \left| W_{kh}^{meas} - W_{kh}^{sim}(\underline{P}) \right| \tag{4.17}$$

where the index *'i'* sweeps over all the experiments, *'k'* indicates the measured or simulated voltage or current waveform (w(t)), *'h'* is the harmonic index for the frequency spectra (W), $\underline{P}$ is the vector of the unknown parameters to be determined, and *'s'* and *'r'* are weighting factors which can be adjusted to make some terms contributing to the error function more dominant than others. The expressions in eqs. (4.16) and (4.17) can be clearly simplified and this is evaluated case by case. Practically, for all the cases reported in this work a Random Search Method is carried out for coarse optimization, followed by a Gradient Search Method for a fine tuning of the parameters. The least-square based numerical optimization runs in combination with a harmonic balance algorithm to solve the circuit in Figure 4-3. The latter, depending on the frequency of the large-signal excitations, can be simplified leading to a separation of parameters to be identified. Consequently, the optimization process can be significantly simplified as compared

with the case when the I-V and Q-V functions parameters are estimated together [11].

The following situations are investigated in this work:

- I-V parameters extracted from high-frequency large-signal waveforms measurements;
- I-V parameters extracted from low-frequency large-signal waveforms measurements;
- both I-V and Q-V parameters determined by exploiting in combination low- and high-frequency waveforms measurements.

So far, the modeling problem is stated mainly in terms of the identification of the I-V and Q-V relationships, provided that the value of the linear-parasitic elements is known either from multi-frequency S-parameter measurements [2], [15], and [17], or electromagnetic simulations of the device layout and package, or it is provided directly by the foundry. Alternatively, the value of the parasitics can be included within the optimization process. This way, one can benefit of the proper selection of the frequency range to have larger influence and sensitivity of the parasitic elements and improve the accuracy of the fit between the experimental large-signal time-domain waveforms and the simulation predictions.

4.4 Modeling of the I-V function

4.4.1 High-frequency large-signal identification

The active device is a GaN HEMT on SiC with 0.25 μm gate length and 200 μm gate width composed by two fingers of 100 μm. With reference to the circuit in Figure 4-3, the drain-source current generator is described with the empirical expression proposed in [17] and which fully accounts for dispersive effects:

$$I_{DS}(t) = [1 + \Delta_m(v_{GS}(t), v_{DS}(t), V_{GS0}, V_{DS0}, P_0] * F_{dc}(\underline{v_x(t)}, T_c) \tag{4.18}$$

$$\underline{v_x(t)} = \begin{bmatrix} v_{GS}(t) + \Delta_g(v_{GS}(t), v_{DS}(t), V_{GS0}, V_{DS0}, P_0) \\ v_{DS}(t) * (1 + \Delta_d(v_{GS}(t), v_{DS}(t), V_{GS0}, V_{DS0}, P_0)) \end{bmatrix} \tag{4.19}$$

where $v_{GS}(t)$ and $v_{DS}(t)$ are the voltages at the intrinsic plane, V_{GS0} and V_{DS0} their average values which determine the average traps' status (see eq. (4.5)). P_0 is the

average dissipated power and T_c is the case temperature. The function F_{dc} is the static drain current characteristic, which can be either approximated by a LUT or described analytically. In eqs. (4.18) and (4.19), the deviation of the dynamic behavior from the static one is accounted for with the correction terms Δ_m, Δ_g, and Δ_d. These terms change the intrinsic voltages $v_{GS}(t)$ and $v_{DS}(t)$ resulting in the modified vector of voltages $\underline{v_X(t)}$. The correction terms Δ_j (j = m, g, d) can be conveniently expressed as a function of purely dynamic terms defined as the difference between the instantaneous values of the controlling electrical quantities and the corresponding average values. The formulation adopted for the considered case study is the following [17]:

$$\begin{aligned}
\Delta_m(t) &= \alpha^m_{1,0,0}\delta_{v_{GS}} + \alpha^m_{0,1,0}\delta_{v_{DS}} + \alpha^m_{0,0,1}\delta_p \\
\Delta_g(t) &= \alpha^g_{1,0,0}\delta_{v_{GS}} + \alpha^g_{0,1,0}\delta_{v_{DS}} + \alpha^g_{0,0,1}\delta_p + \alpha^g_{2,0,0}\delta^2_{v_{GS}} + \\
&+ \alpha^g_{0,2,0}\delta^2_{v_{DS}} + \alpha^g_{0,0,2}\delta^2_p + \alpha^g_{1,1,0}\delta_{v_{GS}}\delta_{v_{DS}} + \alpha^g_{1,0,1}\delta_{v_{GS}}\delta_p + \alpha^g_{0,1,1}\delta_{v_{DS}}\delta_p \\
\Delta_d(t) &= \alpha^d_{0,1,0}\delta_{v_{DS}}
\end{aligned} \tag{4.20}$$

where the $\alpha_{x,y,z}$ coefficients are the bias-independent model parameters to be identified and $\delta_{i,j}$ represent the difference between the total instantaneous $v_{GS}(t)$ and $v_{DS}(t)$ and their average values V_{GS0} and V_{DS0}. The charge sources in Figure 4-3 are replaced by LUTs obtained from multi-bias S-parameter measurements and the parasitic elements are extracted as in [2]. Therefore, the parameters $\alpha_{x,y,z}$ are the only unknowns of the network of Figure 4-3, and they are determined by numerical optimization. High-frequency measurements at f_0 = 5 GHz and three bias conditions V_{GS0} = -2 V and V_{DS0} = 10 V, V_{GS0} = -4 V and V_{DS0} =25 V, V_{GS0} = -3.5 V and V_{DS0} = 25 V (Figure (4-4)) are exploited in the identification phase. The values of $\alpha_{x,y,z}$ obtained for the current source model are reported in Table 4-III.

Table 4-III Parameters of the nonlinear I-V model of the considered 0.25x200 µm² GaN HEMT.

$\alpha^m_{1,0,0}$ V^{-1}	$\alpha^m_{0,1,0}$ V^{-1}	$\alpha^m_{0,0,1}$ W^{-1}	$\alpha^g_{1,0,0}$	$\alpha^g_{0,1,0}$	$\alpha^g_{0,0,1}$ A^{-1}	$\alpha^g_{2,0,0}$ V^{-1}
-0.005	0.020	0.097	-0.010	-0.007	-0.088	-0.041
$\alpha^g_{0,2,0}$ V^{-1}	$\alpha^g_{0,0,2}$ $A^{-2}V^{-1}$	$\alpha^g_{1,1,0}$ V^{-1}	$\alpha^g_{1,0,1}$ W^{-1}	$\alpha^g_{0,1,1}$ W^{-1}	$\alpha^d_{0,1,0}$ V^{-1}	
-0.013	-0.00024	0.006	0.022	-0.0093	0.022	

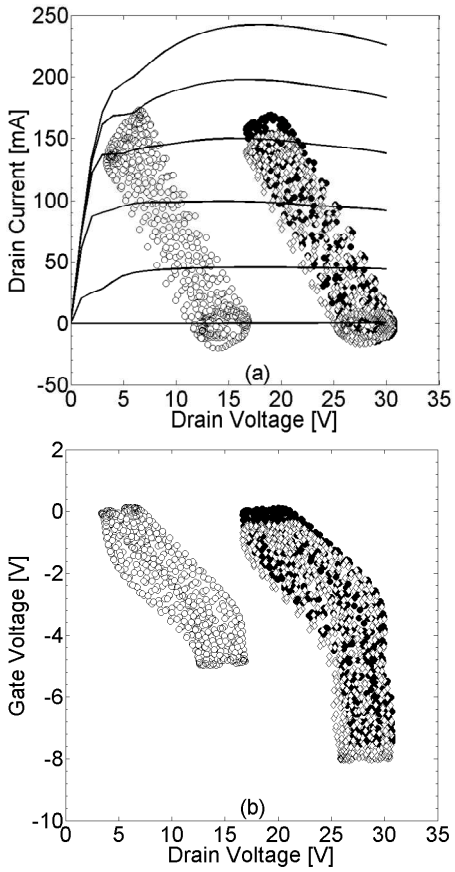

Figure 4-4 (a) Measured load lines and (b) measured input-output voltage trajectories of the investigated GaN HEMT at: V_{GS0} = -3.5 V, V_{DS0} = 25 V (black circles); V_{GS0} = -4 V, V_{DS0} = 25 V (diamonds); V_{GS0} = -2 V, V_{DS0} = 10 V (white circles), and f_0 = 5 GHz. In (a) I_{DS}-V_{DS} static characteristics are shown (continuous lines).

In Figure 4-5, measurements are compared with both the DC based nonlinear model, that is Δ_m, Δ_g, and Δ_d = 0 in eqs. (4.18) and (4.19), and with the model which includes dispersion in its formulation.

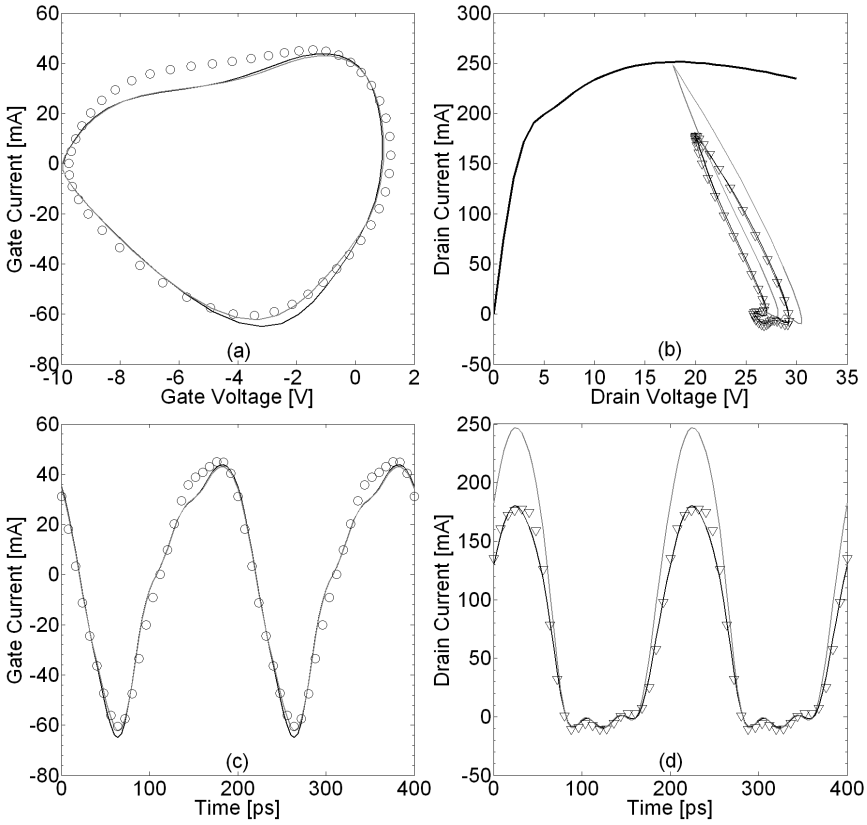

Figure 4-5 Measurements (symbols) and simulations of the model of the GaN HEMT with dispersion (black line) and without dispersion (grey line) at: V_{GS0} = -4 V, V_{DS0} = 25 V, and f_0 = 5 GHz. (a) input loci; (b) load line; (c) gate current waveforms and (d) drain current waveforms. In (b) the I_{DS}-V_{DS} static characteristic at V_{GS0} = 0.79 V is shown.

Evidently, the accuracy of the model's prediction improves significantly when dispersive phenomena are accounted for, especially when looking at the load line. Also the simulated i_G-v_G trajectory is displayed and shows good agreement with the measured one. The gate current has mainly a displacement component (see Figure 4-3) and the achieved good agreement confirms that the table representation of the voltage controlled charge sources provides accurate predictions. The model is validated under different conditions and comparison between measurements and simulations are shown in Figure 4-6. The fundamental frequency is 8 GHz and, as before, the accuracy of the model prediction improves when low-frequency dispersion is accounted for. Also, the gate current is accurately modeled. Such

validation proves that the memory-less properties of both the I-V and Q-V functions represent a good approximation within the investigated high-frequency range.

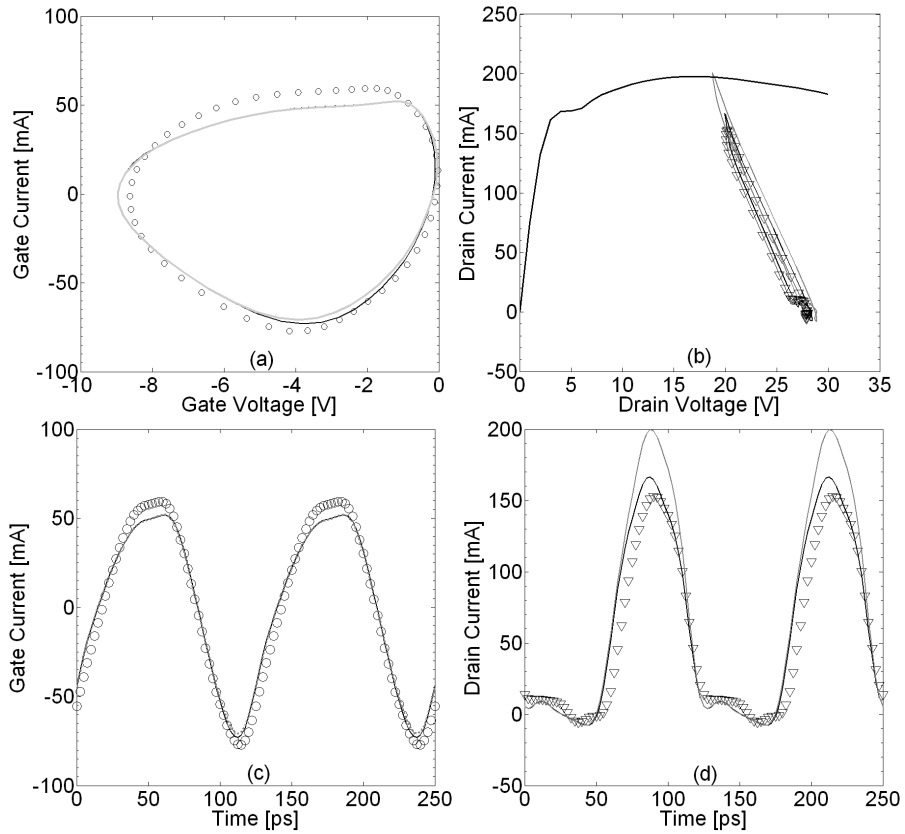

Figure 4-6 Measurements (symbols) and simulations of the model with dispersion (black line) and without dispersion (grey line) at: V_{GS0} = -4 V, V_{DS0} = 25 V, and f_0 = 8 GHz. (a) input loci; (b) load line; (c) gate and (d) drain current waveforms. In (b) the I_{DS}-V_{DS} static characteristic at V_{GS0} = 0 V is shown.

4.4.2 Low-frequency large-signal identification

In this section the nonlinear I-V model is identified directly from low-frequency nonlinear measurements performed with the LF LSNA described in Chapter 2. The investigated active device is an AlGaN/GaN HEMT on SiC substrate with 0.7 μm gate length and 800 μm gate width and which is composed of two 400 μm fingers. As explained in Section 4.3.3, low-frequency measurements can be advantageously exploited for the modeling of only the drain-source current generator. The latter is

the most critical element in the circuit of Figure 4-3, as it is strongly sensitive to dispersive phenomena. At low-frequency, the model in Figure 4-3 simplifies to only the I_{DS} source and the parasitic resistances R_S and R_D. The contribution of any reactive element can be neglected. This is beneficial because the experimental low-frequency large-signal waveforms are directly linked to the I_{DS} nonlinear response and the effect of dispersive phenomena can be directly monitored. In fact, as will be detailed in Chapter 5, when the I-V characteristics are measured at high-frequency, the link between the RF measurements and the actual response of the I_{DS} current source is not immediate as other nonlinearities, originating from the charge sources, contribute to the overall nonlinear response. Moreover, when the current source parameters are separately estimated from the charge sources parameters, the optimization time is remarkably reduced since a small number of parameters has to be identified in the simplified low-frequency model as compared to the complete circuit of Figure 4-3. As regarding the Q-V functions and the parasitic elements, in this Section it is assumed that they are known. The former are available in the form of LUTs whereas the latter are either extracted as in [2] or directly provided by the foundry.

The I-V function is replaced by the semi-empirical equations of Angelov model [26]:

$$I_{DS}(t) = I_{PK0}(T)*[1+\tanh(\psi)]*\tanh(\alpha v_{DS}(t))*[1+\lambda v_{DS}(t)] \tag{4.21}$$

$$\psi = \sum_{k=1}^{3} P_k *(v_{GS}(t)-V_{pkm})^k \tag{4.22}$$

$$\alpha = \alpha_R + \alpha_S *(1+\tanh(\psi)) \tag{4.23}$$

$$I_{PK0}(T) = IPK0*(1+T_{CIPK0}*(T-T_c)) \tag{4.24}$$

$$P_1(T) = P1*(1+T_{CP1}*(T-T_c)) \tag{4.25}$$

wherein I_{PK0} and V_{pkm} are respectively the drain-source current and the gate-source voltage at the peak value of the transconductance, α is the saturation parameter, λ defines the slope of the output characteristics in the saturation region, and P_1, P_2, P_3, T_{CIPK0}, and T_{CP1} are fitting parameters. In eqs. (4.24) and (4.25) T represents the junction temperature which is assumed to be calculated as in eq. (3.5). The complete equations describing this model can be found in [27]. All these parameters are identified on the basis of low-frequency active load-pull

measurements performed at a fixed bias condition (V_{GS0} = -2 V and V_{DS0} = 20 V). The excitations frequency is selected above the cut-off frequency of the dispersive phenomena (see Chapter 3) and the constant junction temperature is determined by the power efficiency associated to each experimental load-line. The model parameters are extracted again through numerical optimization starting from low-frequency measurements performed at 2 MHz by actively sweeping the load impedance in the range illustrated in Figure 4-7. The dissipated power associated to each load line ranges from about 3.5 W (index 10) to about 1.7 W (index 9). This way the junction temperature is varied as well and one can benefit of a better fit of the thermal parameters.

Within the optimization process, the resistive parasitics R_S and R_D are tuned as well and using as starting values the ones obtained from the extraction based on the 'cold' measurements. For the considered device these values are 1 Ω for R_S and 1.7 Ω for R_D. Also, the range of variation of these values is bounded during the optimization process. It is noteworthy that, since R_S and R_D are in series in the considered low-frequency model, the knowledge of an initial estimate is necessary to achieve a consistent estimation of their value. Otherwise it is difficult to distinguish their individual contribution by simply performing standard optimization [28].

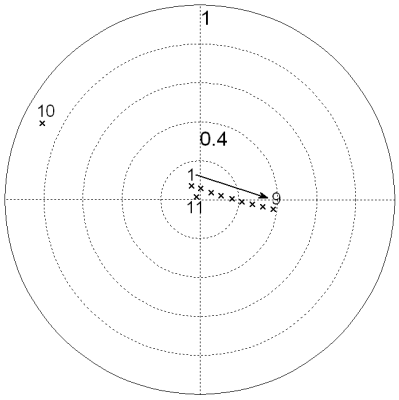

Figure 4-7 Measured output reflection coefficient for the load-lines used for the LF based optimization at f_0 = 2 MHz.

The parameters of the I-V model extracted at V_{GS0} = -2 V, V_{DS0} = 20 V, and f_0 = 2 MHz are reported in Table 4-IV and the simulations of this model are compared with the LF measurements in Figures 4-8 and 4-9. Good level of agreement is achieved both in time and frequency domain.

Table 4-IV Parameters of the nonlinear I-V model of the considered AlGaN/GaN HEMT at V_{GS0} = -2 V, V_{DS0} = 20 V, and f_0 = 2 MHz.

IPK0(A)	P1	P_2	P_3	V_{pks}(V)	D_{vpks}(V)	λ
0.497	0.229	-0.031	0.031	-0.29	0.049	0.008
α_S	α_R	B_1	B_2	T_{cipk0}	T_{cp1}	R_S = 1.4 Ω
0.29	0.02	0.05	1.4	-0.01	0.016	R_D = 2.3 Ω

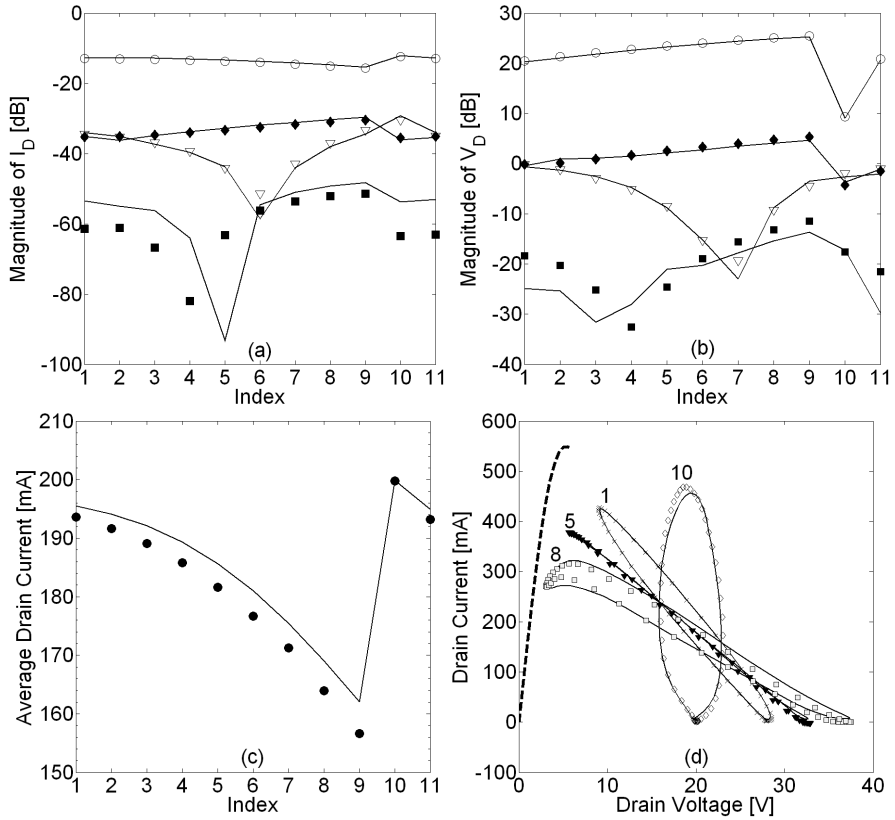

Figure 4-8 Measurements (symbols) and simulations (line) after the numerical optimization at V_{GS0} = -2 V, V_{DS0} = 20 V, f_0 = 2 MHz. (a)-(b) Frequency spectra of the drain current and voltage at f_0 (circles), $2f_0$ (diamonds), $3f_0$ (triangles), $4f_0$ (squares); (c) average drain current; (d) load-lines and DC output characteristic I_{DS}-V_{DS} (dashed line) at V_{GS0} = 0 V. Indices from 1 to 11 are the same of Figure 4-7.

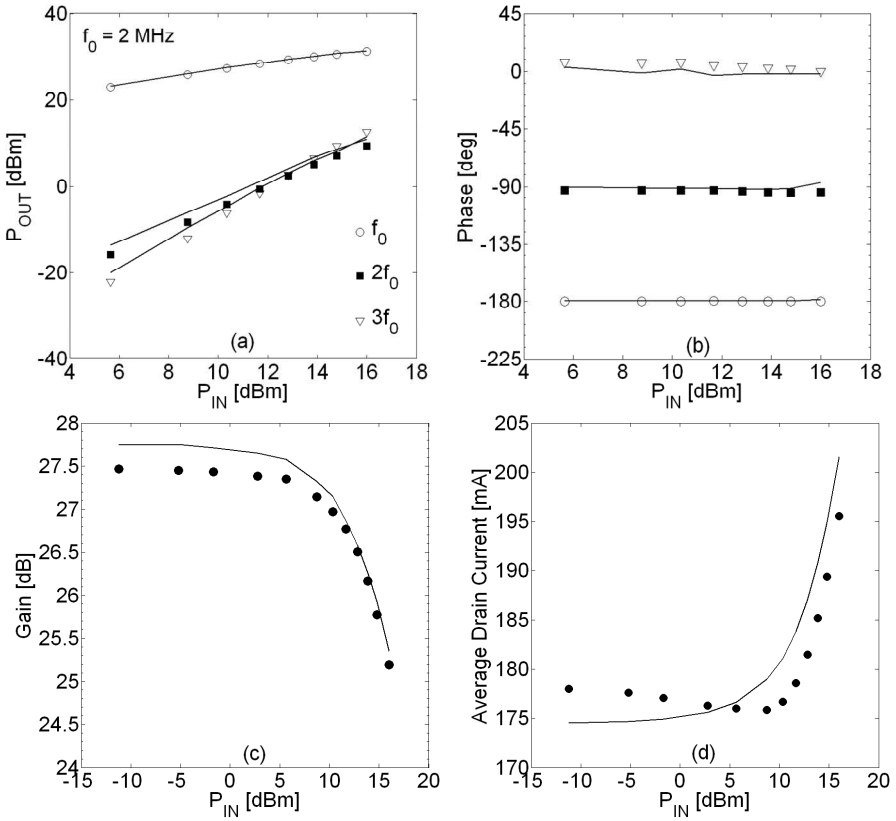

Figure 4-9 Measurements (symbols) and simulations (line) at f_0 = 2 MHz, V_{GS0} = -2 V, V_{DS0} = 20 V, and $Z_L(f_0)$ = 50 Ω. (a) Output power spectrum; (b) output phase response; (c) gain; (d) average drain current. In (b) the relative phase at $2f_0$ is shifted of 90 degrees for visualization purposes.

Differently from the formulation in eqs. (4.18)-(4.20) [17], the parameters of the expression in eqs. (4.21)-(4.25) strictly approximate the dynamic drain-source current at the selected bias condition of the measurements. When the latter is changed, the parameters (Table 4-IV) should be re-extracted for the new quiescent point. Nevertheless, the approach here described is primarily oriented for the modeling of devices employed for the design of power amplifiers. Commonly, such design is carried out at a fixed drain bias condition and the gate bias is set to select the power amplifier class of operation. As a consequence the approach presented here is suitable for this case. Basically it is here assumed that the state of traps is determined only by the quiescent condition. It is important to observe that in general the traps occupation state depends also on the thermal state. The latter is set by the RF operation and, therefore, different for each load-line. Certainly, the

assumption of fixed bias operation may constitute a limitation for the proposed approach. On the other hand, such an assumption allows one to keep a simple model formulation and with a reduced number of parameters which still provide acceptable accuracy, as shown in the obtained results. Differently, if the thermal dependence of the traps state has to be also included, a physics-based model definitely would represent the most suitable solution.

In Figure 4-10 the model is tested at different values of the quiescent gate voltage, with V_{DS0} = 20 V and f_0 = 2 MHz.

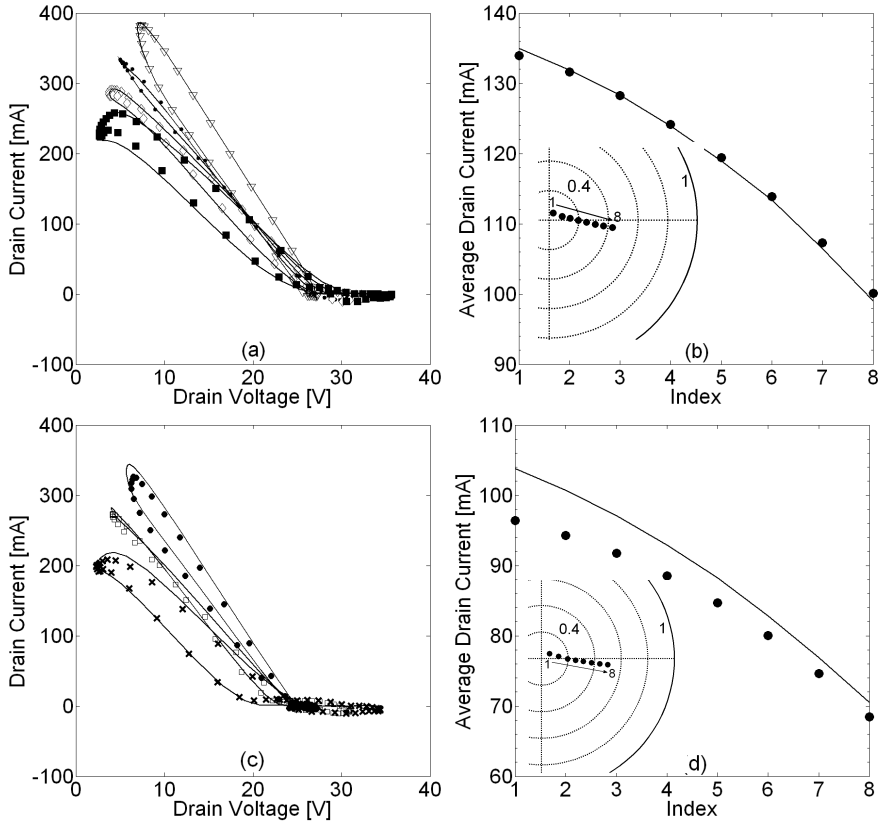

Figure 4-10 Measured (symbols) and simulations (line) of the AlGaN/GaN HEMT at f_0 = 2 MHz: (a)-(b) V_{GS0} = -3 V, V_{DS0} = 20 V; (c)-(d) V_{GS0} = -4 V, V_{DS0} = 20 V. In the inset in (b) and (d) the measured output reflection coefficient corresponding to the 'index' on the x-axis.

As previously said, the model parameters are strictly valid for a fixed quiescent condition. When this is changed, the traps' state is modified as well. Nevertheless, for the considered transistor, the I-V model extracted at V_{GS0} = -2 V and V_{DS0} =

20 V yields good predictions also if the quiescent voltage is changed as in Figure 4-10 (V_{GS0} = -3 V and V_{GS0} = -4 V).

Next, the quiescent drain-source voltage V_{DS0} is increased and a set of load-pull measurements are acquired. In Figure 4-11 the I-V model with the parameters in Table 4-IV is simulated at V_{GS0} = -2 V and V_{DS0} = 30 V. Comparison between model predictions and experiments is depicted in Figure 4-11.

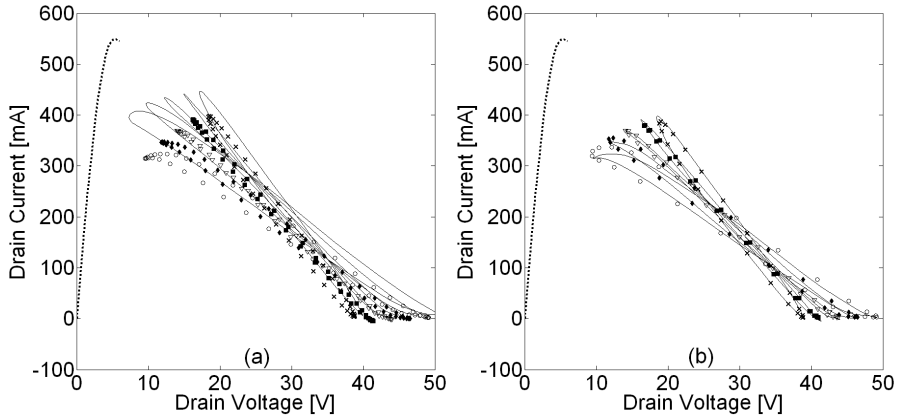

Figure 4-11 Measurements (symbols) and simulations (line) at f_0 = 2 MHz, V_{GS0} = -2 V and V_{DS0} = 30 V. (a) Simulation of the model of Table 4-IV and (b) simulation of the model in Table 4-V. Static I_{DS}-V_{DS} characteristic at V_{GS0} = 0 V (dotted line).

Evidently, the measured load-lines display a significant knee walk out and change of the slope in the linear region as compared with the simulated load-lines obtained from the model extracted at V_{GS0} = -2 V and V_{DS0} = 30 V. This is in agreement with the experimental observations in [18] and [29]. In fact, unless the transistor is driven in the strong pinch-off region, dispersive effects, such as the knee walkout, are more significant when the value of V_{DS0} is increased. In [17], such behavior is accounted for in the formulation of the model which is moreover identified from low-frequency load-lines measured at different bias points. In this work, instead, the parameters are re-optimized at the new quiescent condition. In fact, some of the parameters of the expressions in eqs. (4.21)-(4.25), such as IPK0, α_S, and α_R are directly linked to the dynamic response in the linear and knee region. The new model parameters are reported in Table 4-V.

Table 4-V Parameters of the nonlinear I-V model of the considered AlGaN/GaN HEMT at V_{GS0} = -2 V, V_{DS0} = 30 V, and f_0 = 2 MHz.

IPK0(A)	P1	P_2	P_3	V_{pks}(V)	D_{vpks}(V)	λ
0.410	0.226	-0.024	0.031	-0.34	0.025	0.0078
α_S	α_R	B_1	B_2	T_{cipk0}	T_{cp1}	R_S = 1.4 Ω
0.17	**0.002**	1.3	0.8	-0.01	0.016	R_D = 2.3 Ω

4.5 Modeling of the I-V and Q-V functions

4.5.1 Combined low- and high-frequency large-signal identification

In this section low- and high-frequency large-signal measurements are exploited to identify all the parts of the network in Figure 4-3. The model parameters identification is carried out into two steps. Firstly, the I-V model, R_S, and R_D are identified starting from a set of low-frequency active load pull measurements, as in Section 4.4.2. The I_{DS} source is replaced with temperature dependent expressions of the Angelov model [26]. Nevertheless, this choice is not restrictive and it is only conveniently made as this model is available in the circuit simulator. The gate resistance R_G is neglected in this step as the Schottky junction is not driven in forward conduction or in the breakdown region within the swing of the low-frequency waveforms. Therefore, at few megahertz R_G is in series with an ideal open circuit. Once I_{DS}, R_D, and R_S are known, a second optimization step is performed starting from another set of large-signal current and voltage waveforms. The latter are measured at the same bias condition as the LF experiments. The value of the fundamental frequency is instead increased up to the RF range and, consequently, the contribution of the linear and nonlinear reactive parts is boosted. Within the second optimization step only the charge sources parameters, C_{DS}, R_G, L_G, L_S, and L_D are unknown. I_{DS}, R_D, and R_S are known from the previous step and are assumed to be independent on the operating frequency. It has been mentioned already that the separation of the model parameters into two sets undoubtedly assures shorter optimization times and reduces model parameter uncertainty. An accurate fit of the RF experiments is achieved and, at the same time, also the voltage and current waveforms at the I_{DS} plane are correctly modeled. The modeling procedure is schematically illustrated in Figure 4-12 and it is applied for

the extraction of the nonlinear model of a 0.7x800 μm^2 AlGaN/GaN HEMT and a 0.25x400 μm^2 GaAs pHEMT.

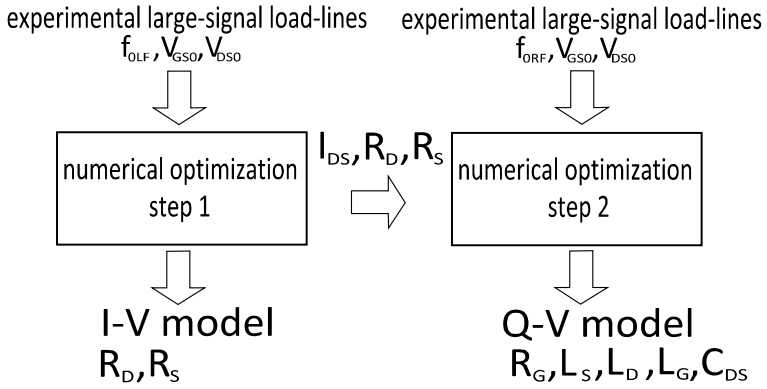

Figure 4-12 Two-step nonlinear model identification.

4.5.2 GaN HEMT and GaAs pHEMT modeling

As regarding the GaN based device, the LF and the RF load-lines are measured at f0 = 2 MHz and f0 = 4 GHz respectively (Figure 4-13). The bias point is fixed at V_{GS0} = -2 V and V_{DS0} = 20 V.

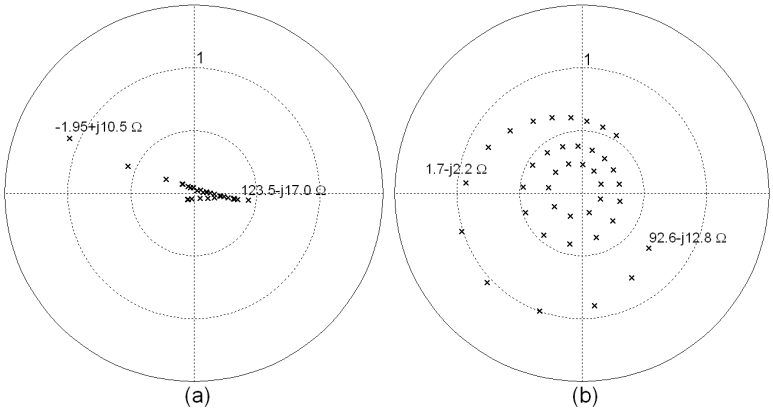

Figure 4-13 Output reflection coefficient associated with the load lines measured at the probe tips and used for the numerical optimization at (a) f_0 = 2 MHz and (b) f_0 = 4 GHz.

The measured voltage and current waveforms at the extrinsic plane and the ones simulated after numerical optimization show a good agreement in Figure 4-14 for various loading and power conditions.

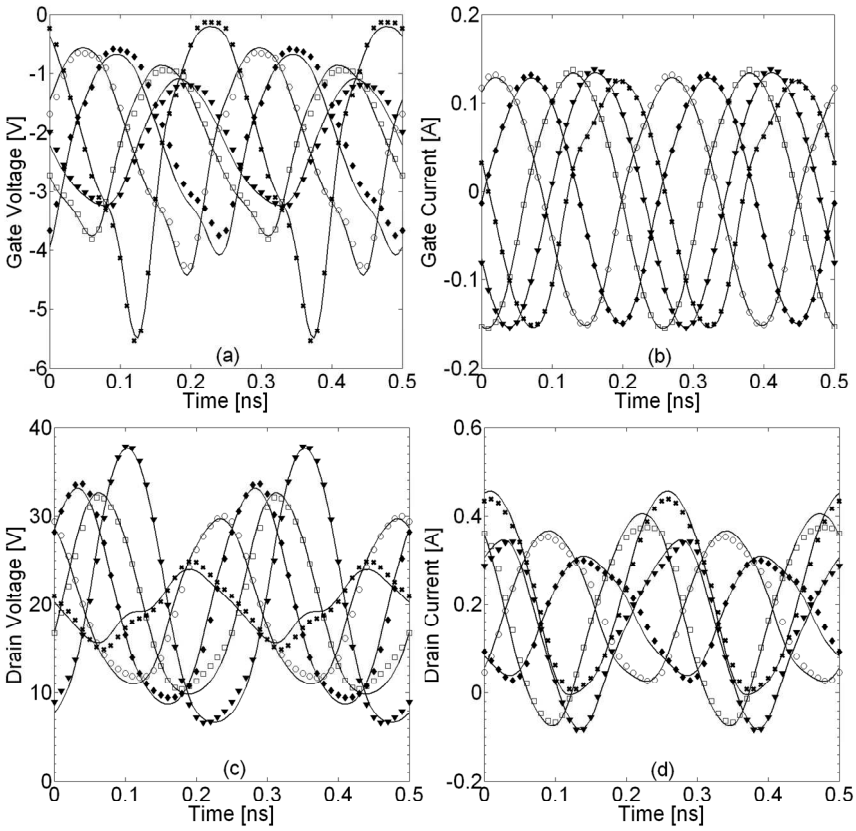

Figure 4-14 Measurements (symbols) and simulations after optimization (line) at different loading conditions and power levels at f_0 = 4 GHz, V_{GS0} = -2 V, V_{DS0} = 20 V: $Z_L(f_0)$ = 53.6-j16.7 Ω, $P_{OUT}(f_0)$ ~ 0.75 W (circle); $Z_L(f_0)$ = 92.6-j12.8 Ω, $P_{OUT}(f_0)$ = 0.83 W (diamond); Z_L (f_0) = 35.6+j31.1 Ω, P_{OUT} (f_0) ~ 0.94 W (square); $Z_L(f_0)$ = -1.1-j19.8 Ω, $P_{OUT}(f_0)$ ~ 0 W (cross); $Z_L(f_0)$ = 48.2-j62.7 Ω, $P_{OUT}(f_0)$ ~ 1 W (triangle). (a) Gate voltage waveforms; (b) gate current waveforms; (c) drain voltage waveforms; (d) drain current waveforms.

As further validation, measurements and simulation performed at the same bias point as before, at f_0 = 2 GHz, and load impedance equal to 50 Ω are compared in Figure 4-15 for different values of input power.

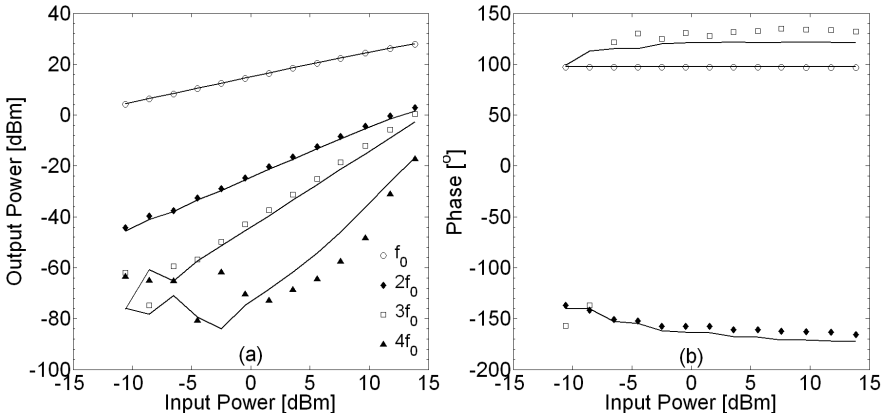

Figure 4-15 Measured (symbols) and simulated (lines) (a) output power and (b) phase response at the fundamental and harmonic frequencies: f_0 = 2 GHz, V_{GS0} = -2 V, V_{DS0} = 20 V, and $Z_L(f_0)$ = 50 Ω. The scattered points at low levels of the input power fall within the measurement noise. In (b) the relative phase of the 4th harmonic frequency is not shown as the measured power level at $4f_0$ falls at the edge of the dynamic range.

Also in this case model predictions yield good agreement with the experiments. In Figure 4-16 the i_G-v_G and i_G-v_D time-domain trajectories are illustrated as function of the input power.

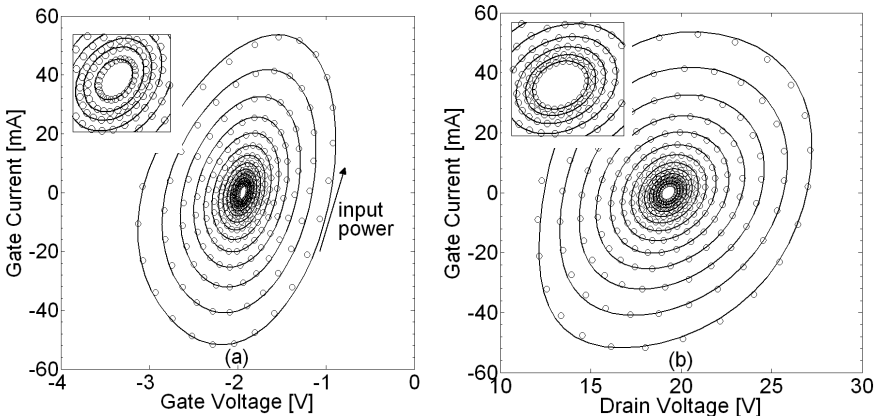

Figure 4-16 Measured (symbols) and simulated (lines) (a) i_G-v_G and (b) i_G-v_D trajectories of the AlGaN/GaN HEMT at: f_0 = 2 GHz, V_{GS0} = -2 V, V_{DS0} = 20 V, and $Z_L(f_0)$ = 50 Ω. In the inset the trajectories at low levels of input power are shown.

Since the intrinsic displacement gate current mainly originates from only the nonlinear charge sources, the agreement between the simulated and measured trajectories confirms that the Q-V functions are correctly modeled. Along with the

estimation of the I-V and Q-V model parameters also the values of the parasitic elements are tuned within the numerical optimization. The tuned values after the optimization are compared in Table 4-VI with the ones extracted from the well-established 'cold FET' technique [2].

Table 4-VI Value of parasitic elements as obtained after the optimization (top row) and from the 'cold FET' extraction (bottom row).

R_G (Ω)	L_G(pH)	R_S(Ω)	R_D (Ω)	L_S (pH)	L_D(pH)	C_{pg}(fF)	C_{pd}(fF)
5.4	130	0.8	1.7	3.1	103	29	29
5.6	*146*	*1.1*	*2.7*	*3.5*	*125*	*30*	*30*

In case of the GaAs based transistor, the frequency of the LF measurements is set equal to 2 MHz whereas the RF frequency to 8 GHz. The quiescent condition is set at V_{GS0} = -0.5 V and V_{DS0} = 6 V. In total 34 load lines are exploited for the identification of the I-V and Q-V model's parameters. As shown in Figure 4-17, the experimental low- and high-frequency waveforms agree quite well with the simulated ones after numerical optimization.

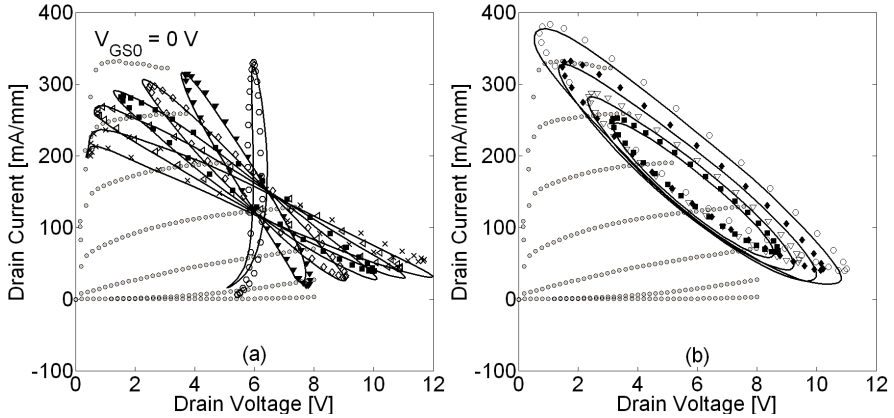

Figure 4-17 Measurements (symbols) and simulation (lines) of the GaAs pHEMT at (a) f_0 = 2 MHz and different load impedances and (b) f_0 = 8 GHz and different power levels. I_{DS}-V_{DS} static characteristics are shown in (a)-(b).

In order to further validate the identified large-signal model, simulation at 4 GHz and for different values of V_{GS0} and V_{DS0} = 6 V are performed. Comparison with measurements are reported in Figure 4-18. From this plot it emerges that the dynamic characteristics of the modeled device manifest no dependence on the quiescent gate voltage V_{GS0} and, therefore, it yields accurate predictions over a

broad range of operating conditions, although the extraction is performed with a small set of experimental time-domain waveforms.

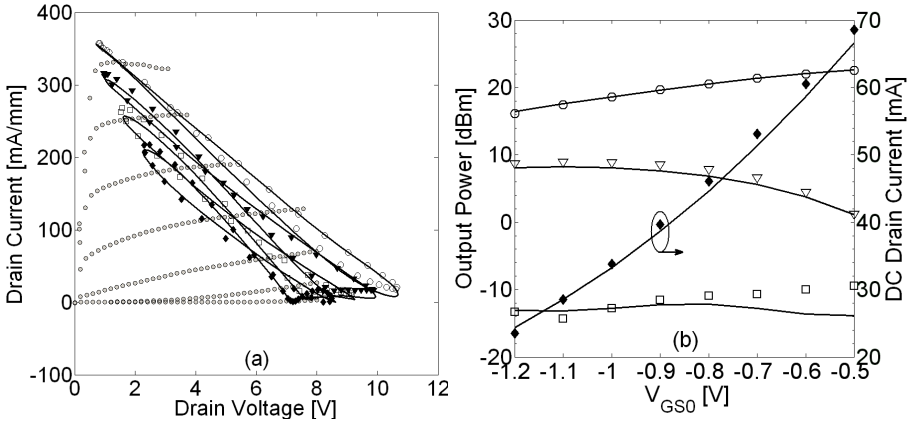

Figure 4-18 Measurements (symbols) and simulations (lines) at f_0 = 4 GHz and $P_{IN,av}$ = 6.2 dBm for the investigated GaAs pHEMT. (a) Load lines at V_{GS0} = -1.2 V (diamonds), -0.9 V (squares), -0.7 V (triangles), -0.5 V (circles); (b) output power at f_0 (circles), $2f_0$ (triangles), $3f_0$ (squares), and average drain current (diamonds) against V_{GS0}.

4.6 Conclusions

In this Chapter measurement-based techniques aimed at the identification of linear and nonlinear models of transistors are described. In the first part of the Chapter the applicability of an existing macromodeling technique for the bias-dependent linear microwave modelling of silicon based FET is investigated. It is demonstrated that the macromodeling approach developed by the INTEC group of the University of Ghent and originally aimed at the modelling of high-frequency passive structures can be successfully exploited for active devices and readily implemented in a commercial circuit simulator.

As regarding the extraction of nonlinear models, the Chapter focuses on the use of large-signal measurements to directly estimate the model parameters. In literature, approaches which separately exploit either low- or high-frequency large signal measurements are reported. In this work, large-signal measurements carried out in the low- (<30 MHz) and high- (>600 MHz) frequency ranges are combined together. More precisely, the low-frequency experiments are exploited to identify the nonlinear I-V functions. The high-frequency measurements are instead used to estimate the parameters of the nonlinear Q-V functions. In addition, also the linear

parasitic elements of the model are tuned within the optimization routine in order to improve the fitting between the experimental and simulated current and voltage waveforms under large-signal conditions. The advantage of the proposed approach is threefold: firstly and commonly to other large-signal based approaches, nonlinear models can be extracted with a reduced numbers of experiments as compared, for instance, with the case of models extracted from multi-bias small-signal measurements. Secondly, the large-signal operation drives transistors under realistic conditions. Finally and importantly the parameters identification is split into two steps. Therefore the numerical procedure for the parameters' estimation is significantly simplified due to the reduced number of parameters to be determined in each step. This procedure is independent on the device technology and it is applied in this work to extract nonlinear models of GaN and GaAs based transistors for the simulation and design of nonlinear circuits. It is shown that accurate and dedicated nonlinear models can be obtained starting from a small set of nonlinear measurements.

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Chapter 5

Nonlinear de-embedding of transistor waveforms

5.1 Motivations

This Chapter focuses on the description of embedding and de-embedding techniques to determine the intrinsic nonlinear I-V relationships of active devices. In Chapter 4 modeling approaches have been described to identify the intrinsic I-V characteristics on the basis of small- and large-signal vectorial measurements. Conversely, the embedding and de-embedding techniques described in this Chapter allow one to obtain the intrinsic I-V response without the need to identify an electro-thermal model of the output current source of active devices. This is a significant advantage especially when dealing with III-V compounds based devices which may be strongly affected by low-frequency dispersive phenomena whose modeling is not a trivial task. It is noteworthy that the knowledge of the actual I-V waveforms is crucial to apply waveform engineering [1], which has strongly entered power amplifier design in the last years. The interest of RF and microwave researchers and designers in looking at the current and voltage waveforms has significantly risen with the increasing availability of RF vector calibrated measurement systems. Designers are mainly interested in obtaining the maximum RF output power while maximizing the efficiency over a specific application frequency band. To this aim, waveform engineering constitutes a very powerful approach by which the source and load impedances at active device terminals are properly tuned to obtain the desired waveforms shape which corresponds to a specific RF operating condition. Moreover, the availability of the waveforms allows one to monitor the interaction between the waveforms themselves and the active device extreme operating regions, such as the knee and the breakdown region which directly affect the deliverable output power. Waveforms-based power amplifier design is reported in [2]-[7] and still represents a challenging task especially when the required output power and operating frequency are pushed up.

All the theoretical aspects of waveform engineering can be derived by Cripps load line theory [8]. The latter basically defines all the PA operating modes at the current generator plane where the optimal shapes of the voltage and current waveforms have to be synthesized. As a consequence, the dynamic I-V characteristics must be accurately known to achieve an accurate waveforms control. In fact, when the I-V relationships are measured in the RF and microwave range, the actual waveforms at the current generator plane are not directly visible as they are significantly masked by the presence of the parasitic elements and by the reactive nonlinearities. Additionally and importantly, the static (DC) I-V characteristics are definitely inadequate to describe I-V dynamics when low-frequency dispersion is significant [9], [10]. Therefore, the dynamic I-V characteristics at the actual device plane can directly provide information on dispersive phenomena which strongly impair transistor behavior under RF operation. In this Chapter, the de-embedding/embedding methods are firstly outlined. Next, examples to demonstrate the capability of the proposed approaches are discussed. The main outcomes of this activity have been published in [11], [12], and [13].

5.2 Proposed approach

As reference for what follows, in Figure 5-1 a simplified HF circuit topology of a FET is illustrated. All over the text and in the reported plots, ‘drain voltage’ and ‘gate voltage’ are referred to the common source terminal. In Figure 5-1, the voltages and the currents at three planes are highlighted: the external plane (EP) corresponds to the calibration or measurement plane which, for on wafer devices, is at the probes tip; the intrinsic plane (IP), which delimits the semiconductor active area and, finally, the current generator plane (CGP). Furthermore, the section encompassed by the IP is split into a resistive core [9], which accounts for the current sources, and a capacitive core, which describes the transistor nonlinear capacitances. As common for semiconductors, the resistive and capacitive cores are strictly in parallel and their electrical response is a function of the total instantaneous voltages present at the IP terminals. For convenience, the electrical quantities of the resistive and capacitive core are indicated with the ‘R’ and ‘C’ superscript respectively. Clearly, the higher is the value of the measurement frequency the more significant is the contribution of the reactive nonlinearities and the reactive parasitic elements. Note that in Figure 5-1 the nonlinear capacitances between the gate-source and gate-drain terminals are replaced by nonlinear voltage controlled charge sources.

The embedding and de-embedding procedures consist of shifting the measured current and voltage waveforms from the intrinsic to the extrinsic plane (embedding) and vice versa (de-embedding). More precisely, in this work the embedding is applied to LF vector-calibrated measurements whereas the de-embedding is applied to RF vector-calibrated measurements. Nonlinear embedding has been reported for the first time in [4] whereas a full nonlinear de-embedding procedure is described for the first time in [11]-[13]. Both procedures enable to obtain the actual current and voltage waveforms at the CGP and the corresponding RF current and voltage waveforms at the EP, without the need of a nonlinear model of the current source I_{DS} and with the sole knowledge of the Q-V functions and the values of the parasitic elements. The latter can be identified as explained in Chapter 4. The embedding and the de-embedding methods applied to the current and voltage waveforms of active devices are outlined step-by-step in what follows.

5.2.1 Nonlinear de-embedding

The results obtained in this part of the work are summarized in the following publications

- A. Raffo, G. Avolio, D. M. M.-P. Schreurs, S. Di Falco, V. Vadalà, F. Scappaviva, G. Crupi, B. Nauwelaers, and G. Vannini, "On the evaluation of the high-frequency load line in active devices," *International Journal of Microwave and Wireless Technology.*, vol. 3, no. 1, pp. 19-24, Jan. 2011,
- G. Avolio, D. Schreurs, A. Raffo, G. Crupi, G. Vannini, and B. Nauwelaers, "A de-embedding procedure oriented to the determination of FET intrinsic I-V characteristics from high-frequency large-signal measurements," *76th Automatic RF Techniques Group Conference (ARFTG),* pp. 1-6, Clearwater Beach, Florida, Dec. 2010,
- G. Avolio, D. Schreurs, A. Raffo, G. Crupi, G. Vannini, and B. Nauwelaers, "Waveforms-only based nonlinear de-embedding in active devices," *IEEE Microwave and Wireless Components Letters*, vol. 22, no.4, pp. 215-217, April 2012.
- G. Avolio, A. Raffo, D. Schreurs, G. Vannini, and B. Nauwelaers, "Nonlinear de-embedding of microwave large-signal measurements," accepted for oral presentation at the *Automatic RF Techniques Group Conference (ARFTG)*, Montreal, Canada, June 2012.

With no loss of generality, the de-embedding method here proposed refers to the network in Figure 5-1 and consists of three steps:

(I) the vector-calibrated RF I-V measurements are shifted from the EP to the IP;

(II) the voltages at the IP, obtained from step 1), are used to calculate the intrinsic displacement current associated with the nonlinear capacitances;

(III) the intrinsic displacement current vectors obtained in step 2) are subtracted from the vectors of the total intrinsic current determined after step 1).

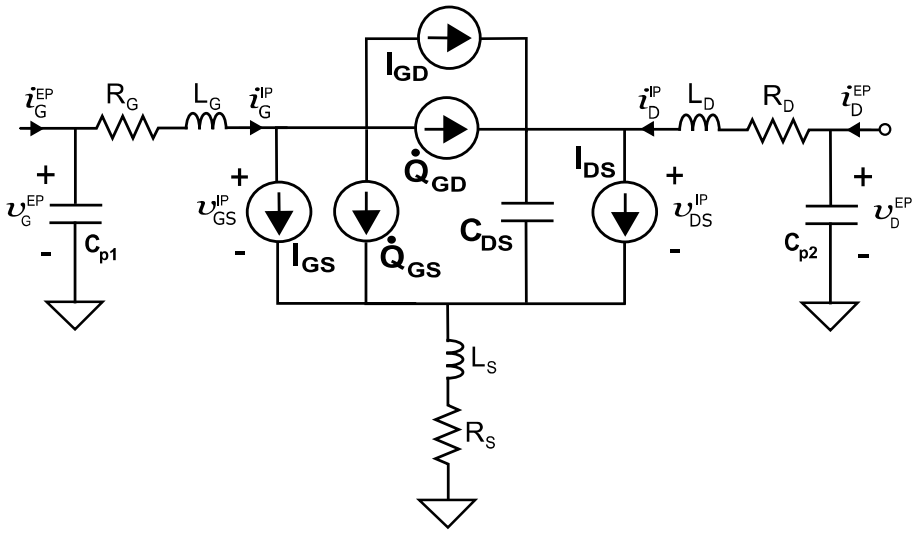

Figure 5-1 High-frequency large-signal equivalent circuit of a FET in common source configuration.

The first step consists of shifting the measured frequency spectra at the extrinsic planes up to the intrinsic ones, which implies an accurate description of the parasitic elements. Commonly, parasitic elements extraction is accomplished through S-parameter measurements by exploiting either lumped parameters approximation, as for example in [14], or, alternatively, by adopting electro-magnetic simulations of the device layout as in [15]. Once the values of parasitic elements are known, the phasors of the voltages and currents at the IP are obtained by applying a linear transformation in frequency domain, as expressed in eq. (5.1):

$$\begin{bmatrix} V_{GS}^{IP}(kf_0) \\ I_G^{IP}(kf_0) \\ V_{DS}^{IP}(kf_0) \\ I_D^{IP}(kf_0) \end{bmatrix}_{k=-N...N} = M(kf_0) \begin{bmatrix} V_G^{EP}(kf_0) \\ I_G^{EP}(kf_0) \\ V_D^{EP}(kf_0) \\ I_D^{EP}(kf_0) \end{bmatrix}_{k=-N...N} \tag{5.1}$$

where $\underline{\underline{M}}$ is a four-by-four matrix which describes the four-port parasitic elements network at the fundamental and harmonic frequencies (kf_0). The elements of $\underline{\underline{M}}$ are derived starting from the Y-parameter matrix representing the four-port network illustrated in Figure 5-2.

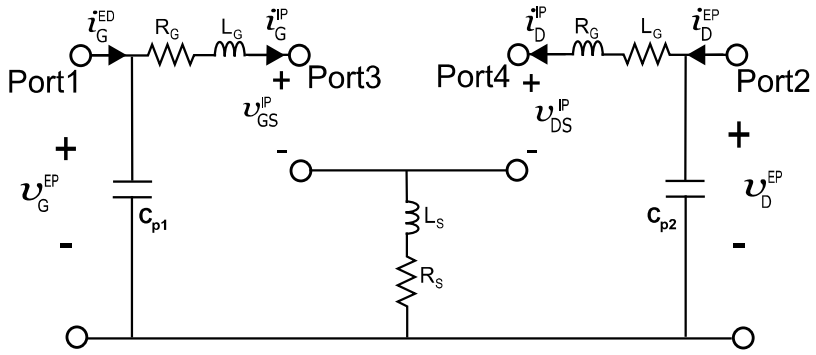

Figure 5-2 Four-port representation of the parasitic network

For the network in Figure 5-2 the following equation can be written:

$$\begin{bmatrix} I_G^{EP}(kf_0) \\ I_D^{EP}(kf_0) \\ -I_G^{IP}(kf_0) \\ -I_D^{IP}(kf_0) \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} (kf_0) \begin{bmatrix} V_G^{EP}(kf_0) \\ V_D^{EP}(kf_0) \\ V_{GS}^{IP}(kf_0) \\ V_{DS}^{IP}(kf_0) \end{bmatrix} \tag{5.2}$$

wherein the electrical quantities at the extrinsic planes are known from the measurements and the Y-parameters are calculated, from the known parasitic elements, at each point of the frequency grid of the measurements. Therefore, the voltages and currents at the intrinsic plane are obtained by simple algebraic manipulation of eq. (5.2).

The second step of the procedure consists of separating the intrinsic displacement current component from the intrinsic resistive one. In fact, due to the presence of the capacitive core, the knowledge of the only electrical quantities at the IP does not allow one to correctly evaluate the currents at the CGP and, consequently, the actual I-V waveforms. The de-embedding of the parasitic elements can give just a qualitative indication of the shape of the load line at the resistive core, which is acceptably closer to the actual one only when the capacitive core contribution can be neglected, which is the case of low-frequency operation [16]. In addition, in some cases it is not sufficient to include only the contribution of the output capacitance (C_{DS}) [17], as also the effect of gate-drain capacitance (C_{GD}) has to be accounted for when the RF frequency is boosted. Strictly speaking, it is necessary to identify the displacement current contribution and to this aim the reactive nonlinearities can be identified either by adopting standard multi-bias S-parameter measurements [9], [18], and [19] or directly from large-signal measurements, as for instance in [20]. This second case will be treated in Section 5.5. When the bias-dependent capacitances are known and under the hypothesis of negligible non-quasi-static (NQS) effects, the intrinsic displacement currents can be expressed as:

$$\begin{bmatrix} i_G^{IP,C}(t) \\ i_D^{IP,C}(t) \end{bmatrix} = \sum_{k=-N}^{N} j2\pi kf_0 \underline{\underline{C}}(v_{GS}^{IP}(t), v_{DS}^{IP}(t)) \begin{bmatrix} V_{GS}^{IP}(kf_0) * e^{j2\pi kf_0 t} \\ V_{DS}^{IP}(kf_0) * e^{j2\pi kf_0 t} \end{bmatrix} \tag{5.3}$$

or, when a charge based formulation is adopted, as:

$$i_G^{IP,C}(t) = \dot{Q}_{GS}(v_{GS}^{IP}(t), v_{DS}^{IP}(t)) \tag{5.4}$$

$$i_D^{IP,C}(t) = \dot{Q}_{DS}(v_{GS}^{IP}(t), v_{DS}^{IP}(t)) \tag{5.5}$$

Note that the assumption of negligible NQS effects can be straightforwardly removed, without impairing the proposed de-embedding method. NQS effects are commonly accounted for by adding in the transistor model the resistors R_{gd} and R_{gs}, as outlined in [21]. In this case when calculating the intrinsic voltages, one has to remove also the contributions of R_{gd} and R_{gs} and eq. (5.3) can be still applied. Clearly other methods can be adopted to include NQS effects but this has no implications on the proposed technique.

In eq. (5.3), $\underline{\underline{C}}$ represents the matrix of the nonlinear capacitances. In eqs. (5.4) and (5.5), Q_{GS} and Q_{DS} describe the nonlinear charge sources between the input and output terminals at the intrinsic plane. The displacement currents can be calculated

either directly from eq. (5.3) or, alternatively, by exploiting a harmonic balance solver.

The currents at the IP, which are obtained after step 1), can be expressed as the vector sum of a resistive and displacement component, as in eq. (5.6):

$$\begin{bmatrix} I_G^{IP}(kf_0) \\ I_D^{IP}(kf_0) \end{bmatrix}_{k=-N...N} = \begin{bmatrix} I_G^{IP,R}(kf_0) + I_G^{IP,C}(kf_0) \\ I_D^{IP,R}(kf_0) + I_D^{IP,C}(kf_0) \end{bmatrix}_{k=-N...N} \tag{5.6}$$

More explicitly and in time-domain, for the currents at the intrinsic plane the following equations can be written (see Chapter 4):

$$i_G^{IP}(t)=f_G(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X(t),T(t)) + \dot{Q}_{GS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X(t),T(t)) \tag{5.7}$$

$$i_D^{IP}(t)=f_D(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X(t),T(t)) + \dot{Q}_{DS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X(t),T(t)) \tag{5.8}$$

The dependence on the variable X(t) and T(t) accounts for the dependence of the instantaneous intrinsic current on both the electrical state of the traps and the thermal effects. Actually, for all the examples here reported, eqs. (5.7) and (5.8) turn into

$$i_G^{IP}(t)=f_G(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) + \dot{Q}_{GS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) \tag{5.9}$$

$$i_D^{IP}(t)=f_D(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) + \dot{Q}_{DS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) \tag{5.10}$$

in which both the traps' state and the temperature are assumed in the steady state, as they cannot follow the fast variations of the exciting signals. The average traps state X_0 is assumed to be dependent on the average values of the intrinsic gate and drain voltage waveforms and on the temperature; the average junction temperature T_0 is set by the dynamic load line, which determines the power dissipated at the intrinsic transistor terminals. Eqs. (5.9) and (5.10) can be further simplified to eqs. (5.11) and (5.12) as the intrinsic displacement component of the current is dependent only on the instantaneous intrinsic voltages, regardless the traps and the thermal state.

$$i_G^{IP}(t)=f_G(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) + \dot{Q}_{GS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t)) \tag{5.11}$$

$$i_D^{IP}(t)=f_D(v_{GS}^{IP}(t),v_{DS}^{IP}(t),X_0,T_0) + \dot{Q}_{DS}(v_{GS}^{IP}(t),v_{DS}^{IP}(t)) \tag{5.12}$$

In step 3), the intrinsic resistive currents are computed by subtraction of the vector of the intrinsic displacement currents calculated in step 2) from the vector of the currents at the intrinsic plane.

As can be deduced from steps 1)-3), the proposed de-embedding requires that only the parasitic networks and the nonlinear capacitances or terminal charges have to be accurately known. Thus, no a priori knowledge of the I-V characteristics ('f_G' and 'f_D' in eqs. (5.7) and (5.8)) is needed which is an advantage from a modeling point of view. As clear from eqs. (5.7)-(5.10), the modeling of the intrinsic resistive currents, which are strongly affected by LF dispersion, might not constitute an easy task as complex phenomena such as charge trapping and thermal effects must be accounted for. When steps 1)-3) are applied instead, the RF I-V at the CGP, including dispersive effects, can be straightforwardly obtained for any load-line measured at the EP, under the commonly adopted assumption of negligible dispersion of the intrinsic displacement currents. Moreover, after steps 1)-3), the impedances synthesized at the CGP are available at the fundamental frequency and the harmonics.

5.2.2 Nonlinear embedding

The concept of nonlinear embedding has been already exploited in [4] for the design of a high-efficiency PA stage. As opposite to the nonlinear de-embedding, the embedding procedure starts from LF I-V measurements [9], [22], [23] and, therefore, the I-V waveforms are firstly experimentally determined, and not modeled, at the CGP under low-frequency excitations. In fact, any reactive effect either related to the active device itself or due to the parasitic elements can be neglected in the MHz range. Next, the intrinsic voltages at the CGP terminals are mathematically shifted up to the RF frequency f_{0RF}, as in eqs. (5.13) and (5.14):

$$v_{GS}^{IP}(t) = \sum_{k=N...N} V_{GS}^{IP}(kf_{0LF}) * e^{j*2\pi kf_{0RF}t} \tag{5.13}$$

$$v_{DS}^{IP}(t) = \sum_{k=-N...N} V_{DS}^{IP}(kf_{0LF}) * e^{j*2\pi kf_{0RF}t} \tag{5.14}$$

The frequency-shifted intrinsic waveforms are used to excite the known nonlinear capacitive core in order to calculate the intrinsic displacement current at the input and output port. At this point, all the currents and voltages waveforms at the intrinsic terminals of the active device are available and the RF electrical quantities at the extrinsic plane can be straightforwardly determined through the

frequency domain linear transformation in eq. (5.1). Consequently, the impedances to be synthesized at the RF fundamental frequency and the harmonics are known at the extrinsic reference plane for the fixed condition at the CGP. A flowchart of the embedding and de-embedding procedures is illustrated in Figure 5-3.

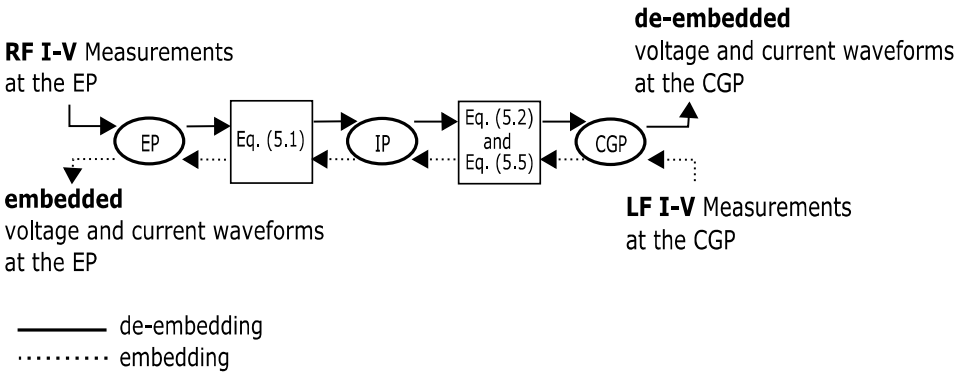

Figure 5-3 Schematic representation of the de-embedding and embedding procedures.

In what follows, examples of nonlinear de-embedding are reported. The nonlinear embedding is instead exploited within the context of this work to demonstrate the nonlinear embedding and de-embedding techniques are actually equivalent and lead to the same result, although they are applied starting from different experimental conditions.

5.2.3 The role of the feedback capacitance C_{GD}

The idea of the full de-embedding of calibrated vector RF nonlinear measurements is clearly not new. However, the novelty of the proposed approach consists of retrieving the dynamic I-V characteristics by considering the full intrinsic capacitive contribution. Often, only the contribution of a constant C_{DS} is de-embedded whereas the contribution of C_{GD} is neglected. Practically, whether or not this approximation is valid depends on the load line at the intrinsic plane, which defines the gate-drain voltage across the C_{GD} and, clearly, on the operating RF frequency. In Figure 5-4, discrepancy exists if C_{GD} is not accounted for. Consequently, the intrinsic displacement current must be properly de-embedded to retrieve the actual I-V characteristic as close as possible to the real one. It is also worthy to stress that the accuracy of the de-embedding strongly depends on how accurate the extraction of the nonlinear capacitances is, which affects the waveforms and impedances at the I_{DS} plane. Despite this, the de-embedding

provides a qualitative insight in the RF I-V waveforms at the CGP, and this information can be successively exploited in the design phase for the impedance tuning to achieve the optimal circuit performance.

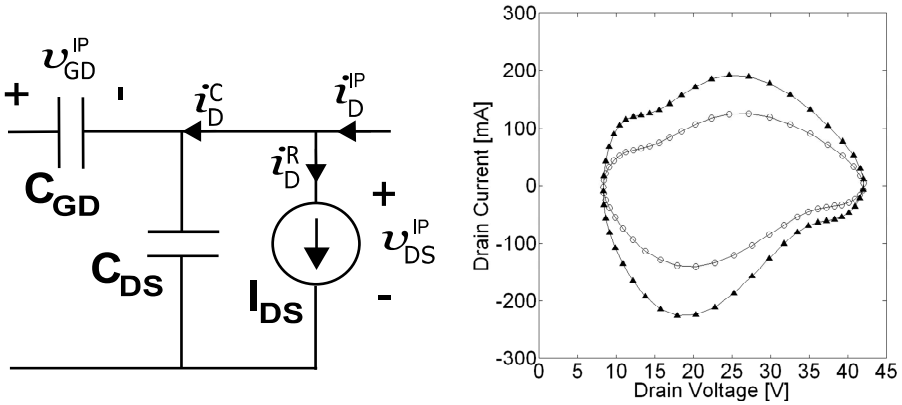

Figure 5-4 Intrinsic equivalent intrinsic circuit at the output port and intrinsic displacement current component of the drain current, calculated as in eq. (5.4) for the load line in Figure 5-9 at f_0 = 4GHz: with only C_{DS} (circles) and with both C_{DS} and C_{GD} (triangles). Both C_{DS} and C_{GD} are extracted by multi-bias S-parameter measurements [9], [18], and [19].

5.3 Examples of nonlinear de-embedding

5.3.1 FinFET

The procedure outlined in Section 5.2.1 is applied to RF I-V measurements of a FinFET. The gate length is L = 60 nm and the width W = 45.6 μm. The device has 50 fingers in total. The RF I-V measurements have been performed at the fundamental frequency of 4 GHz. The parasitics and the nonlinear capacitances (or the equivalent nonlinear charge sources) are extracted from multi-bias S-parameter measurements, as in [9], [18], and [19]. Standard RF single-tone CW power sweep has been performed with an RF LSNA by which the output port is terminated with 50 Ohm load. The measured load lines at f_0 = 4 GHz, V_{GS0} = 0.3 V, and V_{DS0} = 0.9 V are illustrated in Figure 5-5 on top of the measured I_{DS}-V_{DS} DC characteristics at the extrinsic plane.

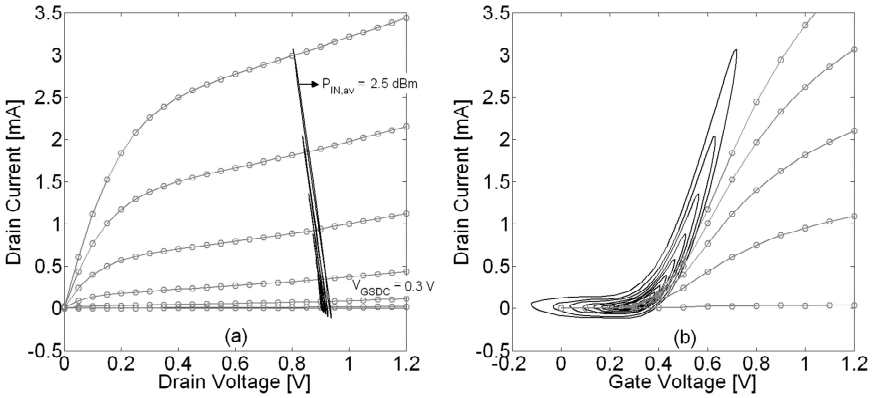

Figure 5-5 Measured load lines (continuous line) of the FinFET at V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz. The input power is swept from -17 to 2.5 dBm. Measured I_{DS}-V_{DS} DC curves at the extrinsic plane (circles).

Due to the 50 Ohm termination, the trajectories in Figure 5-5 do not cross the strong nonlinearities of the output I-V characteristics, though the slight shift of the quiescent point is an indication of nonlinear self-biasing effect. A strong nonlinear behaviour is observed, instead, in the transcharacteristic and the level of the harmonic frequencies of the drain current signal is sufficiently high to test the de-embedding procedure under nonlinear operation.

The de-embedding is applied to the load line corresponding to the highest level of the input power (~ 2.5 dBm). The de-embedded RF load line and transcharacteristic are reported in Figure 5-6. More precisely, the de-embedded transcharacteristic proves the effectiveness of the proposed procedure. In fact, as compared with the measured transcharacteristic at the EP, it shows clipping to zero ampere when the intrinsic gate-source voltage is lower than the threshold voltage, which is approximately equal to 0.35 V for the considered device. Qualitatively, this is an indication that the displacement component of the drain current is properly removed from the intrinsic one.

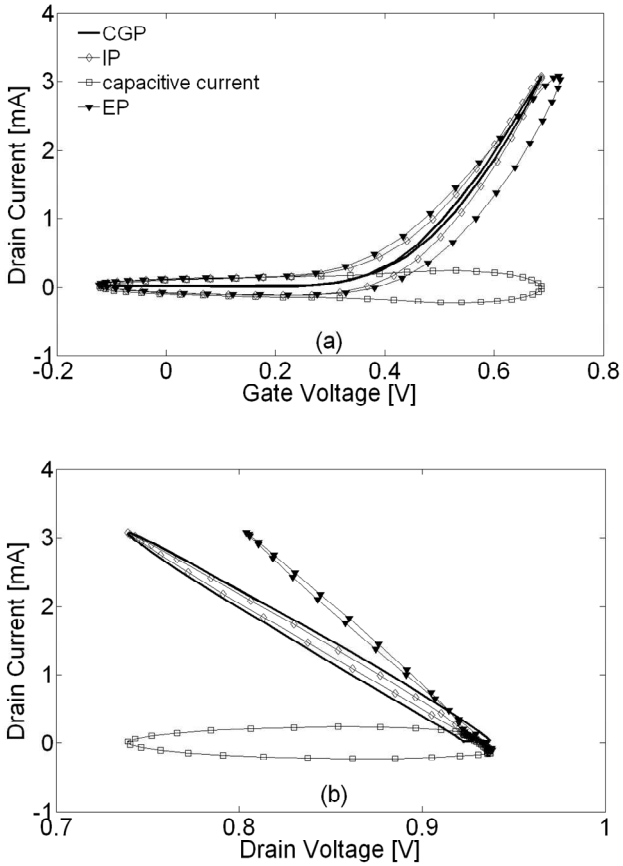

Figure 5-6 Measured (a) transcharacteristic and (b) load line of the FinFET at the extrinsic plane (EP), at the intrinsic plane (IP), and at the current generator plane (CGP). Intrinsic displacement drain current is also shown. Experimental condition: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, and P_{IN} ~ 2.5 dBm.

As further assessment, the resistive component of the drain current retrieved after de-embedding is compared in Figure 5-7 with the prediction of the I-V model which is extracted by adopting the procedure outlined in Chapter 4. The I-V model is excited with the intrinsic voltages obtained after removing the contribution of the parasitic elements (eq. (5.1)). A very good agreement between the I-V model prediction and the de-embedded load line is achieved. This result again confirms that the procedure correctly provide the electrical quantities at the CGP.

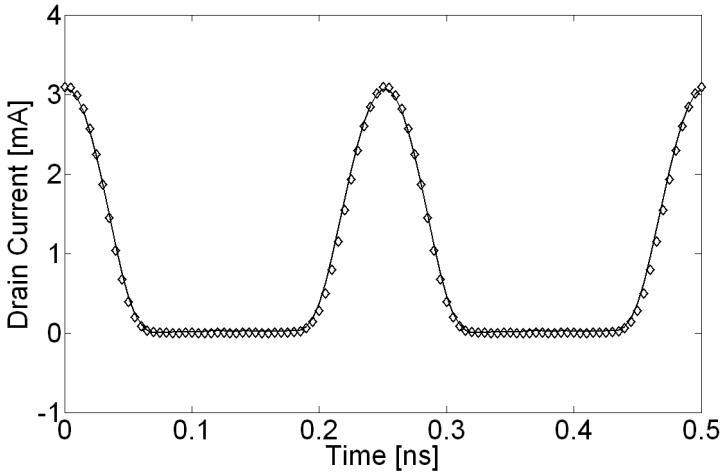

Figure 5-7 De-embedded time-domain waveform of the drain current (line) of the FinFET and I-V model (symbols) prediction at: V_{GS0} = 0.3 V, V_{DS0} = 0.9 V, f_0 = 4 GHz, P_{IN} ~ 2.5 dBm.

5.3.2 AlGaN/GaN HEMT

As second case study, the de-embedding procedure is applied to the RF I-V measurements carried out on an AlGaN/GaN HEMT on SiC substrate with gate length L = 0.7 μm and W = 800 μm (two fingers of 400 um each). Differently from the previous example, where the output impedance is fixed to 50 Ohm by the measurement set-up, active load-pull measurements have been performed with the RF LSNA. Power amplifiers are placed at the input and output port to obtain respectively a significant signal swing at the device input and to actively control the output termination at the RF fundamental frequency. The fundamental frequency f_0 was set to 4 GHz and the quiescent point at V_{GS0} = -2 V and V_{DS0} = 25 V, which corresponds to class-A operation. As for the FinFET, the parasitic network was extracted by exploiting a conventional technique based on "cold" scattering parameter measurements, whereas the bias-dependent capacitances were extracted from multi-bias S-parameter measurements and then stored into a look-up table [9]. In Figure 5-8, a measured RF load line and the corresponding transcharacteristic are illustrated. The measured output power at the EP at the fundamental frequency is about 1.70 W. In Figure 5-9 the same load line and the transcharacteristic after each step of the de-embedding and at each plane are illustrated along with the intrinsic displacement component of the drain current.

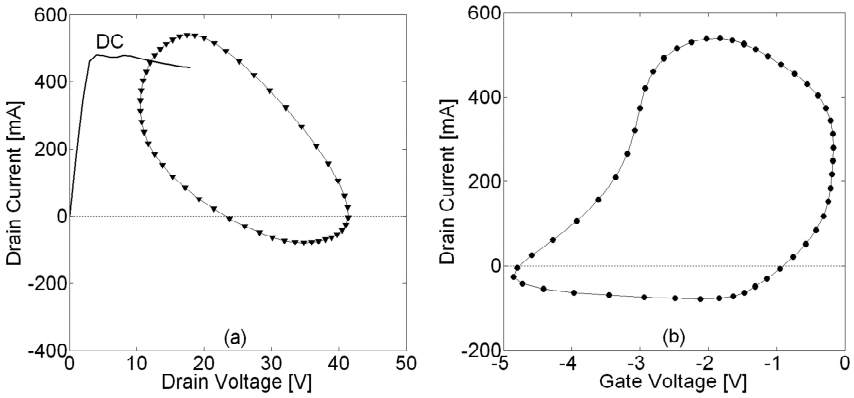

Figure 5-8 Measured (a) load line and (b) transcharacteristic at the extrinsic plane (symbols) at: V_{GS0} = -2 V, V_{DS0} = 25 V, f_0 = 4 GHz, and $P_{OUT}(f_0)$ = 1.70 W. I_{DS}-V_{DS} DC characteristic (continuous line) at V_{GSDC} = -0.2 V.

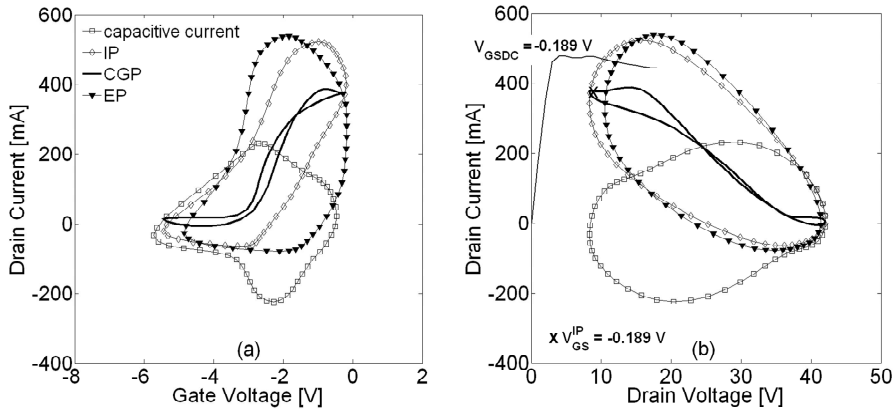

Figure 5-9 (a) Transcharacteristic and (b) load line of the considered GaN HEMT: EP (circles), IP (diamonds), CGP (continuous line), and intrinsic displacement drain current (squares) at: V_{GS0} = -2 V, V_{DS0} = 25 V, f_0 = 4 GHz, and $P_{OUT}(f_0)$ = 1.70 W. In (b) I_{DS}-V_{DS} DC characteristic (thin continuous line) at V_{GSDC} = -0.189 V. In (b), the point highlighted with the symbol 'x' corresponds to the total instantaneous gate-source voltage at the intrinsic plane equal to -0.189 V.

Intuitively, the negative instantaneous values of the measured drain current at the EP are mainly due to the effect of the intrinsic device capacitances, which cannot be neglected at the selected frequency. Also, the significant looping in the transcharacteristic trajectory roughly indicates the presence of a strong reactive component originated by the device capacitive effects. Consequently poor

information can be deduced on the actual RF I-V waveforms at the CGP. On the same plot, the de-embedded load line at the CGP is compared with the output DC characteristic at V_{GS0} = -0.189 V. This value is selected to be equal to the instantaneous intrinsic gate-source voltage corresponding to the point marked on the load line at the CGP. In the absence of dispersive phenomena, the dynamic value of the drain current has to correspond to the static point measured in the same condition. The observed discrepancy is an evident manifestation of LF dispersion.

The load line and transcharacteristic corresponding to different levels of the output power are reported in Figure 5-10 and the same considerations as above hold.

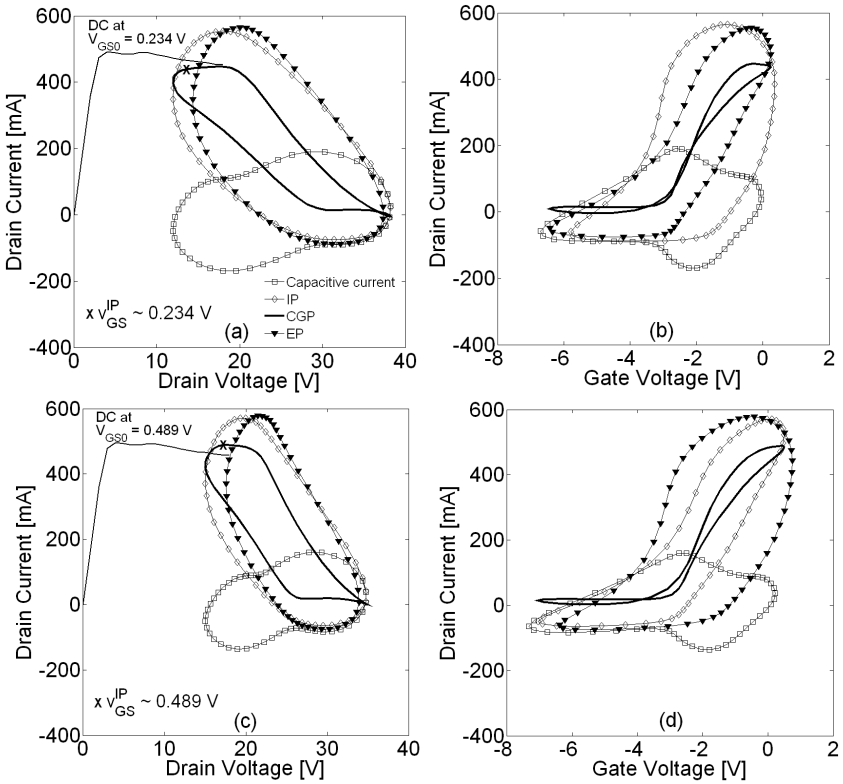

Figure 5-10 Load line at the extrinsic plane (EP), at the intrinsic plane (IP), and at the current generator plane (CGP). The intrinsic displacement drain current is also shown. Experimental condition: V_{GS0} = -2 V, V_{DS0} = 25 V, f_0 = 4 GHz, (a)-(b) $P_{OUT}(f_0)$ = 1.26 W and (c)-(d) $P_{OUT}(f_0)$ = 0.86 W. I_{DS}-V_{DS} DC characteristic at V_{GSDC} = 0.234 V (a) and V_{GSDC} = 0.489 V.

The time-domain waveforms of the drain current of the examples in Figures 5-9 and 5-10 at each plane are shown in Figure 5-11. Similarly to the FinFET, the de-embedded waveform manifests clipping in the pinch-off region, confirming the validity of the de-embedding.

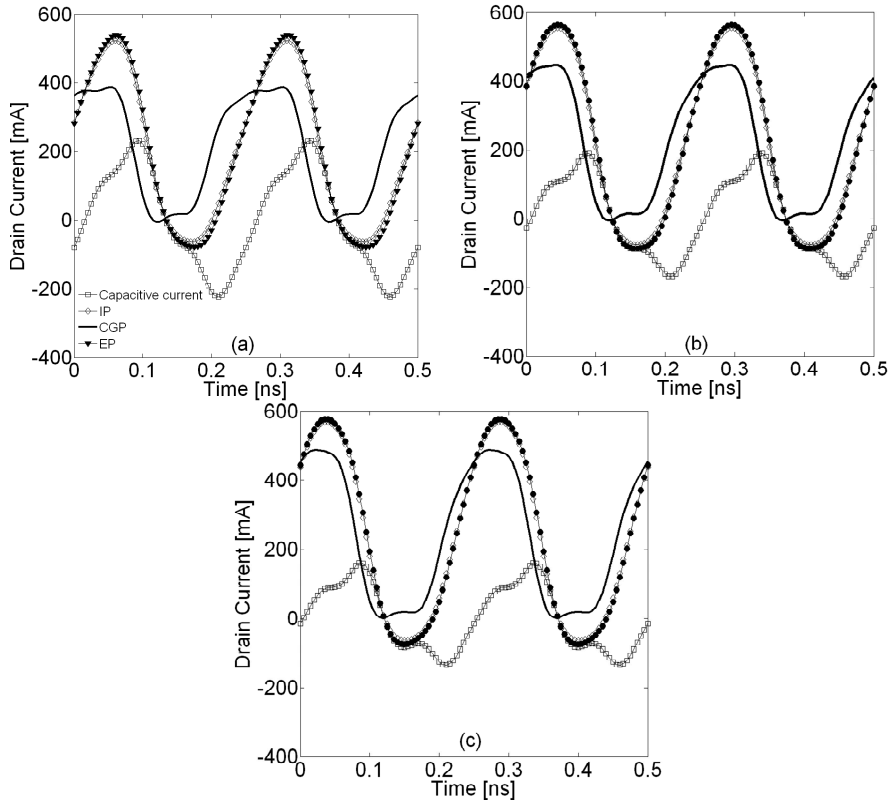

Figure 5-11 Drain current time-domain waveform at the EP (diamonds), IP (triangles), and CGP (continuous line). Intrinsic displacement current (squares). Experimental conditions: V_{GS0} = -2 V, V_{DS0} = 25 V, f_0 = 4 GHz, (a) $P_{OUT}(f_0)$ = 1.70 W, (b) $P_{OUT}(f_0)$ = 1.26 W, and (c) $P_{OUT}(f_0)$ = 0.86 W.

In order to definitely demonstrate the impact of the capacitive core on the impedances synthesized at the current generator plane when microwave operation is involved, in Table 5-I, comparison between the synthesized impedances at the three different considered planes is reported. The numbers in the table further highlight the importance of shifting the measurements at the current generator plane where the synthesized impedances strongly differ from the one obtained at the measurement plane. As it is said in the introduction of this Chapter, the

impedances at the current generator plane determine the voltage and current waveforms which can be compared with the theoretical text-book waveforms.

Table 5-I Output impedances at the different planes up to the third harmonic.

$P_{OUT}(f_0)$(W)	f (GHz)		$Z_{L,EP}(\Omega)$	$Z_{L,IP}(\Omega)$	$Z_{L,CGP}(\Omega)$
0.86	f_0	4	12.0+j*16.9	16.3+j*20.9	29.1+j*16.8
	$2f_0$	8	28.3-j*16.5	28.9-j*10.9	20.5-j*25.1
	$3f_0$	12	58.0+j*18.5	70.4+j*12.4	18.5-j*27.8
1.26	f_0	4	18.4+j*25.2	23.5+j*29.5	47.4+j*20.3
	$2f_0$	8	28.1-j*16.8	28.8-j*11.5	25.0-j*23.7
	$3f_0$	12	54.6+j*18.2	67.0+j*14.0	17.4-j*26.4
1.7	f_0	4	31.4+j*37.7	38.8+j*42.2	82.0+j*5.6
	$2f_0$	8	27.8-j*17.2	28.7-j*12.3	29.1-j*16.9
	$3f_0$	12	53.9+j*23.3	69.4+j*19.5	20.4-j*26.6

5.4 Embedding versus de-embedding

The embedding and de-embedding techniques can be interchangeably exploited to shift the voltage and current waveforms from the CGP plane to the extrinsic one and vice versa. In this work, an embedding method is adopted as further validation for the de-embedding procedure, according to the following steps:

I) starting from an RF I-V measurement, de-embedding is applied and the electrical quantities at the CGP-resistive core are obtained;

II) under the assumption that the resistive core behavior is frequency independent above the cut-off frequency of LF dispersion, the intrinsic voltages across the CGP terminals and the intrinsic resistive currents are mathematically shifted down to the LF frequency (f_{0LF} = 2 MHz) by applying eqs. (5.13) and (5.14);

III) from II), the LF incident waves at the CGP can be calculated and uploaded into an AWG. The uploaded waveforms are then used as excitations to perform I-V measurements at the fundamental frequency f_{0LF} = 2 MHz [22], [23] on the same device;

$$a_j^{IP}(t) = \frac{v_{jS}^{IP}(t) + 50 * i_j^{IP,R}(t)}{2} \quad j = G,D \tag{5.14}$$

IV) the measured currents and voltages at the CGP at 2 MHz are mathematically (eqs. 5.13 and 5.14) shifted up to the frequency of the RF measurement of I). Next, the intrinsic displacement currents are calculated by using the up-converted intrinsic voltages in combination with eq. (5.3) where the matrix $\underline{\underline{C}}$ is replaced with the known nonlinear capacitances. Finally, when all the electrical quantities at the intrinsic plane are determined, the corresponding voltages and currents at the extrinsic plane are obtained by simply applying in sequence eq. (5.6) and eq. (5.1).

An example of the procedure is illustrated in Figure 5-12. The **de-embedded** RF load line at f_0 = 4 GHz is compared with the LF measurement at f_0 = 2 MHz at the CGP in Figure 5-12(a); on the other hand, the **embedded** load line, obtained starting from the measurement at f_0 = 2 MHz after applying steps II)-IV), is compared with the RF measurement at f_0 = 4 GHz at the EP in Figure 5-12(b). In both cases a good agreement is achieved, though it is noteworthy to mention that the accuracy of the de-embedded and embedded load line strongly depends on the accuracy of the adopted model of the capacitive core and parasitic elements. Nevertheless, the example shows that embedding and de-embedding can be interchangeably exploited for simultaneously monitoring the shape of the load line both at the CGP and at the EP. This load line can be qualitatively evaluated and used as starting point for circuit performance optimization.

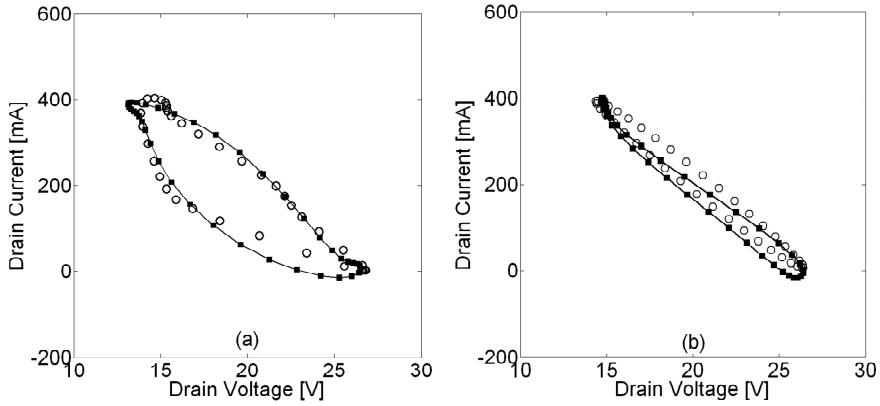

Figure 5-12 Measured load line (symbols) for the considered GaN HEMT at (a) f_0 = 2 MHz and (b) f_0 = 4 GHz. The continuous line represents the load line obtained after (a) 'de-embedding' and (b) 'embedding'. The quiescent condition in is V_{GS0} = -2 V and V_{DS0} = 20 V.

In Table 5-II the values of the output impedance at the fundamental frequency, which is calculated after applying the two procedures, is reported both for the CGP and the EP. The numbers in the table constitute a further indication of the correctness of the concepts outlined over the whole Chapter.

Table 5-II Output impedance at the extrinsic (EP) and current generator plane (CGP) after embedding and de-embedding of the load line in Figure 5-12.

	$Z_{L,CGP}(\Omega)$	$Z_{L,EP}(\Omega)$
DE-EMBEDDING	29.8-j*11.2	30.6-j*4.4
EMBEDDING	30.3 - j*10.7	28.9 + j*2.8

5.5 Waveforms-only based nonlinear de-embedding

5.5.1 Procedure

The de-embedding method described in Section 5.2.1 requires the accurate knowledge of the parasitic networks and the reactive nonlinearities associated with the active device. So far, the parasitic elements and the nonlinear charge sources, or the nonlinear capacitances, have been obtained from multi bias S-parameters and, in case of the nonlinear charge sources, they are stored in a look-up-table indexed by the intrinsic voltages. Alternatively, the Q-V functions can be determined directly from large-signal measurements by which the parameters of semi-empirical expressions describing the value of the terminal charge as a function of the intrinsic voltages can be extracted. This point is already discussed in Chapter 4 and it relies on the combination of nonlinear measurements performed at different frequencies. The identification procedure is reported in the following, although details can be found in Chapter 4:

1) nonlinear measurements are performed at two different frequencies, 2 MHz and 4 GHz in the present case, and at a fixed bias condition (V_{GS0} = -2 V and V_{DS0} = 20 V) . This ensures that for both experiments the occupation state of the traps is fixed. The thermal state, instead, is varies for each measured load line. The reason of the double frequency selection is well explained in Section 4.3.3;

2) eqs. (5.11)-(5.12) are employed by which the nonlinear functions f_G, f_D, Q_{GS}, and Q_{GD} are replaced by semi-empirical expressions. The output capacitance C_{DS} is assumed to be constant;

3) by combining the measurements with numerical optimization, it is possible to determine both the dispersive current sources and the non-dispersive charge sources for the fixed bias condition. Within the optimization routine, the values of the parasitic elements are optimized as well.

Once the parasitics and the charge sources are properly identified, de-embedding can be applied to any RF load line measured at the extrinsic plane. This is practically illustrated in the following Section.

5.5.2 Application to AlGaN/GaN HEMT waveforms

Active load-pull measurements have been performed at V_{GS0} = - 3 V and V_{DS0} = 25 V, and f_0 = 4 GHz on an AlGaN/GaN HEMT on SiC substrate with gate length L = 0.7 μm and W = 800 μm (two fingers of 400 um each). The bias condition intentionally differs from the one selected for the optimization routine carried out to identify the Q-V functions. With reference to eqs. (5.11) and (5.12), the change of the bias point would enforce the extraction of a new I-V model, unless a bias-dependent electro-thermal nonlinear model is available. In fact, the change of the bias point affects only the current source, through the variation of the variable X_0. As stressed previously, the need of a global I-V model is circumvented by exploiting nonlinear de-embedding. In fact, as the Q-V functions can be reasonably assumed to be the same regardless the quiescent condition and the junction temperature, the nonlinear de-embedding actually provides the waveforms at the CGP corresponding to a fixed thermal state (T_0), which is set by the power efficiency of the measured RF load line, and to a fixed state of the traps (X_0 =f(V_{GS0}, V_{DS0})) The results of the full nonlinear de-embedding are shown in Figure 5-13.

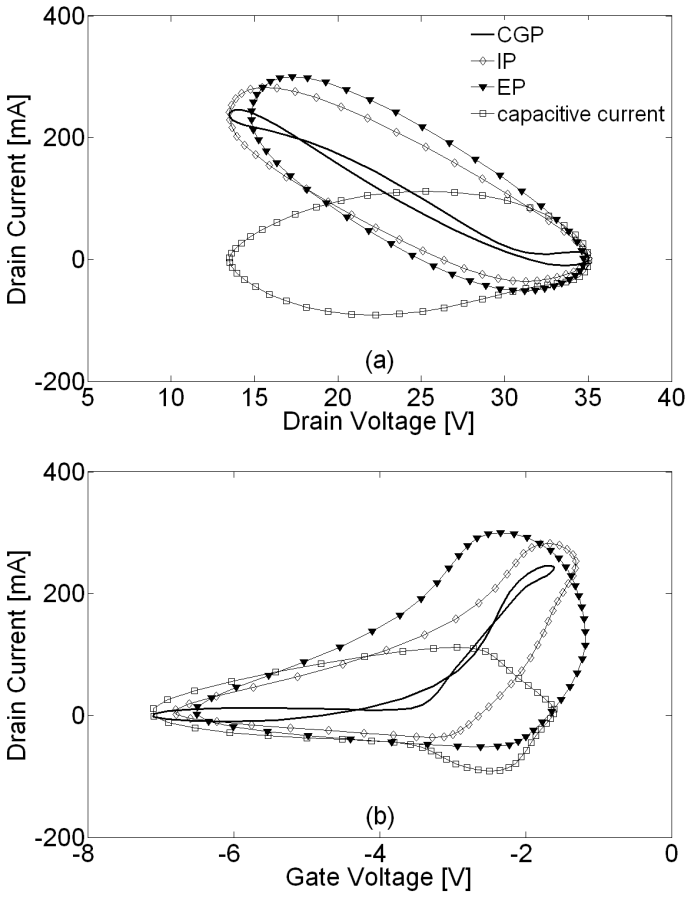

Figure 5-13 (a) Load line and (b) transcharacteristic at the measurement plane (EP) (squares), at the intrinsic plane (IP) (circles), and at the current generator plane (CGP) (continuous line). Intrinsic displacement drain current (triangles). Experimental conditions: V_{GS0} = -3 V, V_{DS0} = 25 V, f_0 = 4 GHz, $P_{OUT}(f_0)$ = 0.74 W. Values of the output impedance at the different planes: $Z_{L,EP}(f_0)$ = 45.3+j*36.0 Ω, $Z_{L,IP}(f_0)$ = 58.6+j*37.7 Ω, and $Z_{L,CGP}(f_0)$ = 80.1-j*15.8 Ω.

As for the cases previously investigated, the waveform of the drain current at the current generator plane manifests clipping, which is the expected behavior for the resistive component of the intrinsic current. Another qualitative indication of correct de-embedding arises from the dynamic transcharacteristic which has to show approximately no or only small looping when the time-domain trajectories over the intrinsic voltages plane cross the saturation region. This condition is actually verified for the de-embedded transcharacteristic.

Nevertheless, in order to further validate the proposed approach, the de-embedded characteristics of Figure 5-13 are compared in Figure 5-14 with the harmonic balance simulations of two I-V models. One model is extracted at a fixed bias point, V_{GS0} = - 2 V and V_{DS0} = 20 V, as outlined in Chapter 4. The second nonlinear model adopts the formulation proposed in [9] which fully accounts for low-frequency dispersion.

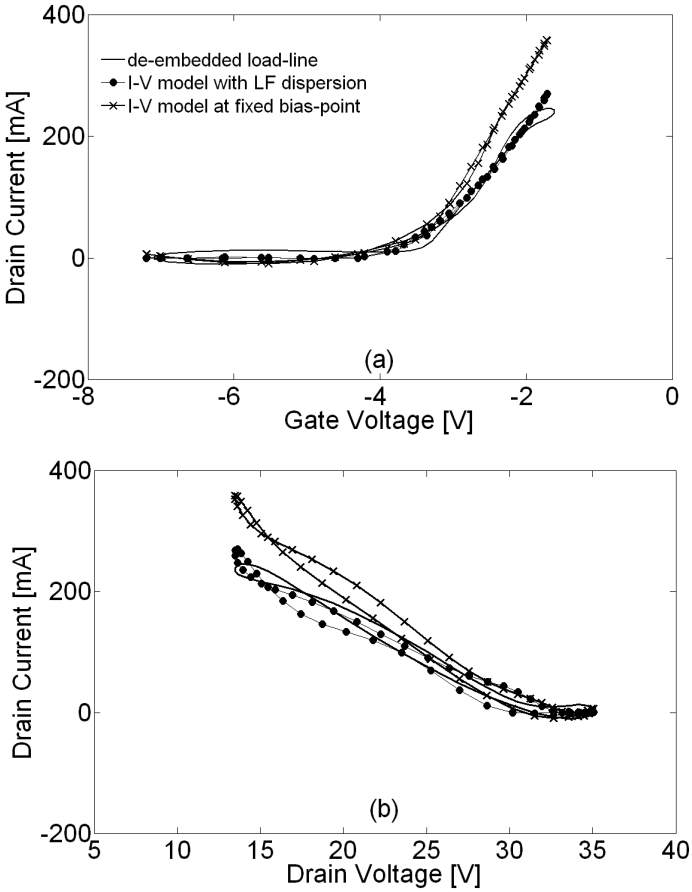

Figure 5-14 (a) Transcharacteristic and (b) load line at f_0 = 4 GHz, V_{GS0} = -3 V, V_{DS0} = 25 V: after nonlinear de-embedding (continuous line); simulation of the I-V model in [9] (dotted line); simulation of the I-V model extracted at V_{GS0} = -2 V, V_{DS0} = 20 V (crosses).

Both models are simulated at V_{GS0} = - 3 V and V_{DS0} = 25 V and excited with the intrinsic voltage waveforms which are obtained by applying eq. (5.1) to the

measured RF waveforms of Figure 5-13. As expected, the dynamic I-V characteristics predicted by the I-V model extracted at V_{GS0} = -2 V and V_{DS0} = 20 V evidently deviate from the one obtained after nonlinear de-embedding. On the other hand, the simulation of the I-V characteristics of the nonlinear model whose formulation fully includes dispersion display good agreement with the de-embedded characteristics. This is in agreement with eqs. (5.11) and (5.12) and, importantly, definitely confirms the validity and accuracy of the proposed nonlinear de-embedding procedure.

5.6 Conclusions

This Chapter focuses on methods to de-embed raw RF measurements in order to shift the RF waveforms from the measurement reference plane closer up to the active device plane. Basically, both from a characterization and design point of view, it is fundamental to accurately know the transistor I-V characteristics. The latter define transistor performance and, moreover, are used as reference for current and voltage waveforms shaping, which is crucial to achieve the optimal RF performance. Nevertheless, when the voltage and current waveforms are measured in the RF and microwave range, they poorly provide information about the actual I-V waveforms due the unavoidable contributions of the parasitics and the intrinsic capacitances of the active device. The methods described in this Chapter allow one to retrieve the I-V dynamic characteristics starting from RF measurements. The proposed technique requires that both the value of the parasitic elements and the device nonlinear capacitances are known. Parasitic elements and capacitances value can be extracted either through well established techniques based on multi-bias multi-frequency S-parameter measurements or directly through nonlinear time-domain measurements. The main advantage of the proposed approach consists of not requiring any knowledge about the current source behavior, which is strongly affected by complex physical phenomena such as charge trapping and thermal effects. The extraction of a global model for the current sources, which account for all those effects, might not be a straightforward task. In this perspective, the *de-embedding* method here proposed simplifies the complexity related to model's extraction. In fact, any RF I-V which corresponds to a fixed state for the traps and temperature can be shifted up to the current generator plane and the actual I-V characteristics can be inferred for the considered RF condition. Nevertheless this approach is valid only if the effect of dispersive phenomena on the value of the parasitics and of the device capacitances is negligible as compared with the effect on the current sources. Actually, in many practical cases this

assumption is verified. For instance, in Chapter 2 it is shown that the gate displacement current measured at RF is negligibly dependent on the substrate temperature. As a remark, this technique can be potentially exploited for the design of high-efficiency power amplifiers for which the waveforms control is crucial. Although not proven in this work due to instrumentation's restrictions, the RF waveforms synthesized at the extrinsic plane could be shifted in real-time to the current generator plane and iteratively tweaked to achieve the optimal RF performance.

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Conclusions and outlook

6.1 Main achievements of this work

This PhD has focused on the characterization and modeling of microwave transistors. More precisely, the interest was addressed to the investigation of the transistors characteristics under large-signal operation. In a transmitter, this condition is typically experienced by the transistors employed in the design of RF power amplifiers.

The first part of the work has been devoted to the development of a novel (at the time this PhD has started) characterization system. A RF LSNA set-up was already available. The further extension of the hardware was needed to perform a more complete investigation. A solution has been proposed by NMDG and it was primarily meant to enhance the RF LSNA under modulated excitations in 50 Ohm environment. After the initial phase of the set-up assessment, we have added further software and hardware changes in order to develop combined low- and high-frequency load-pull capabilities. As extensively reported in both the characterization and the modeling phases of this work, low-frequency nonlinear measurements can be conveniently exploited to gain a deeper insight in transistor dynamic behavior and to enhance the modeling step.

As regarding the characterization, low-frequency load-pull has been exploited to highlight the effect of dispersion of transistors large-signal characteristics. Dispersive effects encompass charge trapping mechanisms, originated by the presence of defects in the semiconductor materials, and thermal effects which unavoidably modify the physical and electrical parameters of transistors. Among the investigated transistors and within the explored operating conditions, the gallium nitride based device has resulted the mostly sensitive to dispersion, in agreement also with the literature. A significant current or power collapse has been observed and this directly reflects on the deliverable output power at high frequencies. Moreover it is shown that the current collapse is frequency dependent in the case of the gallium nitride and this has also implication on the models formulation.

It is interesting to note that this information can be directly inferred by looking at the measured calibrated voltage and current time-domain waveforms. Undoubtedly, when these waveforms are available a more comprehensive view on

the transistor behavior is obtained. The interest in looking directly at waveforms has actually raised among researchers. As an example, we have shown their acquisition in the low-frequency range is essential for a proper reconstruction of the waveforms of transistors operating under high-frequency modulation.

Waveforms can be successfully exploited for the direct identification of large-signal transistor models. Techniques relying only on high-frequency waveforms or only on low-frequency ones existed. In this work the low- and high-frequency information have been unified and models for high frequency applications can be built by exploiting combined low- and high- frequency experimental waveforms. Transistors nonlinear models are represented in terms of current-voltage and charge voltage relationships which are mathematically described by semi-empirical expressions. The models parameters are determined through numerical optimization. It is worth to mention that the unique capability of the proposed identification approach consists of separating the model parameters into two sets, computed from the low- and high-frequency waveforms respectively. Such a choice undoubtedly assures shorter optimization times and reduces model parameter uncertainty.

Within the modeling activity, a macromodeling approach has been exploited to represent the microwave linear behavior of a silicon transistor. The technique, developed at the University of Ghent, has been originally oriented to the modeling of passive electromagnetic structures. In this work it is used for the modeling of the multi-bias and multi-frequency scattering matrix of a silicon transistor. The obtained model yields very accurate predictions comparable with the ones obtained with an artificial neural networks based model and it can be implemented in a commercial circuits simulator. Moreover, the macro-modeling technique may constitute an alternative to the table-based approaches which are often exploited for describing the bias-dependent linear behavior of transistors.

Current and voltage time-domain waveforms are also widely exploited for the design of high-frequency power amplifiers. Among the microwave researchers, waveform engineering techniques are known as a ‘tool’ to shape the current and voltage waveforms to optimize the delivered power and maximize the level of power efficiency. It is well-researched that such techniques can be strictly applied at the current generator plane. With reference to a typical equivalent network representation of a field effect transistor, this plane is placed at the terminals of the nonlinear current generator between the intrinsic source and drain. Nevertheless, the voltage and current waveforms measured in the high frequency range include the effect of the layout parasitic elements and the reactive currents originated by the transistor capacitances. These contributions significantly mask the actual

information needed by the designer. In this work a technique to remove or de-embed the unwanted contributions has been described. It relies on the knowledge of only the values of the parasitic elements and the nonlinear transistor capacitances. Once these elements are known, the actual waveforms at the current generator plane can be retrieved by applying a full nonlinear de-embedding. Interestingly, this approach prevents the need of a nonlinear model for the drain-source current generator. An electro-thermal model would be required for dispersive devices and its extraction is a challenging task. The proposed technique provides the actual response of the current source for the particular condition of the high-frequency large-signal measurements which the de-embedding is applied to. Though de-embedding of raw high-frequency measurements is a well-known concept, according to our knowledge a full nonlinear waveforms de-embedding is here presented for the first time.

6.2 Future work

The activity presented in this work constitutes a small yet valuable contribution in the field of nonlinear characterization and modeling of transistors for high-frequency applications. The work that has been done so far can evolve into at least three directions:

- firstly, the further extension of the characterization system. At the time this PhD has started, it has been decided to extend the RF LSNA down to 10 kHz in order to speed up the assessment of the prototype. Basically this frequency limit is now defined by hardware components, such as the low-frequency bias-tees. Work has been done during this PhD to design an alternative solution for the bias-tee. The proposed design allows one an extension of the frequency range down to 60 Hz. On the other hand, the design circuit yields the expected performance up to 5 MHz. Therefore additional effort is required to make the bias-tee working over a broader frequency range. It is experimentally observed that transistors large-signal characteristics are frequency dependent and the most significant variation appears between the DC and 10-100 kHz. Large-signal measurements in the hertz to tens of kilohertz range are thus preferred. Furthermore, the frequency range is not the only specification to be satisfied as the bias-tee must operate at high-level of DC voltage currents and handle large-signal swings. As the proposed solution relies on active components, the level of distortion introduced by the bias-tee itself must be as possibly minimized.

- Promising additional work goes also in the direction of nonlinear modeling. In this work empirical models formulated in terms of I-V and Q-V functions have been identified starting from the experimental current and voltage large-signal waveforms. As next step, the large-signal waveforms measured at different substrate or case temperatures can be exploited for a consistent identification of a thermal model. This implies also the characterization and the determination of the thermal impedance. Interesting work can be also done as regarding the generation of behavioral models. Black-box models for transistors have gained a lot of attention in the last years. These models are independent on the device physics and can be generated directly from measurements. However, being fully empirical, they offer poor prediction capabilities. Therefore they are accurate in the range of the experiments used for their extraction. In this perspective, when these models are identified on the basis of time-domain waveforms the latter must be as complete as possible to accurately capture the nonlinear behavior of transistors. For example, the RF waveforms generated by the transistor under modulated excitations are commonly exploited to generate behavioral models whereas the frequency component generated at baseband are disregarded. In this work, an example is reported to show that for transistors the low-frequency information is essential for the correct reconstruction of the voltage and current time-domain waveforms. For behavioral modeling purposes, it is fundamental and relevant to enhance the model accuracy by accounting for the complete waveforms in the model extraction phase.

- As regarding the nonlinear de-embedding, the work can be promisingly continued also in view of the interest in the community of microwave designers in this subject. As first step the proposed embedding can be adapted and tested for packaged devices for which parasitic elements due to package and wire bonding are definitely more significant than the ones of on-wafer structures. It would be significant to come up with an automatic procedure allowing to engineer the RF waveforms while monitoring in real-time what is going on at the current generator plane. This can have not only academic interest but it can have important practical (i.e., market-related) implications for the design of power amplifiers. Finally and in the short-time term, the proposed nonlinear de-embedding can be improved by controlling also the impedances at transistor nodes also at the harmonic frequencies. In this work, due to hardware limitations, only the impedance at the fundamental frequency has been tuned. Nevertheless, the contribution of the harmonic frequencies is crucial for the design of high-efficiency power amplifiers.

Appendix A

Combined LF-RF LSNA: architecture and calibration

In the following, the architecture of the LF LSNA (also called *'dynamic-bias'*) including the test-set is described and the calibration procedure is outlined step-by-step. Next it is shown how the LF LSNA is practically combined with an RF LSNA by stressing in particular on the alignment procedure (Section 2.3) of the LF and RF calibration coefficients.

A.1 Complete architecture

The different parts composing the characterization system are here described in more detail. In Figures 6-1, 6-2, and 6-3 the receiver front-end, the LF LSNA, and the RF LSNA blocks diagrams are illustrated. The whole system is controlled via GPIB and USB interfaces and the receiver front-end communicates with the PC through an RS-232 port. A 10 MHz clock acts as synchronization signal. All the control and computation software has been developed with Mathematica Wolfram.

A.1.1 Receiver front-end

The receiver front-end, illustratively shown in Figure 6-1, consists of a PXI of National Instruments which is equipped with eight ADC channels, used for the signal acquisition, and a DAC channel which can act also as arbitrary waveform generator (AWG). The sampling frequency of the ADCs is equal to 60 MS/s with a resolution of 12-bits, whereas the sampling rate of the DAC is equal to 100 MS/s with a resolution of 14-bits. For the architecture of this work channels 0-3 are used for the RF LSNA signal acquisition and channels 4-7 are for the LF LSNA signal acquisition.

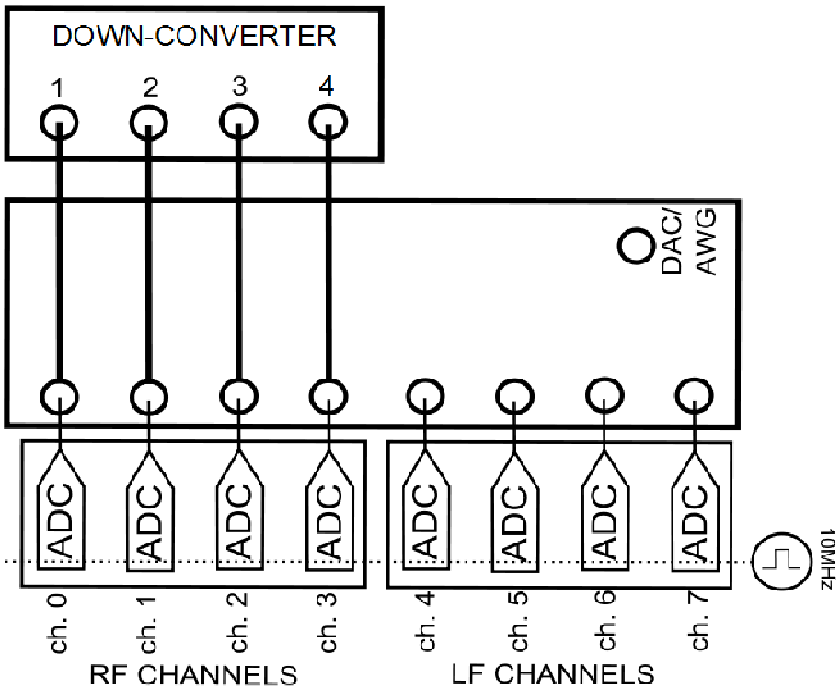

Figure 6-1 8-channels PXI NI-104. The channels for the RF acquisition are connected to the outputs of the down-converter.

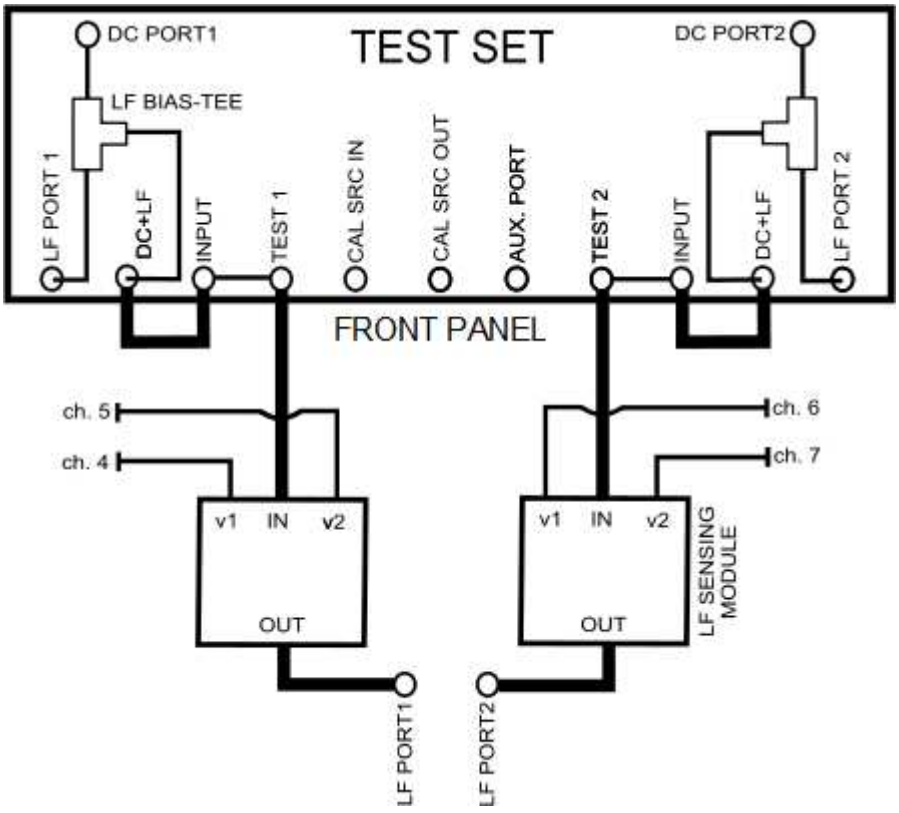

Figure 6-2 LF LSNA and LF test-set.

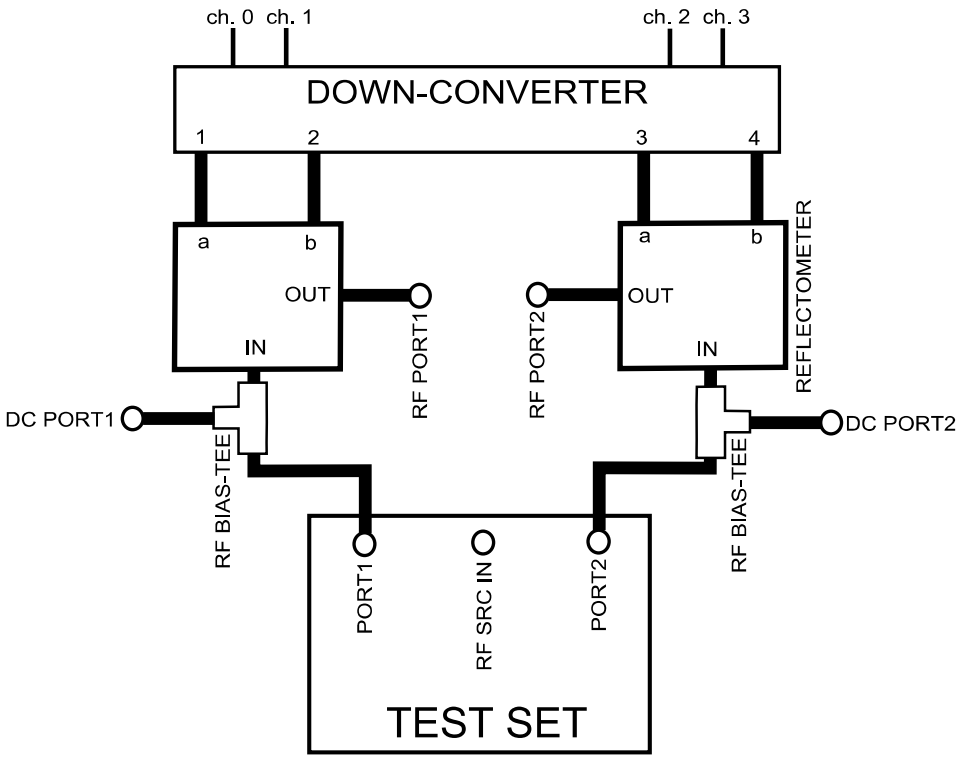

Figure 6-3 RF LSNA and RF test-set.

A.1.2LF LSNA (dynamic-bias)

The LF LSNA block diagram is shown in Figure 6-2 along with the test-set. The latter is mainly composed of switches controlled via software and which allow the user to automatically set the LF LSNA either in calibration or measurement mode. The control signals to the test-set module are sent through a USB port, available on the rear panel of the test-set box. LF bias-tees are also included in the test-set (see Section 2.3). They combine the DC voltages/currents and the LF signals applied externally through the DC and LF PORT1-2. CAL SRC IN, CAL SRC OUT, and AUX. PORT are exploited within the calibration routine, as will be explained in section A.2.1. DC+LF and INPUT1-2 ports are used for external signal routing. The connection between the test-set and the LF sensing modules' input IN is made via BNC cables through the ports TEST1-2. The LF sensing modules, whose output is connected to the DUT ports, also redirect the sensed LF voltage/current signals to the receiver front-end channels 4-7 via SMB-to-SMB cables.

A.1.3RF LSNA

The architecture of the RF LSNA is depicted in Figure 6-3. Since a comprehensive description of this set-up can be found in [A1], the main blocks and their functionalities are only briefly described here. The RF LSNA of this work is composed by an RF test-set, two broadband couplers/reflectometers (50 MHZ – 50 GHz), and a down-converter. The test-set is made of switches which are software controlled. These switches allow one to connect the input of the reflectometers either to the signal used for the calibration (RF SRC IN) or to an internal 50 Ohm load through PORT1 and PORT2. The reflectometers separate and sense the traveling waves at the RF PORT1-2. The ‘a’ and ‘b’ ports are connected to the inputs of the down-converter. The latter actually shifts the sensed RF traveling wave to the IF bandwidth [A1]. The down-converted traveling waves are then sampled and digitized by the channels 0-3 (Figure 6-1). RF bias-tees can be placed on the signal path when also DC voltage is applied, as illustrated in Figure 6-3.

A.1.4LF-RF LSNA

The LF and RF LSNA set-ups illustrated in Figure 6-2 and Figure 6-3 are combined for characterization of nonlinear DUTs with modulated excitations. In fact, they enable the synchronous acquisition of the RF and LF voltages and currents at RF PORT1, RF PORT2, LF PORT1, and LF PORT2.

A.1.4.1 Separate DC/LF and RF ports

As for the example of the power amplifier stage discussed in section 2.4, the DUT may have the DC/LF and RF ports physically isolated due, for instance, to the presence of RF matching networks and bias-circuits. In this situation, the set-ups in Figures 6-2 and 6-3 are connected as in Figure 6-4 and do not require any change in the hardware configuration, though they operate synchronously.

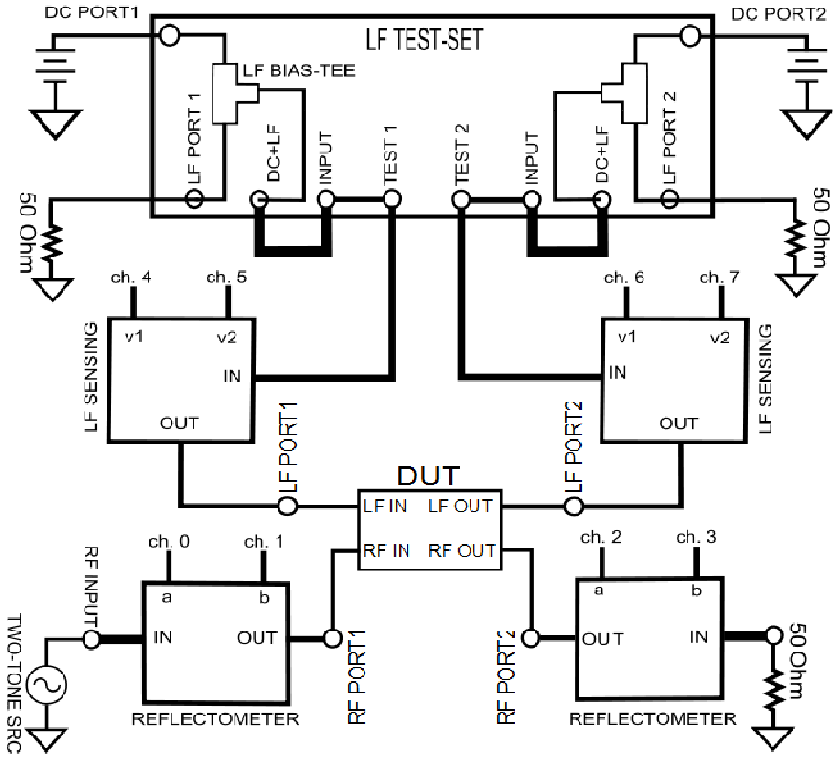

Figure 6-4 LF-RF LSNA for nonlinear characterization with RF two-tone excitation and 50 Ohm load at the RF output ports and at the LF input and output ports. The DC/LF and RF ports are physically isolated.

A.1.4.2 Common DC, LF and RF ports

This situation is typical for on-wafer DUTs, such as transistors, where the DC, LF, and RF signals are applied together at the same reference plane (the probe tips). This implies that the DC, LF, and RF excitations have to be combined at the same plane. This is accomplished with a broadband diplexer which is placed as illustrated in Figure 6-5. Note that in the reported block diagrams the connections from the reflectometers and the LF sensing modules to the receiver front-end are omitted. However it is assumed that they are untouched from the moment the calibration starts till the actual measurement is performed. The diplexer used in this work covers the LF BW from DC to 25 MHz and the RF BW from 90 MHz up to 45 GHz.

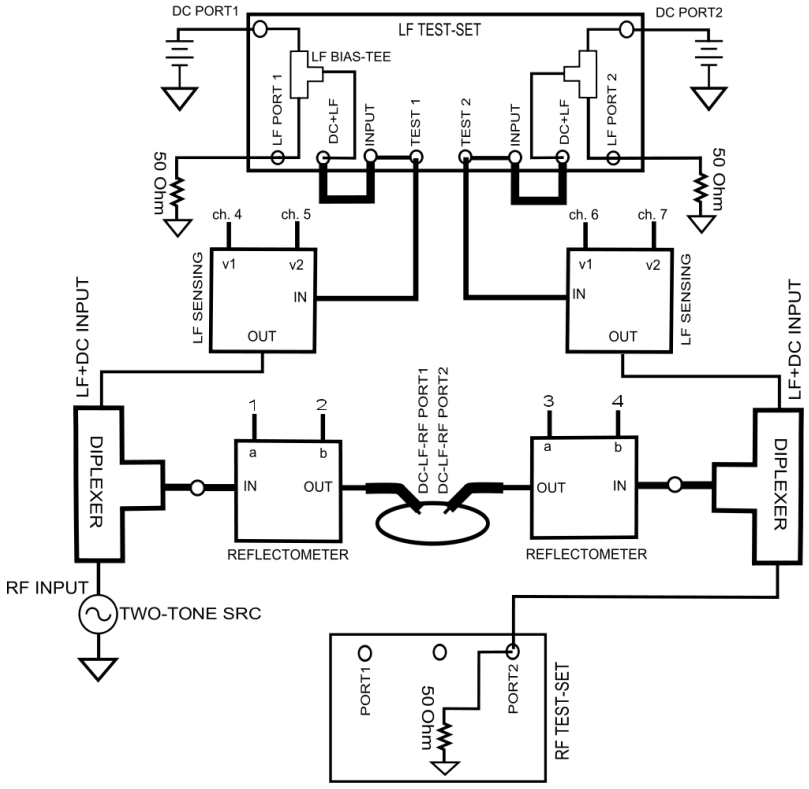

Figure 6-5 LF-RF LSNA for on-wafer nonlinear characterization with RF two-tone excitation and 50 Ohm load at the LF and RF output ports. The DC, LF, and RF signals are at the same reference plane.

A.2 LF LSNA

In what follows, the test-set configurations for the calibration and the measurement mode are described for the LF LSNA.

A.2.1 LF LSNA calibration mode

In calibration mode the DAC output on the PXI front panel (Figure 6-1) is connected to the CAL SRC IN using a BNC-to-SMB cable. As explained in section 2.3, the DAC is used as an AWG and provides both the signal for the LF relative calibration and the reference signal for the LF absolute calibration. This signal is a multi-sine of equally spaced 2400 tones and it is generated through a software

interface (NI-FGEN-Labview) which allows one to remotely control the DAC. The procedure to generate and pre-characterize the calibration signal is as follows:

1. the time domain samples of the multi-sine are created via software;

2. the time samples are uploaded to the DAC through the interface of the control software which also enables to set the sampling rate and the gain of the DAC;

3. the analog output of DAC is connected to CAL SRC IN on the test-set front panel using a BNC-to-SMB cable. An internal switch, controlled by the USB port on the rear panel of the test-set, connects CAL SRC IN to CAL SRC OUT;

4. CAL SRC OUT is connected to one of the channels of the LF acquisition section using a BNC-to-BNC cable (by default channel 4 of the PXI);

5. The spectrum of the measured signal is stored and used as power and phase reference (PPR) for the absolute calibration step.

It is important to mention that after these steps, the cables' connections between the DAC and the test-set must stay untouched during the calibration routine. After steps 1.-5. the actual calibration procedure is performed (A.2.1.11).

A.2.1.1 LF LSNA calibration procedure

Firstly, the relative calibration is carried out in order to determine the seven unknown coefficients of the error matrix (cfr. eq. (2.1)). A S-O-L-T (Short-Open-Load-Thru) method is used in this work. For coaxial calibration, BNC standards are connected to LF PORT1-2, and for on-wafer calibration, standards on a ceramic calibration substrate are used. It is noteworthy that within the calibration frequency grid (10 kHz-24 MHz) the calibration standards can be assumed ideal (Γ_S, Γ_O, and Γ_L equal to -1,1, and 0, respectively, and the 'thru' with zero electrical length).

Next the absolute calibration is performed. For coaxial measurement it only requires that the CAL SRC OUT is connected to the coaxial LF PORT1. As pointed out in section 2.3, the situation is different for on-wafer measurements because the probe tips cannot be connected directly to the coaxial CAL SRC OUT.

An auxiliary port is thus needed and this is available on the test-set front panel (AUX. PORT) (Figure 6-2). The calibration plane at the probe tips is shifted to the auxiliary port through an additional S-O-L calibration.

The full LF calibration procedure is described step-by-step in the following. Throughout the calibration procedure, the switches' configuration inside the test-set module is controlled via the software:

1) LF Port1 is left OPEN (or probe in air), and the calibration signal is routed and applied to TEST1;
2) LF Port1 is connected to a SHORT, and the calibration signal is applied to TEST1;

3) LF Port1 is connected to a LOAD, and the calibration signal is applied to TEST1;
4) LF Port2 is left OPEN (or probe in air), and the calibration signal is routed and applied to TEST2;

5) LF Port2 is connected to a SHORT, and the calibration signal is applied to TEST2;

6) LF Port2 is connected to a LOAD, and the calibration signal is applied to TEST2;

7) LF Port1 and LF Port2 are connected with a 'THRU', and the calibration signal is alternatively applied to TEST1 and TEST2 while the other port is terminated with a 50 Ohm load through an internal switch of the test-set.

Next, the absolute calibration is carried out. For coaxial calibration it requires that the PPR (CAL. SRC OUT) is connected to LF Port1 whereas TEST1 is terminated with a 50 Ohm load inside the test-set box.

For on-wafer calibration the auxiliary port is exploited instead and the following steps are required:

8) probes tip are untouched after step 7), and the calibration signal is routed to TEST1, while TEST2 is connected to AUX. PORT;

9) Measurement with the AUX. PORT left OPEN;

10) Measurement with the AUX. PORT connected to a SHORT;
11) Measurement with the AUX. PORT connected to a LOAD;

12) Measurement with the probes untouched and the PPR (CAL SOURCE OUT) connected to the AUX. PORT.

At the end of the LF calibration routine, the correction coefficients of the error model are automatically computed and stored in a file. Also, the switches' configuration is set via software in the default measurement mode.

A.2.2LF LSNA measurement mode

In the default measurement mode (Figure 6-6), TEST1-2 are connected to INPUT1-2 by internal switches. TEST1-2 are also connected to the LF sensing modules' input IN with a BNC-to-BNC cable. Depending on the application, externals signals can be injected either directly at INPUT1 and INPUT2, or at the LF sensing modules' input, or through the LF bias-tees present inside the test-set box (as in Figure 6-6Figure 6-6) . The LF bias-tees combine the signal applied at LF INPUT 1-2 with the DC voltages (currents) supplied at the DC PORT1-2. The output of the LF bias-tee is connected to the DC+LF port with another internal switch. In the default configuration of Figure 6-6 the DC+LF ports are connected to INPUT1-2 through an external BNC-to-BNC cable. Alternatively, INPUT1-2 can be connected to customized external bias-tees. For illustrative purpose, in Figure 6-6 the LF LSNA configured for on-wafer LF nonlinear characterization with a 50 Ohm load is depicted. Clearly, by replacing the passive load at LF INPUT2 with a signal source, the LF LSNA can be exploited as a low-frequency active load-pull system.

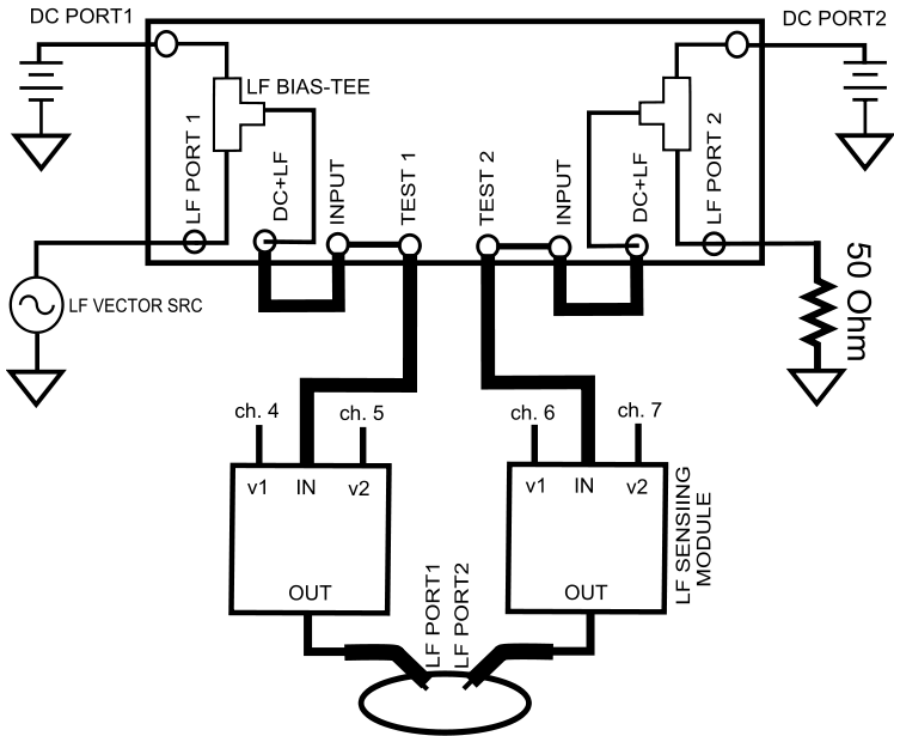

Figure 6-6 LF LSNA configuration for on-wafer low-frequency nonlinear characterization with 50 Ohm termination at the output port.

A.3 RF LSNA

In the following the test-set configurations for the calibration and the measurement mode are briefly described for the RF LSNA. Since details of the RF LSNA calibration and measurement are outlined in [A1] and in Chapter 2, they are not dealt in this appendix.

A.3.1 RF LSNA calibration mode

In calibration mode the input of the reflectometers is connected to PORT1-2. The same steps as in A.2.1.1 are executed for the RF hardware calibration. The switches of the test-set are controlled via software through a ribbon-cable plugged in a VXI rack. The latter also controls some of the hardware circuitry of the down-converter. Throughout the calibration procedure, the switches' either route the calibration signal (RF SRC IN) to PORT1-2 or terminate them with an internal 50

Ohm load. For on-wafer calibration, the input of the reflectometer at the input port is exploited as the auxiliary port to execute the absolute calibration.

A.3.2RF LSNA measurement mode

In measurement mode external signals can be injected at the input of the reflectometers either directly or through RF bias-tees to combine the RF signals with the DC voltages. For standard one- and two-tone test a CW RF source or a vector source are connected respectively to the RF input of the bias-tees (Figure 6-3) or directly to the reflectometers' input when DC is separate from the RF signals. The output port is passively terminated with a 50 Ohm load through PORT2.

A.4LF-RF LSNA

A.4.1Calibration

The LF and RF LSNA set-ups illustrated in Figures 6-2 and 6-3 are put together for the characterization of nonlinear DUTs with modulated excitations (Figures 6-4 and 6-5). The calibration procedure of the LF-RF LSNA is performed in three steps:

I. LF LSNA calibration by following the steps 1)-12) in A.2.1;

II. RF LSNA calibration as in [A1];

III. Alignment of the LF and RF calibrations.

In what follows, the calibration routine is outlined.

A.4.1.1 Separate LF and RF ports

In this situation, the set-ups in Figures 6-2 and 6-3 are connected as in Figure 6-4 and do not require any change in the hardware configuration, though they operate synchronously. The system is calibrated by following the steps 1) – 7) in A.2.1 for the LF LSNA. The same steps are followed for the RF LSNA calibration [A1]. Next, the alignment procedure is carried out, as will be explained in A.4.2.

A.4.1.2 Common DC/LF and RF ports

The system of Figure 6-5 is calibrated by following the steps 1) – 12) in section A.2.1 for the LF LSNA. The RF LSNA is calibrated as in [A1]. Finally, the alignment procedure is applied as described in the following section.

A.4.2RF and LF calibrations alignment procedure

As explained in section 2.3, a reference RF modulated signal is needed to estimate the delay difference between the RF and LF calibrations' coefficients. This reference signal can be generated by software and uploaded into an ESG. The uploaded signal has the same carrier frequency as the fundamental frequency of the RF calibration grid. The modulation frequency is set equal to 100 kHz. Both the RF signal and its in-phase component (I) are available on the front and rear panels of the instrument. It is important for a correct estimation of the delay difference that any additional delay due the ESG hardware and the cables connected to the instruments is also accounted for.

A.4.2.1 ESG and cabling delay characterization

The ESG internal hardware and the cables connected to the RF and I outputs add a delay between the RF and I signals as compared with the uploaded signal. This additional delay is here determined by making use of the LSNA down-converter hardware which actually can work down to DC.

A modulated signal with carrier frequency at 1 GHz and modulation frequency equal to 100 kHz is uploaded into the ESG. It is assumed here that the delay of the instrument and the external cables is independent on the carrier frequency. Afterwards, both the RF and the I signals are connected to the inputs of the down-converter and synchronously detected by two channels of the acquisition section, as in Figure 6-7. By comparison of the measured RF envelope and the I signal, the delay due to the internal hardware of the ESG and the external cables is estimated. For the model of the ESG used in this work (Agilent E4438C) and 1 meter coaxial cables, a delay of about 26 ns is extracted.

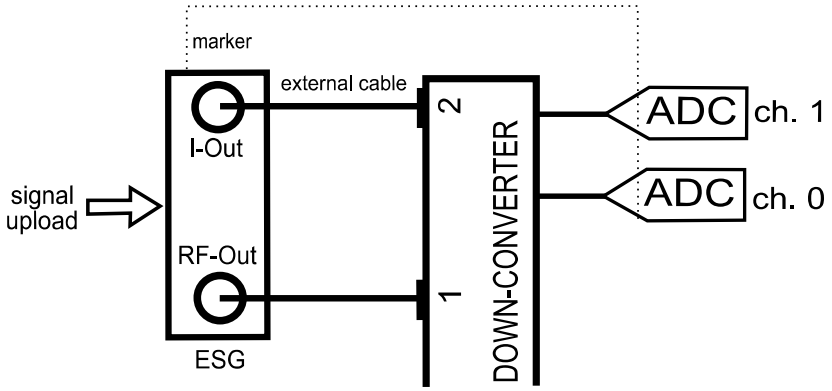

Figure 6-7 ESG outputs connected to the down-converter inputs to estimate the delay difference between the RF and I signals.

A.4.2.2 Alignment with separate DC/LF and RF ports

When the LF and RF ports are isolated from each other (see Figure 6-4), the measurement for the alignment procedure is performed with the set-up configured as in Figure 6-8. The ESG RF and I outputs are plugged to the input of the reflectometers and the LF sensing module at the output port, respectively. A 'thru' connects the LF PORT1-2 and RF PORT 1-2. The RF and the I signals are synchronously measured by an RF and LF channel, respectively. The signal acquisition is triggered by the signal 'marker' generated by the ESG and connected to the PXI frame. The measured LF 'v1' and RF 'b1' waveforms are firstly corrected with the calibration coefficients which include the delay difference. Next, the delay difference is computed by comparison of the corrected waveforms with the reference ones. As final step, the calibration coefficients are re-computed by taking into account the calculated delay difference, including also the delay estimated as in section A.4.2.1.

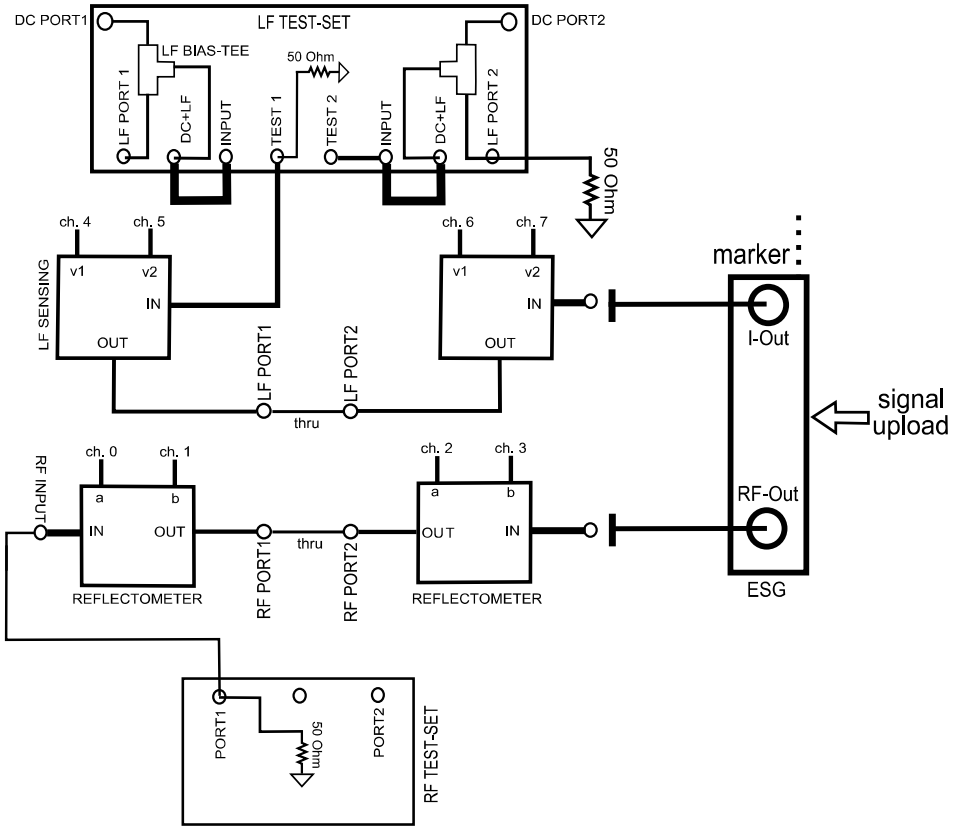

Figure 6-8 Set-up configuration for the evaluation of the delay between the RF and LF calibration coefficients with the DC/LF and RF ports physically separate.

A.4.2.3 DC/LF and RF ports at the same reference plane

The set-up is configured as in Figure 6-9 and the RF-Out and the I outputs are now alternatively applied to the input of the reflectometer at the output port. A ‘thru’ connects the input and output ports, and the signal acquisition is synchronous as explained in section A.4.2.2. The measured LF ‘v1’ and RF ‘b1’ waveforms are then corrected with the RF and LF matrices obtained after the RF and LF relative and absolute calibration routines. The corrected and delayed RF and LF waveforms are aligned with the reference signal generated by the ESG, including also the delay estimated as in section A.4.2.1. Finally, the calculated delay difference is straightforwardly removed from the misaligned correction coefficients.

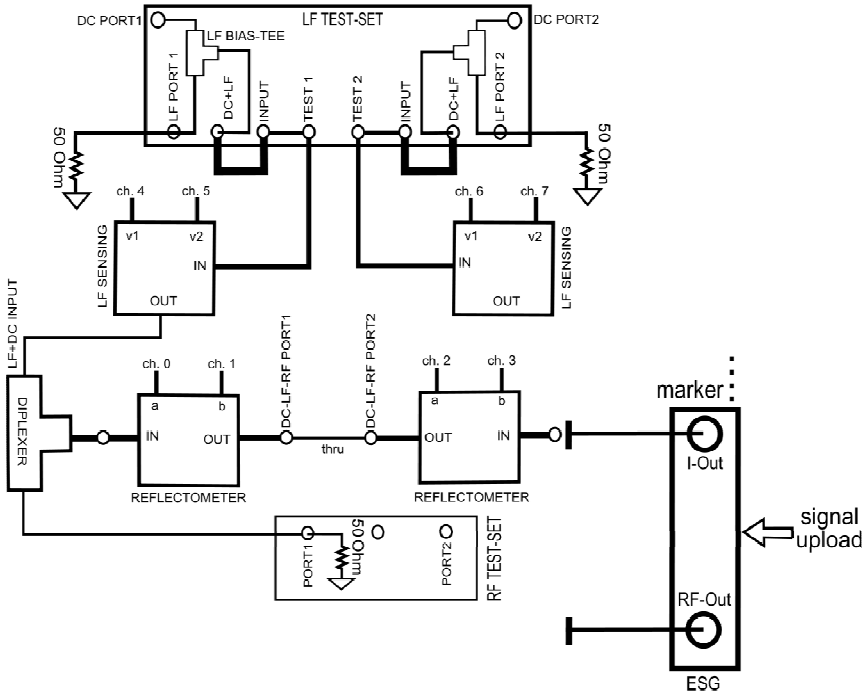

Figure 6-9 Set-up configuration for the evaluation of the delay between the RF and LF calibration coefficients with the DC, LF, and RF ports at the same reference plane.

A.4.3Measurement mode

The default measurement mode configuration of the LF-RF LSNA is depicted in Figures 6-4 and 6-5. That is the typical LF-RF LSNA configuration to perform the RF two-tone test with 50 Ohm termination at the RF output port and at the LF input and output ports. The same configuration can be exploited to acquire high-frequency information while changing the baseband impedance. The latter can be tuned either by replacing the 50 Ohm termination at the LF port with passive loads or by connecting an LF signal generator.

[A1] J. Verspecht, Calibration of a measurement system for nonlinear devices, PhD dissertation, Nov. 1995.

Curriculum Vitae

Gustavo Avolio was born in Cosenza, Italy, in 1982. In 2004 and 2006 he received the Bachelor (110/110 cum laude) and the Master degree (110/110) in Electronic Engineering at the University of Calabria, Italy. In 2008 he joined the TELEMIC division of the Department of Electrical Engineering (ESAT) of the KU Leuven to start the PhD research. His main interest focuses on the nonlinear characterization and nonlinear modeling of microwave solid-state active devices.

List of publications

Articles published in internationally reviewed journals

[J1] G. Avolio, D. Schreurs, A. Raffo, G. Crupi, G. Vannini, and B. Nauwelaers, "Waveforms-only based nonlinear de-embedding in active devices," *IEEE Microwave and Wireless Components Letters*, vol. 22, no. 4, pp. 215-217.

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[W2] G. Crupi, D. Schreurs, G. Avolio, A. Caddemi, A. Raffo, G. Vannini, “De-embedding: linear versus non-linear,” *European Microwave Week (EuMW) workshop on* “*From De-embedding to Waveform Engineering*,” pp. 1-24, Manchester, United Kingdom, 9 Oct. 2011.

[W3] G. Avolio, D. Schreurs, A. Raffo, G. Crupi, G. Vannini, B. Nauwelaers, “Nonlinear measurement techniques for the low- and high-frequency characterization of microwave active devices,” *Automatic RF Techniques Group Conference (ARFTG) workshop on* “*Nonlinear measurements to investigate memory effects of RF transistors and active devices,”* pp. 1-16, Clearwater, Florida, US, 30 Nov. - 1 Dec. 2010.

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Contributions in books chapters

I. Angelov, G. Avolio, and D. Schreurs, “Large-Signal Waveforms Based Transistors Modeling,” chapter in the book "Microwave De-embedding: from Theory to Application" edited by G. Crupi and D. Schreurs, Elsevier Academic Press. Accepted.