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(article begins on next page)

A 0.7mW 13b temperature-stable MASH $\Delta\Sigma$ TDC with delay-line assisted calibration

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Abstract—A 1-1-1 MASH $\Delta\Sigma$ Time-to-Digital Converter (TDC) with 6ps time resolution is implemented in 0.13 μ m CMOS. It achieves an ENOB of 13b and a wide input range of 100ns. The TDC exhibits stability within a temperature range of -20 to 120°C, which credits to the use of an on-chip bandgap reference and passive RC oscillators. A novel delay-line assisted online calibration technique is introduced to mitigate the skew error caused by the large comparator delay. The chip consumes only 0.7mW from 1.2V supply, and occupies 0.08mm² area (core).

I. INTRODUCTION

High resolution TDCs are widely demanded in digital PLLs, ADCs, and time-of-flight (TOF) measurement units. Existing methods to achieve sub-gate-delay resolution such as time amplification [1], local passive interpolation [2], and gated-ring-oscillator [3], suffer from process and temperature variation, which limit their effectiveness in harsh environments. By contrast, data converters which adopt the noise-shaping technique to achieve high resolution are highly immune to component mismatch. The technique has been successfully implemented in analog-to-digital conversion for years, which is well known as $\Delta\Sigma$ modulator. Some works brought the same principle into phase-domain data conversion, as in [4, 5], and achieved first-order and second-order noise-shaping, respectively. However, these phase-domain $\Delta\Sigma$ modulators are analog intensive approaches, and the phase information is converted back to the voltage-domain. As the technology scales down, this becomes less attractive due to the difficulty of achieving high-gain and wide-bandwidth analog blocks under strongly reduced supply but relatively unchanged threshold voltage. Moreover, their performances are highly relying on the linearity of the front-end phase detector, which practically limits the dynamic range of the input time signal.

A digital intensive third-order MASH $\Delta\Sigma$ TDC has been reported first in [6]. It measures a time signal by counting the periods of an oscillating clock generated by a RC oscillator, whose frequency is inherently tolerant to the PVT variation. The data conversion is mainly being processed in the time-domain, which benefits most from technology downscaling.

Fig. 1: Architecture of a 1-1-1 MASH TDC with delay-line assisted calibration.

Furthermore, there is no physical limitation for the TDC's input linear range, which makes it suitable for TOF application. The TDC is able to achieve an ENOB of 11b. However, it still suffers from skew error introduced by the comparator delay. A high speed threshold detection comparator and a high OSR of 250 are then required to guarantee its performance.

This paper describes an online calibration method to mitigate the skew error, which relaxes the high speed constraint on the comparator. Measurements among a wide temperature range have also been performed, proving the TDC's robustness.

II. THE 3RD-ORDER MASH $\Delta\Sigma$ TDC WITH CALIBRATION

The architecture of a 1-1-1 MASH TDC is shown in Fig. 1. The first and second stage have the same structure, where the third stage doesn't have the calibration unit. Each stage

Fig. 2: Timing diagram.

Fig. 3: Structure of the 10 stages delay-line calibration unit.

works as a relaxation oscillator, but enabled/disabled by the input time signal. It works as follows: In each stage, the time signal tin controls a current to charge one of the two capacitors during its active phase. When it exceeds the threshold voltage $VREF$, the comparator output becomes '1'. This reverses the state of the SR-latch, and triggers the oscillation. The phase of the clock $pcnt$, which refers to the residue voltage on the capacitor, is preserved between measurements, as illustrated in Fig. 2. The overall quantization error can then be described as $q[1]-q[0]$. The time signal for the next stage is generated by subtracting the quantization error from the input of the current stage. Third-order noise-shaping is obtained by cascading all three stages.

A. Skew Error in the MASH $\Delta\Sigma$ TDC

The skew error occurs when the stop signal arrives during the time the comparator enters its state-reversing phase, when $vinn$ or $vinp$ just exceeds $VREF$. A delay always exists before the comparator can make a final decision according to its input change. It is impractical to save all the intermediate states of the comparator when the system enters idle. So the output of the comparator will continue rising till its final state '1' even if the oscillation has been stopped. Therefore, when the next start signal arrives, the SR-latch will immediately reverse its state, and alternates the capacitor being charged. This will result in a change in the counting clock period and introduce extra skew error to the preserved quantization residue time. This error is shown by red lines in Fig. 2. According to simulation results, the delay of the comparator has to be limited within 200ps in order not to degrade the SNDR of the TDC, when an OSR of 50 is adopted.

Fig. 4: Schematic of the bandgap reference.

Fig. 5: Schematic of the comparator.

B. Delay-line Assisted Calibration

Fortunately, this skew error can be calibrated by using a coarse delay-line, whose structure is shown in Fig. 3. Each cell has a delay of 150ps. As one can see from Fig. 1, the RS-latch is controlled by the output of the calibration unit EN rather than tin , but both have the same 'stop' edge. LH , the complementary signal of tin , is sent to the delay-line. For the same situation described above, when the comparator's output becomes '1', the state of each delay cell will be sampled by its connected arbiter. For instance, if LH has passed through 3 delay cells, the states of all arbiters will be "1110...0". The switch connected to the third delay cell will also be closed, which charges sel to '1'. sel will be discharged only after the next start signal has also passed through the same delay cells as the stop signal, then activate EN . The resulting waveform on the capacitor is shown in the bottom axis of Fig.2 by blue lines. In this way, the skew error caused by the comparator delay is compensated at an accuracy of 150ps.

However, one problem might limit the effectiveness of the delay-line calibration method, which is the input-dependent delay of the comparator. When the input differential voltage to the comparator is very small, the comparator exhibits a much larger delay. And the relationship between the input voltage and comparator delay is nonlinear. As soon as the input differential voltage exceeds a certain level, which is 10mV in this case, the difference in delay becomes negligible compared to the minimum detectable delay time by the calibration unit.

In order to avoid this nonlinear behavior of the comparator, an arming comparator has also been added to control each main comparator. It has a different reference voltage $vtref$ which is slightly higher than that for the main comparator (10mV higher in this case). When the stop signal arrives, it compares the residue voltage with $vtref$. There are three different cases: (1) the residue voltage is smaller than $VREF$, (2) the residue voltage is larger than $vtref$, and (3) the

(a)

(b)

Fig. 6: Measured PSD with (a) 18kHz -20dBFS (b) 71kHz -60dBFS input.

residue voltage is larger than V_{REF} , but smaller than v_{tref} . In case 1, the main comparator isn't in its state-reversing phase, therefore no skew error will occur. In case 2, the main comparator has an input independent delay, and that can be calibrated by the calibration unit. In case 3, the output signal of the arming comparator will disable the input stage of the main comparator. The state of the main comparator will be held as '0' even when the actual input v_{inn} or v_{inp} exceeds V_{REF} . This avoids the comparator's nonlinear-large-delay state caused by very small input. Meanwhile, the introduced skew error due to this operation is tolerable by the TDC.

C. Circuit Design

An on-chip bandgap current reference [7] is implemented to provide $50\mu A$ charge current for each stage, as shown in Fig. 4. The reference voltage for the comparator is generated by $I_{REF} \cdot R$. Therefore, the frequency of the RC oscillator can be expressed as $I_{REF}/(V_{REF} \cdot 2C) = 1/(2 \cdot RC)$, which only depends on passive components. The oscillator is running at a frequency of 65MHz.

Fig. 5 shows the schematic of the main comparator. It has three stages. The input stage is a low-gain high-bandwidth preamplifier. It tracks the input, and makes fast decision as

Fig. 7: Dynamic range of the MASH TDC.

Fig. 8: Temperature stability test with a 41ns DC input (left axis) and an 18kHz -20dBFS sine input (right axis).

soon as the threshold condition is reached. The input differential voltage is then amplified and fed into the latch stage. A self-biased differential amplifier [8] is implemented as the output buffer stage. It consumes nearly zero static current, but has the ability to source and sink large currents. One comparator draws $30\mu A$ quiescent current from the supply, and has a total delay of 1ns. The arming comparator consists of a preamplifier and a clocked dynamic latch. It has the same preamplifier stage as the main comparator in order to minimize the mismatch between the two comparators.

III. MEASUREMENTS

A PWM signal, modulated by a sine wave, is employed to evaluate the performance of the TDC. The rising edge of the PWM pulse represents the start signal, where the stop signal is located at the falling edge. The carrier frequency is set to 10MHz, which turns to a full scale peak-to-peak input range of 100ns. Then for a bandwidth of 100kHz, the OSR is 50. Fig. 6a shows the output spectrum of the MASH TDC with an 18kHz 10ns_{pp} (-20dBFS) input. It shows an SNDR of 55.2dB and 6ps time resolution. It can be clearly seen that, without calibration, the large skew error caused by the comparator delay will introduce distortion and increase the baseband

TABLE I
COMPARISON OF STATE-OF-THE-ART TDCS WITH SIMILAR SPECIFICATIONS

	[1] JSSC08	[2] ISSCC08	[3] JSSC09	[5] CICC10	[6] ISSCC11	This work
Technique	Time Amplification	Loc. Passive Interpol.	Gated Ring Oscillator	Phase-domain $\Delta\Sigma$	Time-domain $\Delta\Sigma$	Time-domain $\Delta\Sigma$
Sample rate (MS/s)	10	180	50	156	50	10
Resolution (ps)	1.25	4.7	6	2.4	5.6	6
Bits	9	7	11	10	11	13
Meas. Range (ns)	0.64	0.6	12	3.2	20	100
Power (mW)	3	3.6	21	2.1	1.7	0.7
Core area (mm ²)	0.6	0.02	0.04	0.12	0.11	0.08
CMOS (nm)	90	90	130	90	130	130

Fig. 9: Die photo of the MASH TDC.

noise. A 71kHz 100ps_{pp} (-60dBFS) input is used for small signal measurements. A SNDR of 20dB and an ENOB of 13b are achieved. The results are shown in Fig. 6b.

Fig. 7 shows the dynamic range of the TDC. Input signals above -20dBFS are not available due to the limitation of the modulation depth of the test equipment. However, good consistency of the curve is predicted, since in a TDC system, the maximum input amplitude is only limited by the depth of the counter, which can be easily extended to avoid any overloading of the system.

The TDC has also been examined under different temperatures. As illustrated in Fig. 8, with a 41ns DC input, the total shift of the TDC's output is less than $\pm 1.25\%$ over a wide temperature range of -20 to 120°C, which shows a temperature coefficient of 176ppm/°C (7.2ps/°C) without any calibration. From 25°C to 120°C, this value is only 76ppm/°C. During the dynamic measurement, the SNDR of the TDC doesn't drop even when the temperature rises up to 100°C. The power consumption of the TDC core is 0.7mW, regardless of the magnitude of the input time signal.

IV. CONCLUSION

A 1-1-1 MASH $\Delta\Sigma$ TDC is presented with an additional delay-line calibration unit and an assisted 'arming comparator' for mitigation of the skew-error introduced by the delay of the main comparator in the RC oscillator. The TDC is fabricated in 0.13 μ m CMOS, and the die photo is shown in Fig. 9. The performance of the TDC is compared in Table I with state-of-the-art TDCs. It consumes only 0.7mW from a 1.2V supply, which is the lowest, and at the same time, it achieves the highest ENOB of 13b. A wide input range of 100ns has also been achieved. Moreover, the resolution of the TDC can be further improved by increasing the OSR, without any significant increase in power consumption.

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