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Organic complementary oscillators with stage-delays below 1 μ s

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Recently, complex circuits of organic thin-film transistors have been shown. The use of complementary logic can significantly ease the design of large integrated circuits. However, the performance of complementary logic in organic thin-film technology has not been able to equiva-

Over the past years organic thin-film transistors (OTFTs) have been routinely used in circuit designs of increasing complexity.^{1–3} Circuit speed of unipolar organic circuits is up to 1.5 kbit/s for 128 bit radiofrequency identification tags¹ and down to 120 ns stage-delay for single inverters.⁴ The circuits can operate at supply-voltages (V_{DD}) as low as 3 V.⁵ Because of the intrinsic limitations (e.g., static power consumption, design complexity) of the unipolar logic that is used in those designs, the development of organic complementary logic, in which hole-conducting p-type transistors and electron-conducting n-type transistors are integrated on one substrate, currently receives a lot of attention.^{6–9} However, inverter stage-delays so far are much larger than the best reports of unipolar inverters. The main reason for this is that integration of champion n-type and p-type materials in a single process flow is challenging, and in complementary logic the slower transistor dictates the overall speed. In this work, we have developed a process for C_{60} bottom-gate bottom-contact n-type OTFTs resulting in high-performance transistors that can be integrated with high-performance bottom-gate bottom-contact pentacene transistors. The resulting organic complementary thin-film technology can compete in terms of speed with unipolar thin-film technology.

To characterize the intrinsic performance of C_{60} as n-type semiconductor, we made reference top-contact devices as shown in Fig. 1. The gate dielectric is thermally grown SiO_2 . The source and drain contacts consist of LiF/Al (0.6 nm/100 nm) and are defined by a shadow-mask. We extract an electron mobility $\mu_e = 1.5 \pm 0.1$ cm^2/Vs and a threshold voltage $V_T = 4.7 \pm 0.1$ V, when the dielectric is treated with a thin layer of poly(alpha-methylstyrene) (PaMS, molecular weight: 850 k) deposited by spin-coating from solution in toluene (0.1 wt %). The reference device on bare SiO_2 in Fig. 1 demonstrates that the PaMS treatment causes an increase of the on-current by about three orders of magnitude, presumably due to reduced electron trapping. According to the literature, electron trapping is caused or en-

hanced by several factors,^{10–13} that can all be influenced by the presence of PaMS. Determination of the dominant mechanism for the observed improvement is out of the scope of this paper. This experiment mainly shows the excellent performance of C_{60} on PaMS. The shadow-mask technology however, does not permit to envisage true integration with a pentacene bottom-gate bottom-contact process.

Recently, bottom-gate bottom-contact C_{60} transistors were shown using Au electrodes with an adapted treatment of self-assembled monolayers (SAM) on the contacts.¹⁴ We use a similar yet different approach, compatible with our PaMS treatment of the gate oxide. The PaMS surface-treatment is applied on the gate oxide by spin-coating after the definition of Au contacts by lithography. To prevent the formation of an insulating PaMS layer on the contacts, we treat them with a SAM that repels toluene prior to the spin-coating of the PaMS layer. In our normal process, the appropriate SAM to repel toluene is a thiol with a fluorinated end-group.¹⁵ However, such a thiol increases the effective work-function^{16,17} of the metal contact, resulting in a higher barrier for carrier injection from Au into the lowest-

FIG. 1. (Color online) Transfer characteristics of bottom-gate top-contact n-type OTFTs produced by the evaporation of C_{60} on a PaMS-treated SiO_2 gate dielectric. LiF/Al contacts are evaporated through a shadow-mask yielding device of $W/L=2000/64$. The mobility values obtained are practically the same for samples that have not been annealed in UHV prior to semiconductor deposition ($\mu_e = 1.5 \pm 0.1$ cm^2/Vs , circles) as for those that have ($\mu_e = 1.4 \pm 0.1$ cm^2/Vs , triangles). Characteristics of a reference device that lacks the PaMS-treatment (dashed line) show the current increase provided by this treatment.

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FIG. 2. (Color online) Transfer characteristics of bottom-contact OTFTs [$W/L=5000/9$, structure in inset (b)]. The Au contacts are exposed to DSH vapor to guide the self-aligned surface treatment of the channel region by spin-coating. Before evaporation of C_{60} , some samples are subjected to a cure in UHV (filled triangles), while others are not (circles). The difference demonstrates the beneficial effect of the heat treatment. Moreover, when cured substrates are air-exposed before deposition of C_{60} , performance clearly decreases (empty triangles), suggesting the heat treatment mainly removes contaminants. Inset (a) shows an atomic force microscope image of 30 nm of pentacene grown on an equally treated bottom-contact structure (uncured). The growth difference observed proves PaMS has properly dewetted from the contacts.

unoccupied molecular orbital of C_{60} . Therefore, in the present work, we use an alkanethiol [more specifically, dodecanethiol (DSH)]. We verify, using standard pentacene transistors, in the inset of Fig. 2, that dewetting of PaMS in toluene from DSH-treated Au contacts effectively takes place.

Nevertheless, C_{60} n-type transistors perform poorly on DSH/PaMS treated bottom-gate bottom-contact structures as shown in Fig. 2. Very significant improvement is observed when the samples are cured for 4 h in ultrahigh vacuum (UHV) at 180 °C prior to deposition of the semiconductor. As shown in Fig. 2, the mobility on cured substrates is $\mu_e = 1.5 \pm 0.1 \text{ cm}^2/\text{V s}$, which is an improvement of over two orders of magnitude with respect to the uncured samples ($\mu_e = 0.010 \pm 0.006 \text{ cm}^2/\text{V s}$). Because the same curing step has no effect on the transistor characteristics of top-contact devices (Fig. 1), the curing is concluded not to affect the PaMS, but to be a necessary step for the DSH-treatment of the Au contacts. Furthermore, the reduced performance that is seen when cured substrates are air-exposed for 1 h before evaporation of C_{60} suggests that, more specifically, the curing step removes contaminants from the treated contacts. The static performance of C_{60} transistors with the presented treatment suffices for integration in a p-type process for the realization of organic complementary logic as we demonstrate below.

For the demonstration of organic complementary circuits, we photolithographically pattern Au source-drain contacts on a gate-stack that consists of Ti/Au (5 nm/25 nm) and a layer of 100 nm sputtered aluminum oxide. These contacts are first exposed to a solution of 10 mM pentafluorobenzenethiol. Subsequently, a thin layer of PaMS is applied to the channel region of the transistors by self-aligned spin-coating from solution in toluene. Next, to finish the p-type transistors, 30 nm of pentacene is evaporated in UHV at a rate of 0.25 Å/s and a substrate temperature of 68 °C. This

FIG. 3. (Color online) Transfer characteristics of both pentacene-based p-type (dashed line) and C_{60} -based n-type (full line) OTFTs after full integration in a process for complementary logic. The inset shows the subthreshold characteristics of seven OTFTs of both types on a log scale. All are bottom-gate bottom-contact devices ($W/L=140/4$) with sputtered aluminum oxide gate dielectrics. The high spread on n-type parameter values is attributed to the presence of contaminants in these n-types due to the etching of pentacene.

hole-conducting organic semiconductor is patterned in O_2 -plasma after applying, exposing and developing a water-soluble resist.¹⁸ The plasma-etch also removes the pentacene and the surface treatments from the contact and channel regions of future n-type transistors. Therefore, the surface treatments described in the former paragraph are at this point applied to the contacts and channels of future n-type transistors. Finally, C_{60} is evaporated at a rate of 0.33 Å/s with the substrate at room temperature after the previously described curing step in UHV. The resulting devices are characterized in a N_2 -glovebox. Despite all subsequent processing steps of the n-type transistors, the p-types show a mobility of $0.69 \pm 0.05 \text{ cm}^2/\text{V s}$ and a slightly positive threshold voltage of $0.3 \pm 0.1 \text{ V}$. N-type transistors show mobilities of $0.26 \pm 0.09 \text{ cm}^2/\text{V s}$ and threshold voltages of $4.1 \pm 0.7 \text{ V}$ (Fig. 3). We attribute this reduced performance (with respect to the former) to incomplete cleaning of the substrates during the etching of the pentacene.

In Fig. 4 we plot stage-delay values (t_d) as extracted from oscillator measurements for different supply-voltages (V_{DD}); t_d is lower than 1 μs at $V_{DD}=20 \text{ V}$. A recent overview¹⁹ of oscillator stage-delays in organic thin-film technologies shows that an intrinsic trade-off exists between V_{DD} -reduction and lowering t_d . Therefore, a technological improvement consists of moving the Pareto frontier of stage-delay versus V_{DD} , as does the presented technology. Some unipolar technologies^{20,21} offer lower stage-delays but only at significantly higher V_{DD} (70 V). Technologies operating at lower V_{DD} all show higher stage-delays. The lowest stage-delays (3 μs) demonstrated so far with organic complementary technology⁸ required very high supply-voltages (100 V). Finally note that the reliability of the extracted stage-delays is reflected in the rectangular shape of the oscillator waves that were measured (inset of Fig. 4) as well as in the fact that a comparable stage-delay value could be extracted for oscillators that consist of 5 (open symbols in Fig. 4) and 19 stages (filled symbols in Fig. 4).

In conclusion, we show in this paper that cured

FIG. 4. (Color online) Microscope picture of an oscillator of 19 complementary inverter stages with $W_n=2 \cdot W_p=280 \mu\text{m}$ (a). The measured output voltage vs time of such an oscillator at $V_{DD}=20 \text{ V}$ (b). Average stage-delay for oscillators (c) vs the relative size of n-type transistors with respect to p-type transistors at $V_{DD}=10 \text{ V}$ (circles), $V_{DD}=15 \text{ V}$ (squares), and $V_{DD}=20 \text{ V}$ (triangles). The reliability of the measured values is confirmed by the fact that oscillators of five stages (empty symbols) show about the same stage-delay as those of nineteen stages (filled symbols). An optimum relative size exists for the n-type transistors with respect to the p-type as is expected for complementary technologies. The inset of (c) shows the circuit schematic of these ring-oscillators.

alkanethiol-treated Au contacts allow bottom-contact C_{60} transistors with a performance comparable to top-contacts with LiF/Al. By integration of these transistors in a p-type pentacene process, we demonstrate an organic complementary technology that permits to operate circuits at speeds that are higher than for most current unipolar OTFT technologies, i.e., stage-delays below $1 \mu\text{s}$ were measured at a supply-voltage of 20 V .

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