Low-cost CMOS-based receive modules for 60 GHz wireless communication

Piet Wambacq[1,3], Kuba Raczkowski[1,2], Valéry Ramon[1], Alexander Vasylchenko[1,2], Amin Enayati[1,2], Michael Libois[1], Jonathan Borremans[1], Karen Scheir[1,3], Stephane Bronckers[1,3], André Bourdoux[1], Bertrand Parvais[1], Bob Verbruggen[1,3], Steven Brebels[1], Wim Van Thillo[1,2], Christophe Pavageau[1], Bart Nauwelaers[2], Guy Vandenbosch[2], Walter De Raedt[1], Charlotte Soens[1]

[1]IMEC, Belgium
[2]ESAT, Katholieke Universiteit Leuven, Belgium
[3] Vrije Universiteit Brussel, Belgium

Abstract— **To enable mass-market applications based on short-range wireless communication around 60 GHz at datarates above 1 Gbps, cheap implementation technologies are needed. The radios for these applications often use antenna arrays with beamforming to improve the link budget. This work discusses the state-of-the-art on CMOS beamforming architectures and describes the different parts of a wireless link that is built around a four-antenna array on a PCB that also contains 45nm digital CMOS receiver ICs with beamforming capabilities.**

Keywords-CMOS, 60 GHz, mm-wave, phased arrays.

I. INTRODUCTION

The availability of an unlicensed band of 7GHz around 60GHz together with the ability of modern downscaled silicon-based technologies (ultra deep submicron CMOS, SOI, BiCMOS) to handle mm-wave signals has fueled a lot of research in the silicon IC design community to come up with 60GHz building blocks [1-4] and radios [5-9] that often use beamforming to improve the wireless link budget.

CMOS is obviously the most viable candidate to be used in future mass market consumer products, since it has proven to be fast enough and it allows for very complex flexible transceivers. Besides the IC technology, the technology for the antenna and the antenna interface should be cheap as well. In this work we demonstrate a beamforming receiver module based on a mm-wave receiver IC in 45nm digital CMOS. The functionality of the module, which contains two such ICs in a low-IF receiver, as well as four antennas on a PCB laminate and a waveguide to PCB transition, is demonstrated experimentally in a setup that emulates a wireless communication around 60 GHz. Before discussing the receiver module and the setup in Section III, Section II gives an overview of beamforming architectures realized in CMOS.

II. BEAMFORMING ARCHITECTURES

Beamforming in the receiver requires a programmable delay or phase shift followed by signal combination. In the transmitter the signal is split and then a phase shift or delay is applied to the different antenna paths. To minimize the duplication of functional blocks over the antenna paths, one could perform these operations as close as possible to the antenna, right after the low-noise amplifiers (LNAs) in the receiver, and just before the power amplifiers (PAs) in the transmitter. A programmable phase shift at RF can be made for example by first generating a quadrature version [7][10] of the RF signal after which the in-phase version (I) and the quadrature version (Q) are combined. Indeed, with a signal in I-Q format, one can make new in-phase and quadrature components I' and Q' that are phase shifted over an angle φ using

$$\begin{aligned} I' &= \cos(\varphi) I - \sin(\varphi) Q \\ Q' &= \sin(\varphi) I + \cos(\varphi) Q \end{aligned} \quad (1)$$

The two-antenna receiver demonstrated in [7] using a 65nm technology is based on this idea. With two LNAs, two RF phase shifters and a signal combiner this receiver consumes 78 mW per antenna paths with a power gain of 10 dB and a noise figure of 7.2 dB. The 45nm CMOS two-antenna receiver described in Section III.A is also based on RF phase shifting. It consumes less power at the expense of a larger noise figure. However, phase shifting and signal combination or split operations at mm-wave frequencies are hard to implement in bulk CMOS without a significant performance loss (insertion loss, increase of noise figure, …). Moreover, operations on signals at these frequencies are sensitive to small parasitics from on-chip interconnect and transistors, and any modeling error on these parasitics already yields a considerable change in the circuit performance at mm-wave frequencies.

Another phase shift approach is realized by mixing the signal in the different antenna paths with a phase shifted replica of the local oscillator (LO) signal. This has already been demonstrated in 90nm CMOS with a two-antenna receiver [9]. In this way the lossy phase shift operation is removed from the signal path. This LO phase shifting is less susceptible to amplitude variations and gives a limited phase noise degradation in the LO signal as long as the LO swing is kept high enough. An extension of the two-antenna receiver of [9] to four antennas in 45nm digital CMOS has been simulated. It is a direct downconversion architecture (see Figure 1. uses the LNA-mixer section described in [1] and the 56-67GHz PLL from [2]. The phase selectors are similar to the ones used in [9]. The four outputs from the quadrature VCO of the PLL are distributed to the four antenna paths via buffers (see Figure 1.) that can drive long transmission lines and two identical subsequent buffers that can again drive similar transmission

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lines and a load (next buffering stage or the phase shifters). The signal combination is performed at baseband by summing the output currents from the mixers. Simulations on this receiver (including layout parasitics) in 45nm digital CMOS give a noise figure at the output of the channel selection filter of 8dB per antenna path (including downconversion and signal combination) with a 26dB conversion gain and a total power consumption of 307mW (including frequency synthesis and LO distribution).

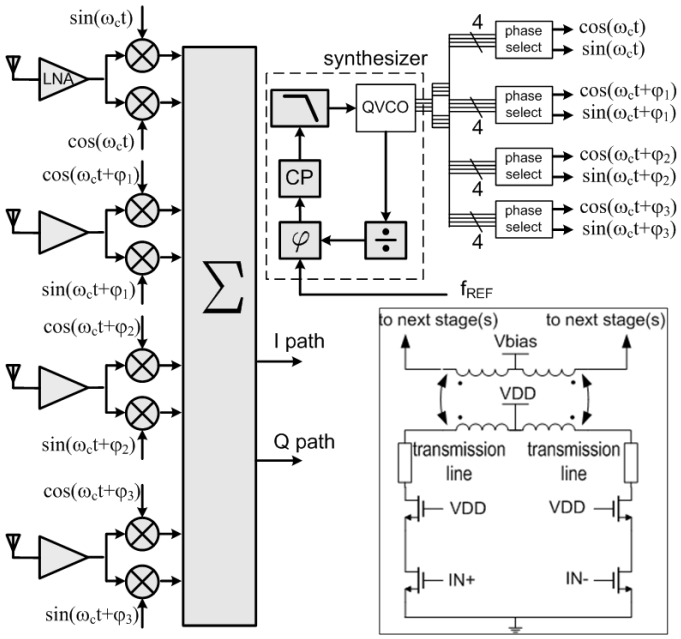


Figure 1. Receive architecture with phase shifting in the LO path. The inset shows the buffer used in the distribution of the LO (both the I and the Q path).

While in the LO phase shifting architecture signal combination has been moved to baseband, one could go one step further and also perform phase shifting at baseband using equation (1). This idea has been demonstrated in the direct upconversion transmitter from [8]. The advantage of baseband phase shifting is its low area consumption as no inductors are needed and a lower sensitivity to small parasitics of a few femtofarads or picohenries.

III. WIRELESS LINK WITH FOUR ANTENNAS

A wireless link (see Figure 2.) has been made with a four-antenna receiver that uses two 45nm CMOS receiver ICs in which beamforming at RF is implemented. These two ICs are mounted on a printed circuit board (PCB) made on a Nelco 4000-12 substrate. The PCB also contains four 60 GHz patch antennas and two commercial GaAs MMIC LO buffers. The LO signal is made with a frequency multiplier that is fed to the LO buffers via a transition from waveguide to microstrip and a power divider. The transmitter is built around an Arbitrary Waveform Generator (AWG) and a commercial 60GHz quadrature mixer. After upconversion by the mixer, the signal is amplified and sent through a coupler to a horn antenna. A picture of the link and a zoom on the receiver module are shown in Figure 3. Figure 4.

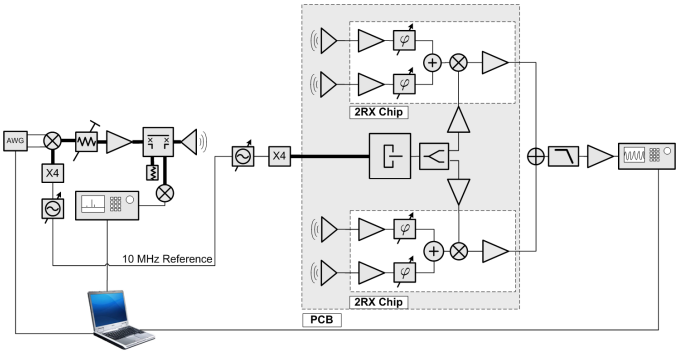


Figure 2. Setup of a 60 GHz link containing a module on a PCB laminate.

A. *Two-antenna receiver IC in 45nm CMOS*

The architecture of the two-antenna receiver IC designed in a digital low-power 45 nm CMOS technology is shown in Figure 7. . The LNA and mixer are described in [1]. The RF phase shifting is realized in two steps before downconversion. First, a quadrature all-pass filter (QAF), similar to the one of [10], generates two differential RF signals in quadrature. Secondly, 360° phase interpolation is achieved based on equation (1). The two paths' signals are then combined at the outputs of the phase selectors, before the mixer. This has two advantages: a combiner circuit is no longer necessary and only one mixer is required. The performance of the RF phase shifting is measured on the standalone IC, using off-chip, manually adjustable waveguide phase shifters. A change in the phase shift of the on-chip phase shifters influences the amplitude of the combined signal, which reaches a minimum when the signals at the output of the two phase shifters have an opposite phase (see Figure 8.).

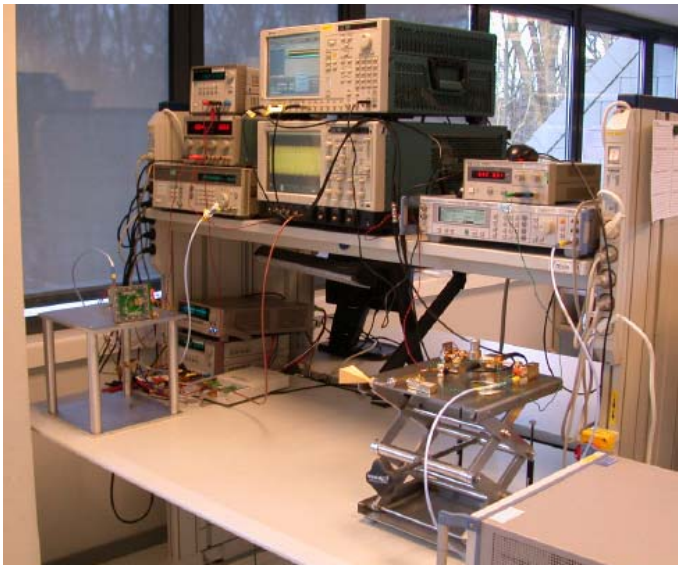


Figure 3. Picture of the wireless link from Figure 2.

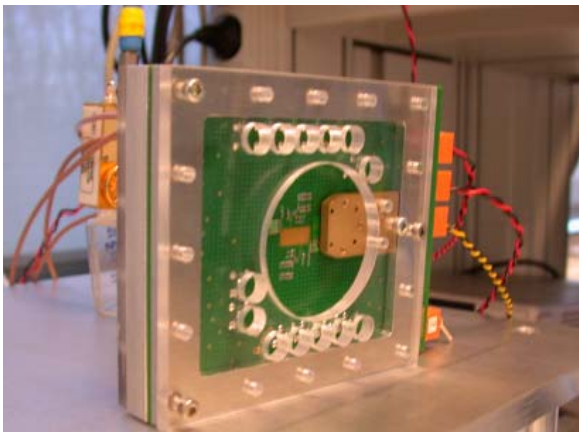


Figure 4. Detail of the wireless link: receiver.

The measured conversion gain of the receiver IC is around 15dB with a noise figure between 14 and 20dB from 55 to 63GHz with an IF frequency up to 1GHz and a power consumption of 60mW. The high noise figure of the receiver IC is due to the loss in the phase shifter and to the mismatch between the resonance frequencies of the different LC tanks used in the RF part of the chip. The many signal operations performed at mm-wave frequencies, each time requiring resonant circuits to boost the voltage swing, make the architecture sensitive to small parasitics and hence subject to large process tolerances. Therefore, architectures that perform a minimal amount of operations at mm-wave are preferred.

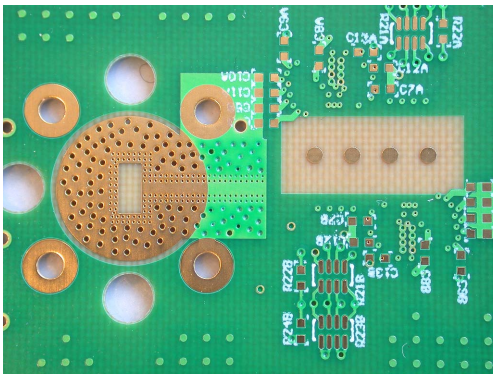


Figure 5. Detail of the receiver PCB : antennas and backside of the waveguide to microstrip transition.

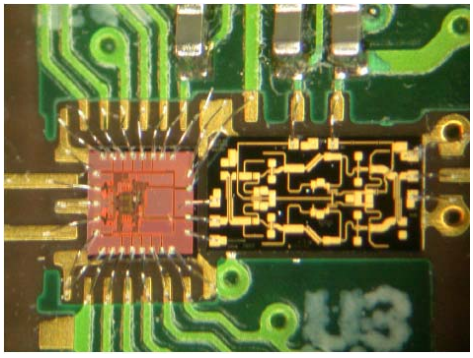


Figure 6. Detail of the receiver PCB: two-antenna receiver chip and MMIC LO buffer.

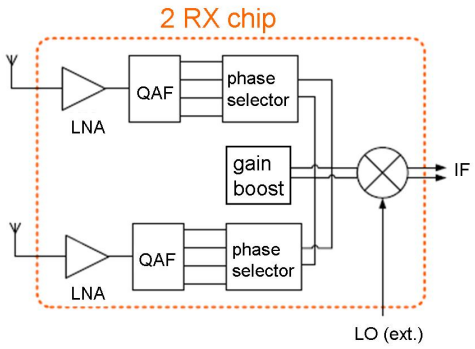


Figure 7. Architecture of the two-antenna receiver IC in 45nm CMOS.

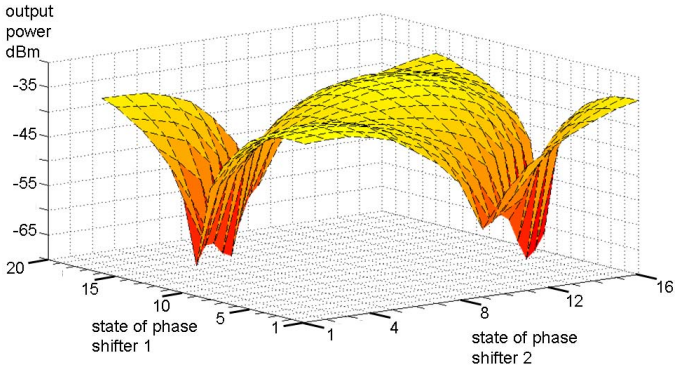


Figure 8. Measured power of the combined signal after downconversion, as a function of the settings of the two variable phase shifters.

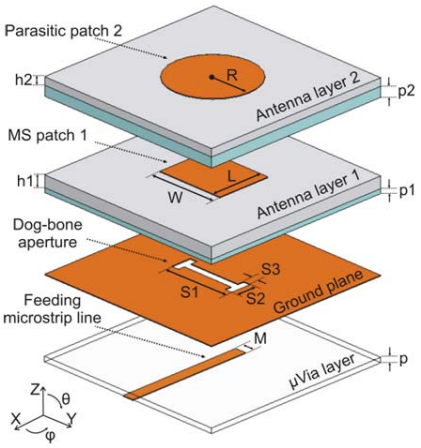
B. *Antenna array*

An array of four patch antennas has been realized on the PCB stack that is composed of several Nelco N-4000-12 core layers and prepreg layers. The antenna is a stacked patch configuration with a rectangular patch on antenna layer 1 and a circular patch on top of the antenna layer 2 (see Figure 9.). A size of the matching stub of the microstrip line has a length of 530 µm. It stretches from the center point of the ground plane aperture until the end of the microstrip line. To increase the bandwidth of the slot antenna, the slot width is increased symmetrically from the slot's center to either end, to provide of dog-bone slot configuration. The dog-bone slot has a main width of 90 µm. The measured antenna gain of one element is shown in Figure 10. . It reaches 6 dB at 61 GHz. The gain of the antenna array is 7 dB, which is constrained by losses in the feeding network. Moreover, the array reaches maximum gain between 50 and 55GHz also due to array's feeding network better matching at these frequencies.

C. *Measurements on the link*

The wireless 60GHz link uses Matlab both to transmit the digital data streams (compliant with the IEEE 802.15.3c standard) and to postprocess the received data (via in-house baseband algorithms). Some parameters of the link are given in Figure 11. The link can sustain a bit rate of at least 1.25Gbits/s (QPSK modulation can be used) with an acceptable bit error

rate (between 10^{-5} and 10^{-4}, uncoded) up to a range (distance between transmitter and receiver) of at least 1 meter. Further, the effect of beam steering can be clearly seen when the settings of the on-chip phase shifters are adapted to the angle of incidence of the signal that is transmitted via the horn antenna (see Figure 11.).



Dimension	value (μm)
h1	150
h2	100
P	75
p1	49
p2	130
L	710
W	850
R	550
M	150

Figure 9. Buildup of one antenna element.

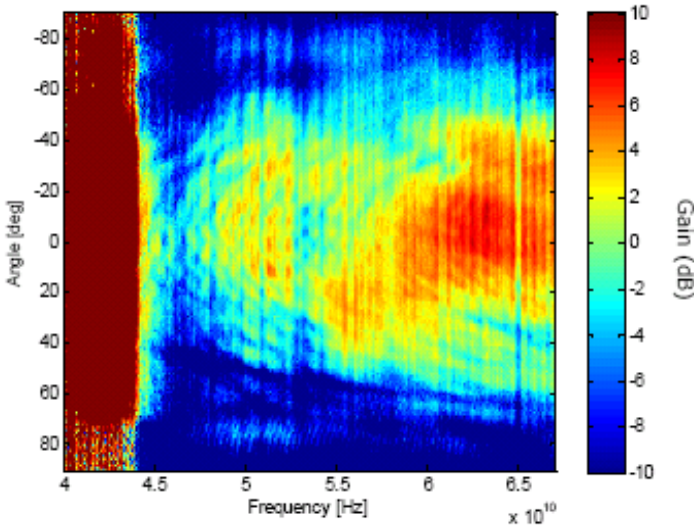
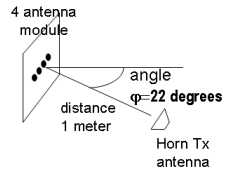


Figure 10. Measured antenna gain in the H-plane.

IV. CONCLUSIONS

In a few years, consumer products for high-datarate communication at mm-wave frequencies are expected to conquer the market. These will most probably be based on CMOS as this allows for a highly complex transceiver at an affordable price. Beamforming architectures are emerging to control antenna arrays which are used to improve the link budget. The coming years' research in this domain will have to focus on lowering the power consumption of the demonstrated prototype circuits and on the baseband circuitry that needs to have a high bandwidth to deal with the high datarates required for wireless communication at datarates above 1 Gbit per second.



Parameters	Values
Carrier frequency	57 GHz
IF (low-IF receiver)	500 MHz
RF bandwidth	1.0417 GHz
Symbol rate	833.3 Msymbols/s
Receiver sampling rate	2.5 GHz
Channel coding	no
Tx antenna gain	23 dB
Power of transmit signal	around 8/9 dBm
Preamble duration	3.072 μs
Payload duration	15.437 μs

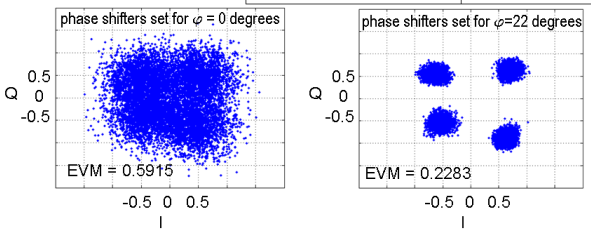


Figure 11. Measured constellation diagrams for QPSK data with the settings of the link given in the above table. The error vector magnitude (EVM) decreases significantly when the state of the phase shifters corresponds to the angle of incidence φ which is 22 degrees in this case.

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