22.5 50-to-67GHz ESD-Protected Power Amplifiers in Digital 45nm LP CMOS

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Research in recent years has shown that downscaled CMOS is a serious technology candidate to implement transceivers for high-data-rate wireless communication around 60GHz [1,2]. A low-cost implementation is the combination of the digital part with the transceiver onto a single chip. The complexity of the digital part demands a very advanced CMOS technology, such as 45nm low-power (LP) CMOS. Although this technology features a high maximum f_T , above 200GHz, the back-end-of-line (BEOL) metallization layers are thinner than in less-advanced technology. This implies a lower quality factor for the passive components and a lower intrinsic ESD robustness due to a higher sheet resistance of the metal layers. These restrictions, together with the limited power capabilities of CMOS make the design of mm-wave power amplifiers (PAs) more challenging [3,4].

In this paper, the first mm-wave PAs in 45nm LP CMOS (Fig. 22.5.1) with state-of-the-art values for output power and with adequate ESD protection is demonstrated. The first of the two PAs to be described consists of two common-source (CS) stages, together with matching networks at the input, output and between the stages. The second PA uses the same interstage matching network and is constructed in a push-pull (PP) configuration. To achieve a differential push-pull operation, a novel center-tapped transformer is used. Moreover, the transformer also provides the output matching of the push-pull PA. Both circuits are fully ESD protected in the RF path and in the bias network. Operated at 1.1V, these amplifiers provide a wideband 1dB compression point (P_{1dB}) and saturated (P_{sat}) output power within the 50-to-67GHz band. Moreover, the push-pull PA is the first reported to achieve a P_{1dB} compression point of +11dBm in digital CMOS.

To design the PAs a load-line approach is first applied to determine the approximate impedance transformation ratio of the output networks. Secondly, load-pull simulations together with classical matching techniques are applied to design and verify the output matching. After that, to increase the low gain of the oversized power transistor in the output stage, a preceding stage is added together with an interstage matching network. The interstage matching is applied in such a way that the first stage is matched for maximum output power, but the second stage is matched for optimum gain. Finally, input matching is realized together with an ESD protection inductor. The designs have been optimized for maximum delivered power rather than for maximum efficiency, yielding an output transistor with a width of 192 μ m in both designs.

Matching circuits have been implemented with lumped elements (spiral inductors and metal-oxide-metal (MOM) capacitors) rather than with transmission lines which would require a larger area. S-parameters for these lumped elements have been determined with Ansoft HFSS. For the push-pull amplifier a novel transformer structure is developed (Fig. 22.5.1). This structure allows the creation of a two-turn, two layer spiral without any need for over- or under-passes. This is desirable as the available digital CMOS technology has only two thicker metal layers and five very thin metal layers underneath, which are not suitable for RF applications. The transformer has tracks with a width of 3 μ m and its size is 32 $\times$ 32 μ m². The simulated and measured performances of this transformer show a coupling factor of 0.7 and an insertion loss of 1.1dB at 60GHz.

ESD protection is provided for all bond pads. Protection of the supply pads consists of a standard I/O ring (including a power clamp) provided by the chip manufacturer. The input and output pads are protected using shunt inductors [5]. The role of these inductors is twofold. First, they resonate out part of the capacitance of input/output pads. Secondly, because of their rather small inductance (e.g. 100pH) these inductors behave as a short circuit for relative-

ly low-frequency ESD events. In the push-pull amplifier the primary windings of the transformers play the role of this shunt inductor. Thanks to these ESD protection components both of these circuits show immunity to ESD HBM events up to 5.3kV at the input port. The protection level for HBM pulses at the output is 5.5kV for the single-ended PA and 5.3kV for the push-pull PA. The ESD measurements have been performed in gnd-/RFpin+ configuration only, which is the worst case for these circuits. The supply pads have been protected with standard ESD protection components of the foundry.

The amplifiers have been fabricated using a low-power P1M7 45nm bulk CMOS LP technology. Micrographs of both amplifiers (Fig. 22.5.7) show a low active area of the amplifiers (290 $\times$ 100 μ m² and 430 $\times$ 130 μ m²).

Figure 22.5.2 shows the measured values for P_{1dB} and the maximum output power (P_{max}) of both PAs. Direct measurement of saturated output power (P_{sat}) was not possible due to limitation of the measurement equipment. Nevertheless, the achieved peak P_{1dB} is +8.4dBm and +11dBm for the CS and PP PA, respectively. Measured P_{max} values are 10.6dBm and 13.8dBm for the CS PA and PP PA, respectively. Both P_{1dB} and P_{max} only vary within 1dB over more than 15GHz around 60GHz (Fig. 22.5.2). A two-tone measurement has been performed with a center frequency of 60GHz and tone separation of 5, 10, and 100MHz (Fig. 22.5.3). The output third-order intercept point is +12.5dBm for the CS PA and +17dBm for the PP PA. S-parameter measurements performed with a 110GHz VNA show that the small-signal gain of both amplifiers is narrowband with a maximum of 5.8dB at 52GHz for the common-source amplifier and 9.3dB at 47GHz for the push-pull amplifier (Fig. 22.5.4). The input matching is better than -10dB from 44.5GHz to 65GHz for the CS PA and from 49GHz to 67.5GHz for the push-pull PA. S-parameter-based stability calculations show unconditional stability of both amplifiers: the stability factor K is always above 6 for the CS amplifier and above 9 for the PP amplifier. At 1.1V the CS PA and the PP PA consume 70mA and 125mA, respectively. This corresponds to a peak drain efficiency of 11% and 13% and a peak PAE of 6.5% and 7%, respectively, as shown in Fig. 22.5.5.

Compared to state-of-the-art (Fig. 22.5.6), the push-pull PA obtains the highest P_{1dB} and P_{max} . As limited RF power of the measurement setup made P_{sat} measurements not possible, we compare the P_{sat} of previous designs with our P_{max} . The wideband aspect of this PA demonstrates its potential for use in high-data-rate communication in the bands allocated in the draft standards IEEE802.15.3c and Ecm TC48, which worldwide cover the range from 57 to 66GHz.

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Figure 22.5.1: Schematics of the PAs and the view of the transformer used in the push-pull PA. The width of each transistor is indicated.

Figure 22.5.3: Measured two-tone performance and extrapolated third-order-intercept points.

Figure 22.5.5: Measured gain, output power, drain efficiency (η_D) and PAE of the amplifiers at 60GHz.

Figure 22.5.2: Measured maximum output power (P_{max}) and 1dB compression point power (P_{1dB}) of the PAs. The roll-off for frequencies higher than 65GHz is caused by measurement equipment limitations.

Figure 22.5.4: Measured S-parameters of the PAs.

Author	Technology	P1dB [dBm]	Psat [dBm]	Gain [dB]	max PAE [%]	Supply Voltage [V]
Pfeiffer et al., JSSC 2007	0.13μm SiGe	13.1	20	18	12.7	4
Yao et al., JSSC 2007	90nm CMOS	6.4	9.3	5.2	7	1.5
Chowdhury et al., 2008 [1]	90nm CMOS	9	12.3	5.5	8.8	1
Suzuki et al., 2008 [2]	90nm CMOS	8.2	10.6	8.3	-	1.2
Tanomura et al., 2008 [5]	90nm CMOS	10	11	14.3	8.2	1
This work CS	45nm LP dig. CMOS	8.4	10.6	5.6	6.5	1.1
This work PP	45nm LP dig. CMOS	11	13.8	6	7	1.1

Figure 22.5.6: Performance summary and comparison of recently published 60GHz power amplifiers.

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Figure 22.5.7: Micrograph of the common-source PA (left) and push-pull PA (right).