A 100 GHz Transformer-Coupled Fully Differential Amplifier in 90 nm CMOS

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Abstract — This paper proposes differential design techniques for W-band CMOS applications. Transformers are used as passive matching circuits, which provide numerous advantages compared to traditional matching circuits. Stabilization and gain improvement of the differential pair is achieved by a wideband neutralization technique. These techniques are combined in a fully differential amplifier which is successfully measured. To our knowledge, this is the first fully differential 100 GHz CMOS amplifier.

Index Terms — Differential Design, mm-Wave, CMOS, integrated transformer, MOS neutralization, W-band.

I. INTRODUCTION

Today's wireless communication systems typically operate at relatively low frequencies. Carrier frequencies below 10 GHz are common, resulting in limited channel bandwidth. The demand for wireless 5 to 10 Gbps data rate systems will increase rapidly in the near future. But current wireless systems are not able to support these high data rates due to their limited bandwidth [1]. Today's wireless LAN standards offer data-rates of 54 Mbps up to 600 Mbps if multiple in, multiple out antenna technologies, complex beamforming and channel aggregation are applied [2]. The solution for this bandwidth problem can be found in the field of mm-wave applications. At mm-wave frequencies much higher bandwidths (2-10 GHz bandwidth is not unusual) are available which in turn can support gigabit wireless systems [3]. Other mm-wave applications can be found in the imaging sector for medical or security purposes or in radar and guiding applications like car radar or airplane landing guidance [4]. All these applications require a high performance, low cost implementation. Thanks to the high integration level, this can be achieved in CMOS. Despite the advantages of the CMOS process, the analog performance at mm-wave frequencies is limited. The integration of digital and analog circuits on the same substrate also leads to increased substrate noise. Adequate modeling and simulation of passive circuits is becoming a necessity due to electromagnetic radiation and the lack of a good ground definition.

In this paper design solutions for the high frequency active device performance (Section II) in combination with new high frequency passive devices (Section III) in a 90 nm

CMOS technology are proposed. The ground definition and substrate coupling problems can be solved by using fully differential circuits which in turn also creates the opportunity of designing new active and passive device topologies. The design and measurements of a fully differential 100 GHz amplifier in a 90 nm CMOS process are described in section IV. In this amplifier the design techniques proposed in the other sections are adopted to achieve high gain at high frequencies and full range stability.

II. ACTIVE DEVICES

Although the operating frequency of mm-wave circuits approaches the f_t and f_{max} , active circuits can still be designed by using circuit techniques which enhance the gain at these high frequencies. The behavior of a 15 μm 90 nm nMOS transistor is depicted in figure 2. At frequencies lower than the stability break point (75 GHz for 3 μm fingerwidth and 130 GHz for 1 μm fingerwidth in figure 2), the gain of the device is described by the G_{msg} or Maximum Stable Gain. In this region the device is conditionally stable. This means that for certain load impedances, such as complex conjugate input and output matching, the device will oscillate. Stabilization is achieved by introducing losses such as mismatch or resistive losses. At frequencies beyond the stability break point the device becomes unconditionally stable which results in a faster roll-off of the gain curve. The position of the stability break point is mainly a function of the parasitic gate resistance. An increase of this resistance, for example by increasing the fingerwidth, results in a more stable device over a wider frequency range. However, this also leads to a lower gain at higher frequencies. A device with a lower gate resistance (smaller fingerwidth) can thus provide more gain at higher frequencies. The first 2 curves of figure 2 show this effect for a transistor with a constant W/L. Decreasing the fingerwidth from 3 μm to 1 μm leads to an increase of the the stability break point from 75 GHz to 130 GHz.

In the conditionally stable region the gain is limited by the internal feedback of the transistor. The problem is the

gate-drain parasitic capacitance which creates a feedback loop. This internal feedback can be neutralized by connecting a negative capacitor in parallel with the original one so that the resulting feedback becomes smaller. The negative capacitance can be achieved by cross-coupling a capacitor between gate and drain in a differential pair (Figure 1). This is another benefit of using differential circuits at these high frequencies. Another advantage of this neutralization technique is the increase in stability performance without introducing extra losses, leading to a higher stability over a wider frequency band without losing gain. This also simplifies the design of the input and output matching networks. The effect of this neutralization technique is depicted in figure 2. Clearly, at 100 GHz the gain is improved with about 3 to 4 dB and the stability break point is pushed to an even lower frequency (65 GHz) than the original one (75 GHz).

The cross-coupled capacitors are inactive nMOS transistors (Figure 1). MOS capacitors are chosen here to overcome mismatch problems with the active devices of the differential pair due to process variations. If the cross-coupled capacitor is larger than the parasitic one of the active device, the stability performance of the complete differential pair is decreasing so oscillation can occur again at certain frequencies. To create a save stability margin, the MOS capacitors are approximately 20 % smaller than the active devices.

Fig. 1. Neutralized differential pair.

High gain at high frequencies can thus be achieved by reducing the fingerwidth which in turn results in a lower gate resistance, and gate-drain capacitor neutralization. For the 90 nm CMOS process, gain values of approximately 9 dB can be reached for a single nMOS transistor at 100 GHz (Figure 2).

III. PASSIVE DEVICES

Accurate mm-wave impedance matching networks are a must to create a conjugate match at input and output to

Fig. 2. Gain and stability approval by R_g reduction and C_{gd} neutralization.

maximize the power gain. Typical matching circuits at 100 GHz are build from bulky transmission lines [5]. Lumped element matching with capacitors and inductors is gaining importance, resulting in a reduced chip area [6], [7]. Using differential circuits, new matching circuit topologies can be obtained. One of the most important differential matching circuits is the transformer [8]. Even at mm-wave frequencies its performance is remarkably good. On top of this, the circuit can act as an impedance transformer and DC-blocker between different stages. DC-biasing can be connected at the center tap of the transformer which takes away the need for large inductors or transmission lines and coupling capacitors. The G_{max} of a planar transformer (Figure 3) is depicted in figure 4. At 100 GHz a minimal loss of approximately 1.1 dB can be reached.

Fig. 3. 3D view of an integrated planar 1:1 transformer.

The loss of the transformer decreases with frequency up to the point where the effect of self resonance becomes important. At this point the loss reaches a minimum. For this particular transformer, the SRF (self resonance frequency) is situated at relatively high frequencies due to the planar design. By altering the dimensions of the transformer, it can be optimized for coupling factor, SRF or impedance matching. The impedance transformation ratio can be adjusted by changing the dimensions and number of inner and outer windings. This also alleviates the need for extra series or parallel matching circuits. The simulations of the transformer are performed in the 2.5D finite element simulator Momentum. Good agreement between measurements and simulations is achieved (Figure 5).

Fig. 4. Transformer performance.

Fig. 5. Transformer measurements vs. simulations.

IV. AMPLIFIER MEASUREMENT RESULTS

A fully differential 6-stage transformer-coupled amplifier was optimized for maximum power gain. One single stage of the amplifier is shown in figure 6. Interstage matching is accomplished by optimized transformers to obtain ideal impedance transformations. This impedance transformation is achieved by increasing the diameter of the primary coil and decreasing the diameter of the secondary coil. In other words, the coupling factor is changed to optimize the leakage and magnetizing inductors for tuning the gate and drain capacitors of the transistors. The input and output matching networks do not only provide impedance matching between the 50 Ohm probes and the circuit, they also act as baluns to convert the differential signal on chip to a single ended 50 Ohm impedance. The use of transformers also creates the possibility to easily connect decouple capacitors and ESD protection for the DC-supply/biasing bondwires. Indeed, large capacitance can be tolerated at the center tap of the transformer, which is a virtual ground for the differential circuit.

Figure 7 shows the chip photograph. The amplifier consumes an area of $1360 \mu\text{m}$ by $640 \mu\text{m}$, including on chip baluns, GSG-probepads, bondpads, decouple capacitors and ESD protection. The actual amplifier only consumes an area of 0.11 mm^2 . Each stage consists of a neutralized differential pair with $15 \mu\text{m}$ active devices and $12 \mu\text{m}$ crossed capacitors to obtain high gain and stability at 100 GHz.

The proposed 6 stage amplifier provides a small signal gain of 11 dB at 99 GHz. The 3 dB bandwidth is about 11 GHz starting from 93 GHz up to 104 GHz (Figure

Fig. 6. Schematic of a single stage of the 100 GHz amplifier.

Fig. 7. Chip photograph.

8). The measurements are performed with an Agilent N5250A Vector Network Analyser and Infinity 110 GHz 75 μm pitch GSG probes. The amplifier consumes about 94 mW with a supply voltage of 1.2 V. This results in a current density of approximately 400 $\mu\text{A}/\mu\text{m}$ which is the optimal bias point for maximal f_{max} [6].

Fig. 8. Measured and simulated S-parameters.

Although the original design was simulated to achieve a gain of 18 dB with the same power consumption, the measurement results show a gain of only 11 dB. This was caused by an error in the port and probepad definitions of the finite-element simulations of the input and output matching networks. The simulations and measurements were matching much better after solving this problem (Figure 8). From this we can conclude that a gain of approximately 20 dB can be achieved when these impedance mismatch problems are solved.

V. CONCLUSION

Differential design techniques for accurate and structured design of W-band mm-wave CMOS circuits were proposed in this paper. Transformers were introduced as passive matching circuits, which provide numerous advantages compared to traditional matching circuits. Stabilization and gain improvement of the differential pair is achieved by a wideband neutralization technique without increasing the power consumption. Compared to traditional mm-wave single ended design techniques, which suffer from poor noise performance and high area consumption due to bulky passive devices, these differential techniques offer innovating solutions. Also, adequate simulation of the active devices, which is less accurate at these high frequencies due to the lack of a virtual ground in single ended circuits, can be achieved with these new techniques. All these techniques were combined in a fully differential 6 stage amplifier which is successfully measured. To our knowledge, this is the first fully differential 100 GHz amplifier in CMOS.

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REFERENCES

- [1] S. Ohmori, Y. Yamao and N. Nakajima, "The Future Generations of Mobile Communications Based on Broadband Access Technologies," *Communications Magazine, IEEE*, vol. 38, Issue 12, pp. 134-142, December 2000.
- [2] J. Wells, "MM-Waves in the Living Room: The Future of Wireless High Definition Multimedia," *Microwave Journal*, vol. 52, No. 8, August 2009.
- [3] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, S. P. Voinigescu, "A Zero-IF 60GHz Transceiver in 65nm CMOS with > 3.5Gb/s Links," *Custom Integrated Circuits Conference, CICC 2008. IEEE*, pp. 471-474, September 2008.
- [4] K. Mizuno, "Millimeter wave imaging technologies," *International Symposium on Signals, Systems, and Electronics, ISSSE 1998*, pp. 289-290, September 1998.
- [5] Y. Jiang, J. Tsai, H. Wang, "A W-Band Medium Power Amplifier in 90 nm CMOS," *Microwave and Wireless Components Letters, IEEE*, vol. 18, no. 12, pp. 818-820, December 2008.
- [6] T. Yao, M. Q. Gordon, K. K. W. Tang, K. H. K. Yau, M. Yang, P. Schvan, S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *Journal of Solid-State Circuits, JSSC 2007*, vol. 42, Issue 5, pp. 1065-1075, May 2007.
- [7] S. P. Voinigescu, S. T. Nicolson, M. Khanpour, K. K. W. Tang, K. H. K. Yau, N. Seyedfathi, A. Timonov, A. Nachman, G. Eleftheriades, P. Schvan, M. T. Yang, "CMOS SOCs at 100 GHz: System Architectures, Device Characterization, and IC Design Examples," *International Symposium on Circuits and Systems, ISCAS 2007, IEEE*, pp. 1971-1974, May 2007.
- [8] D. Chowdhury, P. Reynaert, A. M. Niknejad, "A 60GHz 1V +12.3dBm Transformer-Coupled Wideband PA in 90nm CMOS," *International Solid-State Circuits Conference, ISSCC 2008, IEEE*, pp. 560-562, February 2008.