A 70 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB Impulse Radio Receivers

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Abstract—This paper presents an integrated ultra-low power analog front-end (AFE) architecture for UWB impulse radio receivers. The receiver is targeted towards applications like wireless sensor networks typically requiring ultra energy-efficient, low data-rate communication over a relative short range. The proposed receiver implements pulse correlation in the analog domain to severely relax the power consumption of the ADCs and digital backend. Furthermore a fully integrated prototype of the analog front-end, containing a PLL, programmable clocking generator, analog pulse correlator, a linear-in-dB variable gain amplifier and a 4-bit ADC, is demonstrated. Several design decisions and techniques, like correlation with a windowed LO instead of with a matched template, exploiting the duty-cycled nature of the system, operation in the sub-1 GHz band as well as careful circuit design are employed to reach ultra-low power consumption. The analog front-end was manufactured in 130 nm CMOS and the active circuit area measures $1000\ \mu\text{m} \times 1500\ \mu\text{m}$. A maximum channel conversion gain of 50 dB can be achieved. Two symbol rates, 39.0625 Mpulses per second (Mpps) and 19.531 Mpps are supported. The AFE consumes 2.3 mA from a 1.2 V power supply when operating at 39.0625 Mpps. This corresponds to an energy consumption of 70 pJ/pulse. A wireless link over more than 10 m in an office-like environment has been demonstrated at 19.531 Mpps with a PER $< 1\text{E} - 3$ under direct LOS conditions.

Index Terms—ADC, analog front-end, impulse radio, mixer, PLL, UWB, VGA.

I. INTRODUCTION

WIRELESS sensor networks have gained an increasing research interest in the last few years. They provide a huge all-new myriad of application domains in a number of fields (like healthcare, logistics, agriculture, environmental monitoring, etc.) with very specific requirements for the communication. Often only modest data rates over short distances are required. The practical feasibility of such applications depends largely on the power consumption of the sensor nodes, which is typically dominated by the radio. For long-term battery-powered, or even autonomously scavenger-powered devices, ultra energy-efficient radios are required.

The FCC defined ultra-wideband (UWB) communication in 2002 [1]. Impulse radio communication is a specific form of

UWB where data is modulated on short pulses in time (less than 2 ns). This form of communication has a high robustness against fading and multipath channels, typically frequency selective effects [2], and allows the use of fairly simple, low-power transmitter [3]–[6] and receiver designs. As such, impulse radio communication becomes increasingly popular for energy-efficient low data-rate radios.

Due to the recent advances in integrating very potent and complex digital logic, fully digital receivers [7] became attractive. In these receivers, the AFE boils down to adequate amplification after which the signal is digitized. With powerful digital processing readily available, very good performance can be achieved. However, due to the wide bandwidth signals employed, very fast ADCs at Nyquist rate and digital logic are required which comes at a power penalty. As demonstrated in [7], this type of receivers is well suited for high data-rate applications, but the high power-consumption cannot be tolerated in low-power wireless sensor networks.

At the other end of the spectrum, super-regenerative receivers (SRR) typically boast very low power consumptions (e.g., [8] reports a 400 μW receiver). The AFE consists of an oscillator core which is periodically activated at the pulserate. If a pulse with the same center frequency as the oscillator core arrives at the same time the core is started, the start-up time will be significantly faster. This difference in start-up time is measured to determine whether a pulse arrived or not. Super-regenerative receivers are thus well suited for OOK. Due to the high gain of the oscillator, these receivers can operate at very low power levels while maintaining a decent sensitivity. A big disadvantage however is the very limited robustness against in-band interferers. Any signal close to the center frequency will increase the start-up time of the oscillator tank. Since UWB is supposed to work overlaying existing and future narrowband users in the same band, this issue cannot be overlooked. Precautionary measures are required adding again to the overall power consumption (e.g., [9] implements 12 narrowband SRRs and combines the output. A wideband pulse will trigger all SRRs, while a narrowband interferer will only corrupt a single one).

A quadrature analog correlating receiver [10], [11] allows low power consumption at low data rates, while maintaining good interference robustness and is used for the presented receiver. A block schematic of the implemented receiver is shown in Fig. 1. The received signal is correlated with a template waveform. This is implemented in the analog domain allowing the ADCs and the digital back-end to be clocked at the low pulse rate. To overcome the problem of transmitter/receiver synchronization, I/Q reception is employed so that small clock offsets between transmitter and receiver can be tracked and corrected.

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Fig. 1. Complex analog correlating receiver architecture.

Since the pulse correlation is shifted towards the analog domain, the feasibility of the proposed receiver depends on the possibility of an energy-efficient implementation of the analog front-end (AFE). One of the most power consuming functionalities of the AFE is typically the analog pulse correlation and template generation. To reduce the power consumption of this function, correlation with a windowed LO instead of with a matched locally generated template is performed. Furthermore, the duty-cycled nature of the pulsed input signal can be exploited by only enabling the RF blocks when an input pulse is expected to arrive [12]. Finally the receiver operates in the sub-1 GHz band which provides sufficient bandwidth for the required data-rates.

The receiver operation is detailed in Section II. The design of the AFE is explained in Section III. Experimental measurement results are shown in Section IV.

II. PRINCIPLE OF OPERATION

A. Pulse Reception

With impulse radio communication, data is modulated onto several short pulses according to a certain modulation scheme and spreading code. BPSK modulation is employed since it poses the least strict requirements in terms of output SNR. A target pulse error rate (PER) of $1E-1$ requires -1 dB E_B/N_0 . When looking at the UWB spectral mask as defined by the FCC in [1], two frequency bands can be identified for UWB. An effective isotropically radiated power (EIRP) of -41.3 dBm/MHz is allowed in the 0–960 MHz band (currently available for imaging and ranging) and in the 3.1–10.6 GHz band. Since the low band provides sufficient bandwidth for the targeted performance, this band was chosen to keep the power consumption of the RF building blocks as low as possible. The employed pulses occupy a 500 MHz-wide band ranging from 350 MHz to 900 MHz with a center frequency of 625 MHz. The 900 MHz upper boundary was chosen to be sufficiently far away from the GSM band, while the lower boundary was confined by antenna size. A typical pulse train is shown in Fig. 2(a). To recover the data bits, the receiver has to detect the pulses and then recover the data bits by correlating the received pulse train with the proper spreading code. As is often the case, most of the power savings can be found at the highest design

Fig. 2. (a) Typical input pulse train and receiver window of operation. (b) The results of correlation with a windowed LO. (c) The corresponding digitized constellation diagram.

abstraction level. Thus designing an ultra-low power impulse radio receiver starts with an optimal architectural exploration.

There are several methods to implement impulse radio receivers. An extensive architectural exploration is described in [10]. If power consumption is the main criterion, the most promising receiver architecture is the “complex analog correlating receiver” (see Fig. 1). In the analog correlating receiver, the pulse train is detected in the analog domain and the data is recovered in the digital domain. This has the benefit of only needing low-resolution ADCs at the low pulse rate (e.g., < 40 MHz). The consequence is that the whole digital back-end is only working on data at the same low pulse rate as well. The power consumption of the ADCs and the digital back-end can thus be very low compared to an all-digital design where the incoming pulse is immediately digitized requiring fast, high-resolution ADCs and fairly complex high-speed logic to recover the pulse train.

The problem of recovering the pulse train is now shifted to the analog domain. To do this, the incoming signal needs to be correlated with a template waveform. Generating the proper template waveform for matched filtering is not a trivial thing to do requiring complex signal processing and filtering for channel estimation. It is however possible to use a windowed clock as a pulse template instead, as is explained in [10]. Simulations using the IEEE 802.15.4a channel model [2], which provides a

Fig. 3. (a) Input pulses and RX window clock in the presence of clock offset. (b) The corresponding constellation diagram resembles a spiral.

model for low rate UWB under 1 GHz, shows a performance loss of -4.5 dB compared to the ideal case where a matched template with channel estimation is used. This needs to be compensated for by modulating a single data bit onto sufficient pulses until the required SNR is achieved. The number of pulses needed depends on the application (required data rate, distance between transmitter and receiver, channel properties etc.) and can range from 1 to 64 or even more resulting in processing gain of 0 dB–18 dB. To generate the windowed clock, an LO with the same center frequency as the incoming pulse is generated with a PLL. This LO is only passed to the mixer inputs when a window signal, indicating the arrival of an incoming pulse (see Figs. 1 and 2(a)), is high, effectively generating the windowed clock. In our application, the window is a signal at pulse rate with an on-period of 5 ns. For a Gaussian pulse with a center frequency of 625 MHz, 99% of the pulse energy is contained in a 4 ns period. The 5 ns window is thus sufficiently long to receive the pulse even if the window is slightly misaligned. On the other hand, it is short enough in order not to receive too much noise and interference (a 5 ns receive window suppresses noise and interferer power by 7 dB for a pulse repetition rate of 39.0625 MHz) without posing too strict requirements on the window clock generator (better than 1 ns timing resolution). The use of a windowed LO as a template for the correlation, means that the receiver is most sensitive to interference at 625 MHz, which is thus only suppressed by 7 dB for a pulse rate of 39.0625 Mpps.

The outputs of the analog correlation with a windowed LO are shown in Fig. 2(b). The correlation action is performed only during the short window interval. After that the value is held, eliminating the need for a sample and hold for the ADC further down the channel. Right before a new pulse is expected to arrive the channel is reset (the correlator outputs go to zero).

The output of the analog correlator is amplified with a digitally controlled variable gain amplifier. The digital BE determines the optimal gain setting. Finally the result is converted to digital (Fig. 2(c)) and fed to the digital BE.

B. Synchronization

Two important issues need to be addressed, RX synchronization and TX–RX clock offset.

Initially, the receiver has no idea when a pulse is arriving at the antenna and the window signal will thus not be properly aligned with the incoming pulses. In order for the receiver to be able to synchronize to the incoming pulses, data communication consists of two phases, data acquisition and data reception. During data acquisition, a known header is transmitted. The receiver searches all possible window positions for this known header and measures the received signal energy in each window. These search algorithms run on the digital backend, which controls the analog front-end (see Fig. 1). Once the proper window is found, the receiver waits till it has received the header end, and then switches to regular data reception.

Additionally, in a real application clock offset between the transmitter and receiver will be inevitable. A small clock offset results in a slowly but gradually increasing phase difference between incoming signal and the window. As a result, the incoming pulse signal will gradually move outside the window and eventually data is lost (see Fig. 3(a)). To overcome this problem, the digital back-end can reposition the window clock. To detect the clock offset and the direction, I/Q reception is employed. Clock offset will now result in a constellation diagram resembling a spiral towards the origin (see Fig. 3(b)). If the RX clock is faster than the TX clock, the constellation diagram will rotate clockwise. The speed of rotation determines the value of the clock offset. The digital BE is thus able to track the clock offset and correct for it.

C. Link Budget

An EIRP of -41.3 dBm/MHz is allowed in the 0–960 MHz band. The EIRP takes the antenna gain into account, which allows to make abstraction of the antenna in the calculation of the link budget. Taking a 3 dB margin for not completely filling the spectrum, an average transmit power P_{TX} of -17.3 dBm can be radiated when using 500 MHz of bandwidth. According to the IEEE 802.15.4a channel model [2], up to 60 dB loss (PL) can be expected at 10 m distance in an office-like environment. The channel noise $N_{channel}$ in a 500 MHz wide band equals -87 dBm. It was argued in the previous section that a 4.5 dB performance degradation $Loss_{templ}$ is to be expected because of the correlation with a non-ideal template waveform. Finally $E_b/N_0 = -1$ dB is required for a raw PER better than $1E-1$

Fig. 4. Charge-pump PLL block diagram.

when BPSK is used. For a pulserate of 39.0625 Mpps, this translates to -12 dB SNR while only -15 dB is required for 19.531 Mpps. Under these assumptions, the link budget for a pulse repetition rate of 39.0625 Mpps is shown in the formula below.

$$\text{SNR} = P_{TX} - PL - N_{\text{channel}} - \text{Loss}_{\text{templ}} - \text{NF} - I \quad (1)$$

$$\begin{aligned} \text{NF} + I &= -17.3 \text{ dBm} - 60 \text{ dB} + 87 \text{ dBm} - 4.5 \text{ dB} + 12 \text{ dB} \\ &= 17.2 \text{ dB}. \end{aligned} \quad (2)$$

Therefore, a 17.2 dB noise figure NF (including additional implementation losses I) should suffice for communication at 39.0625 Mpps over 10 m with a raw PER of $1\text{E} - 1$. The requirement relaxes to 20.2 dB for a pulse repetition rate of 19.531 Mpps. This is a rather high number indicating that an LNA is not a necessity if sufficient gain is achieved within the first stage of the receive chain (the analog pulse correlator) and additional implementation losses can be kept low.

III. RECEIVER FRONT-END DESIGN

An energy-efficient implementation for the complete digital back-end, implementing all the data acquisition, data reception and clock offset algorithms has been demonstrated previously [13]. The design of the analog front-end, will be discussed in this section. The main building blocks are the PLL, the programmable window (and other derivative) clock generator, the analog pulse correlator, the variable gain amplifier and the analog-to-digital converter. All the blocks are DC-coupled and the output stages properly bias the input stages of the next block. This eliminates the need for additional bias networks. Because the front-end implements a full PLL, a duty-cycled mixer and ADC, all switching building blocks, a lot of supply and substrate noise can be expected. In order to provide sufficient supply noise rejection, a fully differential design is used. Each of the building blocks will be discussed in detail.

A. Phase-Locked-Loop

The phase-locked loop is implemented as shown in Fig. 4. A charge-pump structure, with passive loop filter, differential ring oscillator and integer- N divider, was chosen. The requirements are not too strict [10] allowing a low-power implementation. The required LO output frequency is a rather modest 625 MHz. Since the LO is not intended for frequency selectivity as is the case in more traditional narrowband communication, but rather as a template for wideband signals, a fairly high level of phase noise can be tolerated. High-level system simulations did not show any significant performance degradation for levels up to -90 dBc at 1 MHz offset. Finally differential quadrature outputs are required.

Fig. 5. Ring oscillator delay cell schematic.

1) *VCO*: Keeping in mind the specific requirements (low power consumption, modest phase noise specification, modest output frequency, differential quadrature outputs required) a ring oscillator based VCO is a suitable structure. Since quadrature outputs are required, an even number of differential delay cells is required. All the requirements could be met with the minimum number of two delay cells.

Fig. 5 shows the implementation of a single delay cell. Transistors M1 essentially form an inverter. This structure was chosen since no DC current sources are needed which saves power consumption. Furthermore full rail-to-rail switching is employed which results in a better phase noise performance [14], [15]. Since no true fully differential design is employed, oscillation is not guaranteed if only simple inverters are used. Unequal rise and fall times of the individual delay cells would eventually cause all the VCO nodes in Fig. 4 to go to either of the supply rails, which is a stable operating point. To counter this problem, transistors M2 form a positive cross coupling forcing the output nodes at opposite voltages. Furthermore the output voltages flip at the same moment even if the input signals do not (e.g., due to mismatch or unbalanced interconnect) mitigating the effect of unavoidable unequal rise/fall times.

Imagine $\text{In}+$ flips from VDD to GND and $\text{In}-$ from GND to VSS but a little later (see Fig. 6). At the moment $\text{In}+$ flips, M1a is switched off. M1c is switched on and starts charging its drain node. As a result, M2b starts conducting and its source node is charged to VDD, shutting off M2c. This prevents the output $\text{Out}+$ to flip to VDD. At the moment $\text{In}-$ flips from GND to VDD, M1b starts conducting, effectively discharging its drain node. This causes M2c to start conducting and both outputs flip at the same time, as can be seen in Fig. 6.

Since minimum sized transistors are used in order to reduce the power consumption as much as possible, the VCO free running frequency is very dependant on process variations and device mismatch. Monte Carlo and corner simulations showed a possible deviation of ± 70 MHz on the center frequency. Therefore a quite broad tuning range of 23% is required. Each delay cell is loaded with a varactor in the form of a MOS transistor wired as a voltage-controlled capacitor. MOS varactors are well suited for frequency control in ring VCOs [16] and have the added benefit that they are easy to integrate and do not consume a lot of die area.

Fig. 6. Simulated output waveforms of the delay cells. If one of the inputs (In+) flips before the other one, its corresponding output is prevented from flipping until the other input flips.

Fig. 7. (a) Phase-frequency detector block diagram. (b) TSPC DFF implementation.

2) *Phase-Frequency Detector and Dividers*: Three dividers are cascaded to divide the VCO frequency with a factor of 8. No fractional-N synthesizers are used to save power consumption. The dividers are implemented in true-single-phase-clock logic which lends itself for low power, small area implementation for frequencies below GHz range [17].

The VCOs divided output is compared with an externally applied reference clock by a phase-frequency detector (PFD) implemented as in Fig. 7. Once again, in order to save power consumption, true-single-phase-clock (TSPC) D-flip-flops are used to implement the SR-latches. The D-flip-flops are positive edge-triggered which makes the PFD insensitive to the duty cycle of the incoming signals. Due to the gate delay of the NOR port resetting the latches, both the UP and DN signals are high for about 300 ps with equal inputs. This eliminates the dead-zone, frequently associated with this type of PFDs by assuring that a valid input always drives the charge pump [18]. Failing to do so, would result in UP and DN signals both being zero for equal inputs. The charge pump is then in a high output impedance state effectively cutting the PLL loop.

3) *Charge Pump and Loop Filter*: The charge pump and loop filter are shown in Fig. 8. The NUP and NDN signals (buffered PFD outputs) drive the input transistors M1 which are sized to have a much stronger sink capability than M2. Imagine that NUP is high. Almost all of the current is then flowing through M1b and no current is mirrored to the output transistors Moutb. The output voltage is not pumped up. If however NUP is low, all of the current is flowing through M2b and gets mirrored to the output transistor Moutb. The dual case is valid for down

Fig. 8. Charge pump and loop filter schematic.

pumping. The proposed charge pump is able to achieve rail-to-rail output.

A second-order passive loop filter is implemented because of the design simplicity and power savings compared to an active filter. The UP/DN signals from the PFD charge/discharge capacitor C1. R1 realizes a zero which controls the damping and C2 suppresses glitches which occur when the charge pump output transistors switch [19]. The filter values were determined with a high-level Matlab model, which resulted in: $C1 = 34.3$ pF, $C2 = 5.48$ pF, $R1 = 20.6$ k Ω all of which are easy integrated. Note that the value of C2 is rather high. Typically this capacitor is about 10 times smaller than C1 [19]. A larger C2 will provide more glitch suppression at the expense of a reduced damping in the loop transfer function. Since the PLL does not have to switch between different frequencies, the loop dynamics are only of secondary concern.

The complete PLL including buffers has a measured power consumption of 800 μ W (see Table I). According to post-layout simulations, almost 60% of the power goes to the buffers, which have to drive fairly long lines (600 μ m each) in the final design as can be seen in the die photo (see Fig. 13).

B. Derivative Clocks Generator

A pulse reception cycle starts when the window clock goes high (see Fig. 2). When it goes down again, the ADC should sample after the internal amplifiers have settled. Finally the integrators should be reset after the ADCs have sampled. The positioning in time of all these clocks should be programmable, as was explained earlier, corresponding to the time-of arrival of the incoming pulses. The receiver thus needs three internal clock signals derived from the LO: an ADC sample clock, a window clock and an integrator reset clock. All three clocks are clocks at pulse rate. Since the window is 1 ns longer than the transmitted pulse, the precision of the clock positioning should be better than 1 ns.

Four identical cascaded stages are employed to generate the clock at pulse rate. Each stage consists of a MUX and a negative edge-triggered divide-by-two with differential outputs. An extra MUX is placed behind the last divider (see Fig. 9). The first stage is driven by the 625 MHz LO. Each MUX determines whether LO/OUT_i or $\overline{LO/OUT_i}$ is passed to the first/next divider. Using four of these stages it is possible to derive from a 625 MHz LO a 39.0625 MHz clock and position the rising edge with a precision of 800 ps (= half the LO period). An additional stage (not shown) is present as well generating the same signals at 19.531 MHz so that the front-end can switch between a high or a low pulse rate. Arbitrary pulse rates are thus not achievable because that would require more complex and

Fig. 9. Programmable window clock generator.

Fig. 11. Correlator output during the integration phase. The difference between the two curves is where the integration is performed.

Fig. 10. Analog pulse correlator schematic.

power-consuming dividers. Six bits, connected to the MUXs, are used to select the different clock positions. An edge-triggered glitch generator is used to generate the proper window and reset pulses. With the proposed scheme a minimum number of gates are clocked at the high LO frequency compared to a more straightforward approach using a programmable counter. The derivative clocks generator includes a non-programmable divider providing a stable clock that is used to clock the digital BE. The complete derivative clocks generator, again including adequate buffering, consumes $450 \mu\text{W}$ according to measurements (see Table I).

C. Analog Pulse Correlator

The analog pulse correlator is basically a mixer followed by an integration stage. The circuit is shown in Fig. 10. The mixing action itself is performed by a double balanced switching Gilbert cell. The benefit of using this topology, is that it provides an easy-to-implement means to duty-cycle the power consumption. As discussed before, the template waveform is a windowed version of the LO and is generated by an AND of the LO and the window signal, resulting in the signals LOW (see Fig. 10). The LO is thus passed to the mixer only when a pulse is expected to arrive. Any other time, LOW is low meaning that all transistors M2 are shut off. No direct path from VDD to VSS remains, eliminating the mixer's power consumption when it is not needed.

The mixer's output current is integrated onto capacitors C1 and C2 through the switches MS. The integration action cannot

be performed at nodes n1 directly because a positive correlation between IN and LOW would drive nodes n1a and n1b to opposite voltages. Since transistors M2 operate in the linear region, this voltage difference is transferred to the drain nodes of transistors M1. Eventhough they are biased in the saturation region, the lengths are kept as small as possible to reduce the parasitic capacitance. Differences in V_{ds} will thus have a non-negligible effect, resulting in a gradually increasing difference between gm_1 and gm_2 . The result is a limited output range and non-optimal mixing action as can be seen in Fig. 11. Making matters worse, this effect depends on the phase difference between the LO and the input signal. The more in-phase the two are, the more pronounced the effect is, turning the analog pulse correlator into a time-variant system. Therefore the integration capacitors are placed after the switches, allowing nodes n1a and n1b to remain at constant DC voltages. This results in a much better integration as can be seen in Fig. 11. The switches are also driven by the window clock. When it is low, the integrated value is held onto the capacitors. The pulse correlator thus also acts as a sample and hold which means no additional sample and hold is needed for the ADC.

At the end of the pulse reception cycle, capacitors C1 and C2 should be reset. Instead of grounding the capacitors and thus discarding any charge present in them, they are reset by precharging them to VDD through transistors MR. The reset current is subsequently reused as part of the bias current. At the start of the integration interval, both capacitors are fully charged. They discharge at an almost constant rate to give the proper bias current together with bias transistors M3. At the same time they integrate the signal current. This current reuse provides a third contribution to reduce power consumption.

The mixer provides a 19 dB voltage conversion gain and has an input-referred 1 dB compression point of -12 dBm. This guarantees linear operation in the presence of relative strong narrowband interferers. The average power consumption is $105 \mu\text{W}$ at 1.2 V with a window length of 5 ns and a pulse repetition frequency of 39.0625 MHz according to post-layout simulations. The power consumption of the analog pulse correlator alone could not be measured, because it shares its powerline with other blocks (VGA and ADC).

Fig. 12. Variable gain amplifier schematic.

D. Variable Gain Amplifier

The correlator's output signal must be amplified to the proper levels for A/D conversion. Depending on the distance between transmitter and receiver and the channel properties, the received signal levels can vary by as much as 30 dB. A linear-in-dB variable gain amplifier is thus needed. This VGA is digitally controlled by the back-end, which determines the ideal amplification during the acquisition phase of data reception.

The VGA is a two-stage amplifier similar to the one described in [20]. The schematic is shown in Fig. 12. The first stage, consisting from transistors M1–M2 is a source-degenerated fully differential transconductance amplifier. The transconductance G_m is given by (with g_{o1} the output conductance of M1 and g_{m1} and g_{m2} the transconductance of M1 and M2):

$$G_m = \frac{1}{\frac{g_{o1}}{g_{m1}g_{m2}} + R_s}. \quad (3)$$

The second stage (transistors M3–M4) is a transimpedance amplifier with closed-loop gain of $-R_f$ for sufficiently large current gain a . The total gain is thus $-G_m R_f$ and can be altered by either changing R_s or R_f [20].

For high linearity, the non-linear term $g_{o1}/(g_{m1}g_{m2})$ needs to be small compared to R_s . For a good compromise between power consumption and linearity, R_s can range in our design between 6 k Ω and 30 k Ω (digitally controlled by 3 bits). This allows the gain to change over a range of 14 dB in stepsizes of 1.95 dB. Higher gains would require a lower value of R_s . In order to guarantee the linearity, too much current would be needed to provide a sufficiently high g_{m1} and g_{m2} . Therefore R_f can be changed as well between either 250 k Ω or 37 k Ω .

A common-mode feedforward structure consisting of transistors M4–7 is used for common-mode output control. The differential first-stage output current is sensed by transistors M5. Differential signals are canceled at node ncm. The second-stage output current is regulated with current mirrors M4–M7. Furthermore the desired output common-mode voltage can be set through the externally applied voltage Vocm.

The simulated gain ranges between 31.27 dB and 1.76 dB, with a stepsize of 1.95 dB, while the minimum bandwidth is larger than 60 MHz. The maximum settling time is 11 ns, which is sufficiently fast for receiving 39.0625 Mpps. The maximum total power consumption is less than 350 μ W for all gain settings. This is again based on post-layout simulations.

Fig. 13. Die photo.

E. Analog-to-Digital Converter

As shown in [10], a resolution of two to three bits for the ADC proves to be the most power-efficient solution. A four-bit ADC is implemented in order to guarantee sufficient ENOB even after integration of a noisy digital BE on the same die. Given this rather low resolution requirement and the modest conversion rate (39.0625 MHz), a flash ADC is the most suitable structure. Flash ADCs typically use a resistor ladder to generate the reference voltages. In order to minimize the effects of kickback noise, a rather large current needs to flow through the reference ladder. Therefore comparators with built-in reference voltages were employed as to eliminate the reference ladder [21]. Each comparator has four binary-weighted calibration capacitors in order to fine-tune the trip points of each comparator individually after manufacturing. Since the output impedance of the VGA is fairly high, a simple low-output-impedance buffer drives the ADC to eliminate the effect of kickback noise on the input. The comparator thermometer code goes through a bubble error correction stage and is subsequently converted to gray code using a ROM-based encoder. The complete ADC including input buffer consumes 200 μ W at 1.2 V, according to post-layout simulations.

IV. MEASUREMENT RESULTS

The analog front end was manufactured in 130 nm CMOS technology. A die photograph is shown in Fig. 13. The chip contains two identical channels which are clearly visible. The clock generation circuitry can be found in the middle of the die. The PLL is located at the right side. Most of the area of the PLL is occupied by the loop filter passives. The total active circuitry measures 1000 μ m $\times$ 1500 μ m. It is clear that this is a pad-limited layout, so discarding all I/O required for testing, would even allow a smaller die size.

A. PLL Measurements

The measured PLL tuning range was from 550 to 692 MHz. All the measured samples (from the same wafer) were able to generate the desired 625 MHz center frequency without a problem. The measured phase noise @ 1 MHz offset was -87 dBc/Hz (see Fig. 14). The measured long-term rms jitter

Fig. 14. Measured PLL phase noise.

Fig. 15. Measured PLL output jitter. The black curve shows the actual measured edges of the LO. The gray curve is the timing histogram of the 0.6 V crossings.

is shown in Fig. 15 and found to be better than 25 ps, easily satisfying the required timing resolution for the window.

B. Analog Pulse Correlator Measurements

Fig. 16 shows the measured differential output waveform for a phase modulated (0/90/180/270 degrees) input pulse with center frequency of 625 MHz. The four demodulated signals are clearly visible. Furthermore, the three different stages discussed previously (integration/hold/reset) are shown as well. A 19 dB voltage conversion gain is achieved and the input-referred 1 dB compression point is located at -12.6 dBm. The LO-to-RF and LO-to-IF isolations are respectively 88 dB and 79 dB resulting in negligible LO-selfmixing.

C. Full Front-End Measurements

To test the full front-end, a ParBERT 81250 was used as a transmitter. Two generator slots were employed to generate the BPSK modulated pulses. These generators can output digital signals with arbitrary low and high voltages. One generator was used for the positive parts of the pulse, the other for the negative. The outputs were combined and filtered to generate pulses as shown in Fig. 17. In order to represent the true ability of the front-end to detect incoming pulses, synchronization was done manually. This means that the proper window code was fed to the front-end and the window was not allowed to change. For the same reason, no clock offset was introduced for the following

Fig. 16. Analog pulse correlator measurements.

Fig. 17. Transmitted pulse.

Fig. 18. Pulse error rate (calculated from the measured EVMS) versus average input power (wired measurements at 39.0625 Mpps).

measurements. The on-chip PLL locked onto the ParBERT reference clock.

Fig. 18 shows the theoretical pulse error rate (PER) versus the average input signal power for a pulserate of 39.0625 Mpps. The PER is calculated from the EVMS of the measured constellation diagrams [22]. A theoretical fit seems to indicate a NF (including implementation losses) of 23.5 dB is realized. In a complete system, where a digital BE would demodulate the pulses into actual bits and would automatically synchronize the window to the incoming pulses, the final bit-error-rate performance can be increased by using several pulses to represent a single bit resulting in more code gain. On the other hand, erroneous synchronization will lead to increased packet error rates.

Fig. 19. Pulse error rate (calculated from the measured EVMs) versus distance between TX and RX at 19.531 Mpps (LOS).

Fig. 20. Constellation diagrams measured at various distances between TX and RX antenna.

A wireless indoor experiment was performed as well. Wide-band planar bowtie antennas were employed to transmit and receive the pulses. They have a maximum gain of 2.3 dBi within the band of interest. The physical size of these antennas is 10 cm $\times$ 23.5 cm. The FCC limits stipulate an EIRP of maximum -41.3 dBm/MHz. This means that, assuming a 3 dB margin for not completely filling the spectrum, an average transmit power of -19.6 dBm can be applied to antennas with 2.3 dBi gain. Taking into account the antenna impedance and duty-cycled nature of the signal, pulses with an amplitude of 130 mV were applied to the transmit antenna when signalling at 19.531 Mpps. This reduces to 91 mV when signalling at 39.0625 Mpps. The pulse-error-rate as a function of the distance under direct line-of-sight conditions is shown in Fig. 19. A PER better than 10^{-3} can be reached at 10 m with a pulse rate of 19.531 MHz under these optimal circumstances.

Fig. 20 shows constellation diagrams as measured at the output of the ADCs at maximum gain settings. To give better visual feedback, the size of each dot is relative to the times it was measured and a unity circle is drawn. Two distinct constellation points are clearly visible. At high gain settings a DC-offset is witnessed which arises from mismatch mainly in the analog pulse correlator. This is a systematic offset and is digitally corrected in the current setup, but reduces the useable input range of the ADCs. A less mismatch-prone design or the addition of a DC-offset compensation could solve this problem.

An overview of the power consumption of the different building blocks is shown in Table I. Four power pins are provided, one for the PLL, one for the derivative clocks generator, one for the I/O and one for the rest of the front-end circuitry.

TABLE I
MEASURED POWER CONSUMPTION AND KEY PERFORMANCES
OF THE DIFFERENT BLOCKS

Block	Power @ 39.0625Mpulses/s	Specification
PLL + buffers	800 μ W	< 20ps rms jitter
Deriv. clocks generator	450 μ W	800ps timing resolution
Analog Pulse Correlator	}	19dB conversion gain
VGA		1.5-31dB gain
ADC		> 2.5ENOB
Total	2.7mW	

TABLE II
COMPARISON WITH OTHER SIMILAR STATE-OF-THE-ART
AFE IMPLEMENTATIONS

	Technology	Band	Pulses/sec	Energy per pulse
[7]	0.18 μ m CMOS	3-5GHz	1G	98pJ
[11]	0.18 μ m CMOS	3-5GHz	20M	1.44nJ
[24]	0.18 μ m CMOS	sub-1GHz	1M	300pJ
[25]	0.13 μ m CMOS	sub-1GHz	30M	128pJ
[26]	0.18 μ m CMOS	3-10GHz	250M	547pJ
[12]	90nm CMOS	3-10GHz	16.7M	2.5nJ
[27]	0.18 μ m CMOS	3-9GHz	62.4M	6.5nJ
[28]	0.18 μ m CMOS	6-8.5GHz	8M	250pJ
This work	0.13 μ m CMOS	sub-1GHz	39.0625M	70pJ

This means that the power consumption of the analog pulse correlator, ADC and VGA could not be measured separately. The complete front-end core has a measured total power consumption of 2.7 mW when receiving 39.0625 Mpps resulting in a very low energy consumption of only 70 pJ per pulse. The power consumption of the IO bondpad drivers was not taken into account, since the front-end is designed to be integrated on the same die as a digital backend.

A comparison with similar UWB receivers is shown in Table II. It is clear that the proposed receiver achieves energy-efficient communication and compares favorable to other implementations. Furthermore results from a true wireless link are shown exceeding previously published results [23], [24].

V. CONCLUSION

Impulse radio UWB communication is becoming increasingly popular for low data-rate, low range, ultra-low power communication. Typical applications include sensor networks. A suitable architecture for a low-power impulse radio receiver is discussed and an ultra low-power integrated quadrature analog front-end is presented. The IC was manufactured in 130 nm CMOS technology. A maximum total channel gain of 50 dB can be achieved and a wireless link in excess of 10 m has been demonstrated at 19.531 Mpps. The AFE consumes 2.7 mW total from a 1.2 V supply when operating at its maximum symbolrate of 39.0625 Mpps. It then achieves a very low energy-consumption of only 70 pJ/pulse.

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