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ESD Protection for Multiple Gate Field Effect Devices and for RF CMOS Circuits

Promotor :
Prof. Dr. Ir.
Guido GROESENEKEN

Proefschrift voorgedragen tot
het behalen van het doctoraat
in de Ingenieurswetenschappen

door

Steven THIJS

September 2009

In samenwerking met

imec VZW

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To Katarina, Nyo and Ime

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Abstract

This thesis addresses two main ESD challenges which lie ahead. First, FinFET technology has a limited available silicon volume to dissipate the ESD current. Therefore, a detailed ESD analysis on FinFET devices is required. Secondly, as technology downscaling allows RF applications operating at higher RF frequencies and wider bandwidths, to be implemented in CMOS, adequate ESD protection needs to be developed without compromising RF performance. Moreover, these enabling technologies simultaneously become more susceptile to ESD stress due to reduced gate oxide breakdown voltages and device power handling capabilities.

To be able to investigate these two challenges in more detail, limitations of the current commercially available ESD measurement equipment need to be overcome. In this thesis, three enhanced ESD characterization and analysis techniques have been developed. First, a Multi-level TLP system was developed enabling the measurement of the true holding voltage as well as the real device physics under ESD stress. Secondly, as gate oxides become more fragile due to technology scaling, the transient turn-on response of the ESD protection devices becomes critical. This turn-on is investigated by a newly developed method to calibrate and analyze the TLP voltage and current waveforms. We have developed a fast, powerful method referred to as HBM-IV, where during an HBM stress pulse, besides the similar quasi-static information as from TLP, also the transient turn-on information is obtained. HBM-IV on a high voltage example shows that under HBM stress, voltage and current overshoots can occur which cannot be reproduced by TLP pulses.

ESD analysis has been performed on ESD protection structures, implemented in SOI FinFET technology. It is found that a new normalization methodology is needed for correct interpretation of the ESD results. Complex dependencies of the different ESD performance parameters on both device geometry and process technology are found. Non-uniform failure exists for grounded gate NMOS devices at high current levels which can be improved by increasing gate length and various ballasting techniques. Narrow fin devices have improved cooling properties but suffer from reduced area efficiency. Well doping, selective

epitaxial growth, strain and silicide blocking can improve the ESD performance. From RF point of view, the large overhead capacitance of the narrow fin devices degrades the RF figure of merit with respect to the wide fin devices, making wide fin devices the preferred choice. To be able to cope with this complex set of dependencies, a design methodology is developed which allows optimization towards a given ESD target while taking these dependencies into account. As such, efficient ESD protection can be designed in FinFET technology, achieving product level HBM levels.

Classical low-capacitive RF-ESD solutions become worse when RF frequencies increase resulting in either degraded RF or ESD performance. Further, CDM protection needs more attention due to its fast rising, high current pulses, travelling along unknown current paths, causing voltage overshoots and turn-on of parasitic current paths. We propose inductive ESD protection as narrowband RF-ESD solution due to its high ESD robustness, low RF impact and large frequency scaling potential. It can be either implemented as a "plug-and-play" inductor to ground, or using an RF-ESD co-designed transformer. CDM robustness is predicted by means of on-wafer VFTLP measurements, allowing identification of possible weak spots at an early design stage. High-quality inductors in combination with voltage clamping diodes can provide very high VFTLP robustness. The future scaling possibilities of the inductor to ground approach are demonstrated in 45 nm planar and FinFET CMOS technologies, up to RF frequencies of 60 GHz. At these frequencies, less ESD signal couples into the RF circuit and due to the decreased inductance of the inductor to ground, less voltage overshoot is present. Therefore, with increasing frequency, the inductor to ground methodology becomes better in terms of RF performance, ESD performance and area consumption, yielding world-record results.

Two-novel wideband RF-ESD protection solutions are proposed with the potential of providing high ESD protection levels at very large bandwidths. First, the "T-diode"-concept uses a transformer to tune out the parasitic capacitance of the ESD protection devices over a wide frequency band. Input matching is maintained from DC to 16.1 GHz, in a 90 m digital CMOS technology. Local clamping and additional turn-off circuitry to prevent failure of parasitic current paths inside the RF core circuit, further increase the ESD robustness level. Secondly, a novel distributed ESD concept (Center Balanced Distributed ESD) is developed, specifically for distributed amplifier circuits. A 1-110 GHz distributed amplifier in 45 nm CMOS is protected using this methodology, yielding excellent ESD robustness.

In conclusion, ESD is not a showstopper for the introduction of FinFET technology. Further, efficient ESD solutions can be implemented for narrow- and wideband RF circuits which exhibit both excellent RF and ESD performance.

List of Acronyms

AD	Analog-Digital
BCD	Bipolar CMOS DMOS (smart power IC technology)
$BEOL$	Back End of Line
$BiCMOS$	Bipolar Complementary Metal Oxide Semiconductor (technology)
BJT	Bipolar Junction Transistor
BOX	Buried Oxide
BV	Breakdown Voltage
BW	BandWidth
$CCTLP$	Capacitively Coupled Transmission Line Pulse
$CESL$	Contact Etch Stop Layer
$CBDESD$	Center Balanced - Distributed ESD
CDM	Charged Device Model
CNT	Carbon Nano Tube
$CMOS$	Complimentary Metal Oxide Semiconductor (technology)
DA	Distributed Amplifier
DC	Direct Current
$DIBL$	Drain Induced Barrier Lowering
DRC	Design Rule Check
$DTSCR$	Diode Triggered Silicon Controlled Rectifier
DUT	Device Under Test
EOT	Equivalent Oxide Thickness
ESD	Electro Static Discharge
$ESDA$	Electro Static Discharge Association
EOS	Electrical Overstress
$FDSOI$	Fully Depleted Silicon On Insulator
FED	Field Effect Diode
$FEOL$	Front End of Line
$FinFET$	Fin Field Effect Transistor
FOM	Figure of Merit
$ggNMOS$	grounded-gate NMOS
$HARVi$	High Aspect Ratio Via
HBM	Human Body Model

HMM	Human Metal Model
HV	High Voltage
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IMD	Inter-Metal Dielectric
$ITRS$	International Technology Roadmap for Semiconductors
$JEDEC$	Joint Electron Device Engineering Council
LDD	Lightly Doped Drain
LNA	Low Noise Amplifier
$LVTSCR$	Low Voltage Triggered Silicon Controlled Rectifier
M	Multiplication Factor
$MEMS$	MicroElectroMechanical System
MIM	Metal Insulator Metal
MM	Machine Model
MOM	Metal Oxide Metal
$MOCVD$	Metal-Organic Chemical Vapour Deposition
$MOSFET$	Metal Oxide Semiconductor Field Effect Transistor
$MTLP$	Multi Level Transmission Line Pulse
OEM	Original Equipment Manufacturers
OPC	Optical Proximity Correction
PA	Power Amplifier
PC	Power Clamp
$PDSOI$	Partially Depleted Silicon On Insulator
RF	Radio Frequency
SB	Silicide Blocking
SCE	Short Channel Effect
SCC	Short Channel Control
SCR	Silicon Controlled Rectifier
SDF	Spacer Defined Fins
SEG	Selective Epitaxial Growth
SEM	Scanning Electron Microscope
SOI	Silicon On Insulater
STI	Shallow Trench Isolation
$TCAD$	Technology Computer Aided Design
$tCESL$	tensile Contact Etch Stop Layer
TDR	Time Domain Reflectometry
TDT	Time Domain Transmission
TEM	Transmission Electron Microscope
TIM	Transient Interferometric Mapping
TSV	Through-Silicon Via
TLP	Transmission Line Pulse
TWA	Traveling Wave Amplifier
$VDMOS$	Vertical Diffused Metal Oxide Semiconductor
$VFTLP$	Very Fast Transmission Line Pulse

UTB	Ultra Thin Body
UWB	Ultra WideBand
$WCDMA$	Wideband Code Division Multiple Access
$WLAN$	Wireless Local Access Network
WLP	Wafer Level Packaging

List of Symbols

β	Common-Emitter Bipolar Current Gain
β	Weibull Slope
BV_{CBO}	Common Base Breakdown Voltage
BV_{CEO}	Common Emitter Breakdown Voltage
BV_{ox}	Oxide Breakdown Voltage
C_B	Board Capacitance
C_{CDM}	CDM DUT Capacitance
C_{DUT}	DUT Capacitance
C_{ESD}	Capacitance of ESD Device
C_{HBM}	HBM Capacitance
C_j	Junction Capacitance
C_{MM}	MM Capacitance
C_{narrow}	Capacitance of Narrow Fin Device
C_{oh}	Overhead Capacitance
C_{pla}	Capacitance of Wide (Planar) Fin Device
C_{PROB}	Voltage Probe Capacitance
C_{tot}	Total Device Capacitance
$E(t)$	Dissipated Energy as function of Time
f_C	Corner Frequency
f_T	Unity Current Gain Cutoff Frequency
γ	Voltage Acceleration Factor
GBW	Gain Band Width
g_{ds}	Output Conductance
g_m	Transconductance
H_{fin}	Fin Height
I_d	Diffusion Leakage Current
I_{ds}	Drain to Source Current
I_{ESD}	ESD Current
$IIP3$	Third Order Input referred Intercept Point
I_m	Modulated Current
I_{on}	MOS Drive Current
$I(t)$	Current as function of Time

It_1	Trigger Current
It_2	Failure Current
k	Coupling Factor
L_{cont}	Size of Source/Drain Contact Area
L_{ESD}	Inductance of ESD Protection Inductor
L_g	Gate Length
L_s	Series Inductance
L_{SD}	Distance between Source/Drain Contact Area and Gate
M	Mutual Inductance
M	Multiplication Factor
M_n	Electron Current Multiplication Factor
M_p	Hole Current Multiplication Factor
n	Turn Ratio of transformer
N	Number of Fins
$nblocks$	Number of Parallel Device Blocks
NF	Noise Figure
q_e	Injected Charge due to Diffusion Current
q_m	Charge in the Base Region
R_{CDM}	CDM Discharge Resistance
R_{HBM}	HBM Discharge Resistance
R_{mo}	Initial Bulk Resistance
R_{on}	On-Resistance
R_s	Series Resistance
R_s	Source Impedance
$R_{s,ESD}$	Series Resistance of ESD Device
R_{tot}	Total Resistance
S_{11}	Input Matching
S_{12}	Reverse Isolation
S_{21}	Gain
S_{22}	Output Matching
S_{norm}	Normalized Fin Spacing
S	Fin Spacing
τ	Carrier Lifetime
τ	Electrical Delay
T_{BOX}	Thickness Buried Oxide Layer
t_{fr}	Forward Recovery Time
T_m	Transit Time
V_{BD}	Breakdown Voltage
V_{CDM}	CDM Precharge Voltage
V_{DD}	Power Supply Voltage
V_{drop}	Voltage Drop during ESD

V_{GS}	Gate to Source Voltage
V_h	Holding Voltage
V_{HBM}	HBM Precharge Voltage
V_j	Junction Voltage
V_M	Modulated Voltage
V_{max}	Maximum Allowed Voltage
V_{MM}	MM Precharge Voltage
V_{SS}	Ground Potential
V_T	Threshold Voltage
$V(t)$	Voltage as function of Time
Vt_1	Trigger Voltage
Vt_2	Failure Voltage
W_{chan}	Channel Width
W_{eff}	Effective Width
W_{ext}	Overlap Gate on Fins
W_{fin}	Fin Width
W_{gen}	Generic Width
W_{intr}	Intrinsic Width
W_{layout}	Total Layout Width
W_{norm}	Normalized Width
Z_c	Characteristic Impedance
Z_{ESD}	Impedance of ESD Device

Publication list

Journal Contributions - First Author

J1 **S. Thijs**, M. I. Natarajan, D. Linten, W. Jeamsaksiri, T. Daenen, R. Degraeve, A. J. Scholten, S. Decoutere and G. Groeseneken, "Implementation of Plug-and-Play ESD Protection in 5.5 GHz 90 nm RF CMOS LNAs - Concepts, Constraints and Solutions", *Microelectronics Reliability*, Vol. 46, Issues 5-6, pp. 702-712, May-June 2006.

J2 **S. Thijs**, D. Trémouilles, C. Russ, A. Griffoni, N. Collaert, R. Rooyackers, D. Linten, M. Scholz, C. Duvvury, H. Gossner, M. Jurczak and G. Groeseneken, "Characterization and Optimization of Sub-32nm FinFET Devices for ESD Applications", *IEEE Transactions on Electron Devices*, Vol. 55, no. 12, pp. 3507-3516, December 2008.

Journal Contributions - Second Author

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P11 S. Thijs and D. Trémouilles, "Silicon Controlled Rectifier (SCR) in FinFET technology"

P12 S. Thijs, D. Linten and D. Trémouilles, "Bidirectional ESD power clamp for SOI CMOS technologies (e.g. FinFET)"

P13 S. Thijs, D. Linten and D. Trémouilles, "Keep-off circuit for ESD protection devices"

P14 S. Thijs and D. Linten, "Center Balanced Distributed ESD protection"

P15 S. Thijs and D. Linten, "Turn Off of parasitic path in core circuit"

Nederlandstalige Samenvatting

ESD Bescherming voor Meervoudige Gate Veld Effect Structuren en voor RF CMOS Circuits

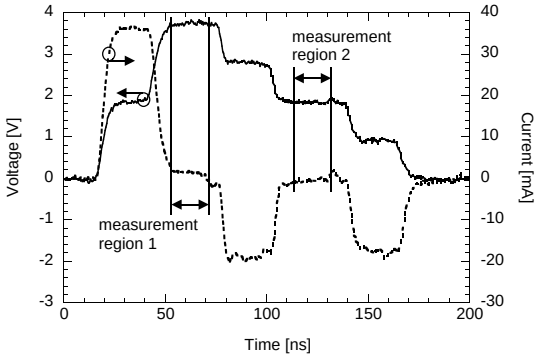
Inleiding

Twee grote uitdagingen liggen in het verschiet voor de ESD ontwerpingenieur. Is ESD enerzijds een spelbreker voor de introductie van FinFET technologie door het geringe silicium volume van de structuren? Is anderzijds een goede ESD bescherming compatibel met de strenge vereisten voor RF circuits met steeds hoger wordende RF frequenties? Voor deze laatste uitdaging zijn zowel oplossingen nodig voor smalbandige als breedbandige RF toepassingen. Ook moet er meer aandacht besteed worden aan CDM bescherming ten opzichte van HBM, omdat dit type ESD stress meer kritisch is en er moeilijker tegen te beschermen valt. Om deze twee uitdagingen goed aan te kunnen gaan, moeten eerst de beperkingen van de huidige meetsystemen worden weggewerkt.

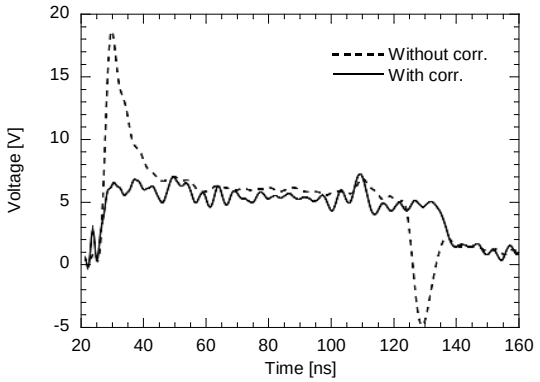
ESD Karakterisatie en Analyze Technieken

In deze thesis werden er drie nieuwe ESD karakterisatie en analyze technieken ontworpen die de bestaande technieken en meetsystemen verder uitbreiden. Eerst hebben we een Multi-Level Transmissie Lijn Puls (MTLP) meetsysteem ontworpen. Vervolgens hebben we een transient analyze uitgevoerd op ESD protectiestructuren door gebruik te maken van de spannings- en stroomgolfvormen verkregen tijdens een klassieke TLP meting. Als laatste hebben we een Human Body Model-IV (HBM-IV) curve verkregen door de transient spannings- en stroomgolfvormen van een HBM meting te combineren.

Door MTLP te gebruiken kan een TLP-IV curve gegenereerd worden die niet beperkt is door de impedantie van het meetsysteem, typisch 50 Ω. Eerst wordt de te onderzoeken structuur aangeschakeld door een puls aan te leggen



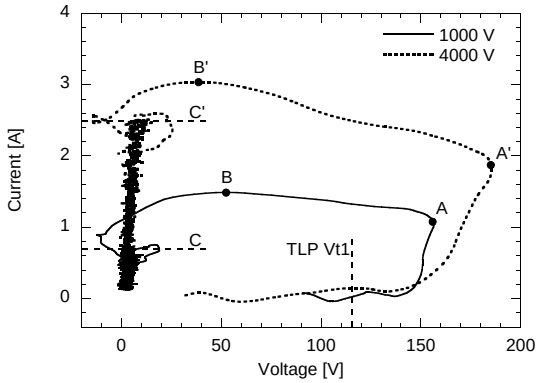
Figuur 0.1: Resulterende spannings en stroom golfvormen tijdens een MTLP meting op een open belasting.



Figuur 0.2: Ruwe en gekalibreerde spannings golfvorm voor een ggNMOS transistor in een 90 nm CMOS technologie tijdens een 500 mA TLP stroom puls.

met voldoende grote amplitude. Na het aanschakelen wordt de amplitude van de puls verlaagd zonder deze af te schakelen, zodat de structuur vanuit aangeschakelde toestand naar een toestand met lage stroom wordt gebracht en bijgevolg niet beperkt is door de systeemimpedantie. Een voorbeeld van een resulterende spannings en stroom golfvorm tijdens dergelijke MTLP meting op een open belasting wordt getoond in Fig. 0.1.

Uit de spannings- en stroomgolfvormen die verkregen worden tijdens een TLP meting kan naast de quasi-statische TLP-IV curve ook informatie verkregen worden over het transient schakelgedrag van de structuur door het tijdsgedrag van de golfvormen te analyzeren. Het is hiervoor belangrijk dat de oscilloscoop zodanig ingesteld is dat de volledige golfvormen opgemeten kunnen worden zonder tegen de limieten van het instelbereik van de oscilloscoop aan te lopen. Verder is het noodzakelijk om de parasitaire elementen van het meetsysteem



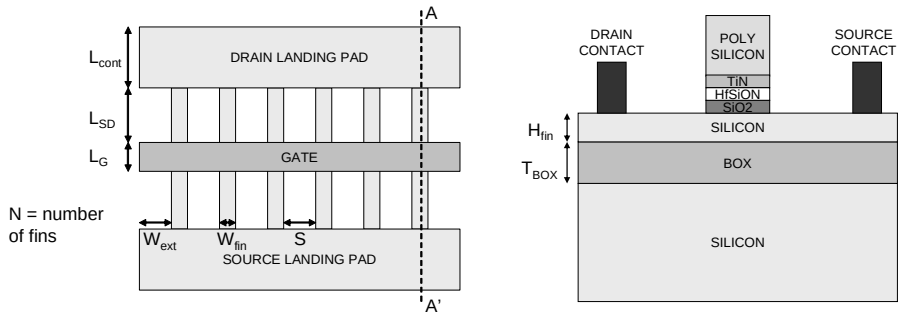
Figuur 0.3: HBM-IV curve gegenereerd uit spannings en stroom golfvormen van een VDMOS SCR structuur, voor 1000 V en 4000 V HBM stress niveau's. Punt A toont een spanningspiek aan, punt B een stroompiek en punt C toont het verwachte stroomniveau gebaseerd op de HBM spanning.

op te meten en een nauwkeurige kalibratie uit te voeren om de invloed ervan te verwijderen. Op die manier wordt het transient schakelgedrag van de te onderzoeken structuur bekomen. Een voorbeeld hiervan wordt getoond op een ggNMOS transistor in Fig. 0.2 waar een spanningspiek opgemeten wordt zonder kalibratie en die volledig verdwenen is na de kalibratie. Er treedt bijgevolg bij het aanschakelen van dergelijke ggNMOS transistor geen spanningspiek op.

Vanuit de opgemeten spannings en stroom golfvormen tijdens een HBM meting op een ESD structuur kan een HBM-IV curve gegenereerd worden door eliminatie van de tijd. Naast dezelfde quasi-statische parameters die ook met TLP bekomen worden, kunnen nog een aantal bijzondere effecten opgemeten worden die ontstaan uit de interactie tussen de structuur en de HBM tester. Deze effecten zijn uniek voor de HBM meting en kunnen niet met TLP bekomen worden. Het is ook belangrijk om op te merken dat de impedantie van de HBM tester, met name 1.5 kΩ, een grote rol speelt in deze interactie. Bijgevolg zullen 50 Ω implementaties van een HBM tester tot foutieve resultaten leiden. Een voorbeeld van een 1000 V en 4000 V HBM-IV curve voor een VDMOS SCR structuur wordt getoond in Fig. 0.3. Er is duidelijk een spanningspiek zichtbaar bovenop de quasi-statische TLP trigger spanning Vt_1, en een stroompiek bovenop het verwachte stroomniveau gebaseerd op de HBM spanning. Deze spannings- en stroompieken kunnen aan de basis liggen voor miscorrelatie tussen HBM en TLP resultaten.

ESD Bescherming in FinFET Technologie

Volgens de Internationale Technologie Roadmap voor Halfgeleiders (ITRS) 2007, zal de fysieke gate lengte van een transistor 9 nm bereiken in 2016. Het gebruik van bulk CMOS zal dan beperkt worden door een aantal korte-



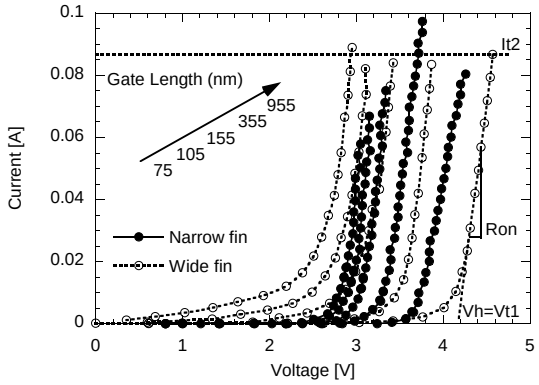
Figuur 0.4: Vereenvoudigd horizontaal zicht (links) en vertikale doorsnede volgens de snede A-A' (rechts) van een FinFET structuur met aanduiding van de belangrijkste geometrische parameters (niet op schaal).

kanaaleffecten, die gepaard gaan met transistor schaling. Om deze barrière te overwinnen, worden er nieuwe structuren ontwikkeld, waarbij de meervoudige gate structuren de meest veelbelovende resultaten geven. Een FinFET is een dergelijke meervoudige gate structuur met heel goede controle over de korte-kanaaleffecten en waarvan de processing compatibel is met standaard CMOS processing. Fig. 0.4 toont een horizontaal bovenaanzicht (links) en een vertikale doorsnede (rechts) van een FinFET structuur, met aanduiding van de belangrijkste geometrische parameters. De structuur is opgebouwd uit parallelle silicium 'vinnen' ('fins') waarvan het kanaal aan de zijkanten en de bovenkant gecontroleerd wordt door de gate.

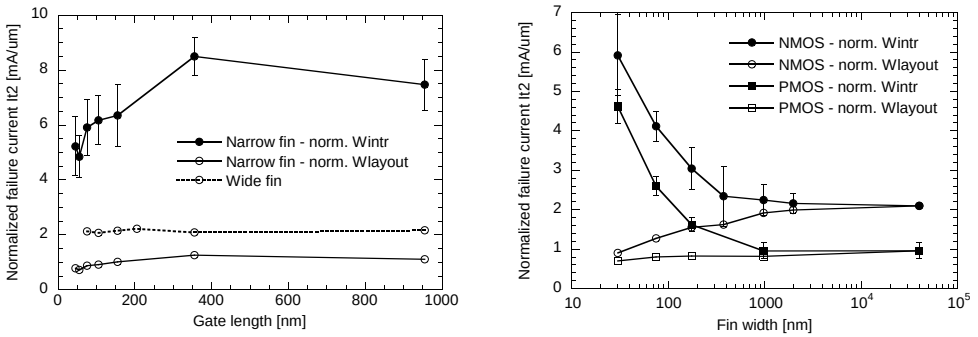
Fig. 0.5 toont een set van TLP metingen op een N-type FinFET in bipolaire mode voor zowel structuren met smalle als met brede fins. Door de SOI-technologie is de basis van de bipolaire structuur vlottend, zodat er geen typische 'snapback' karakteristiek in de TLP-IV curve waargenomen wordt. De structuren gaan zonder spanningsterugval over naar de bipolaire werkingsmodus wanneer hun houdspanning V_h bereikt wordt. De faalstroom It_2 is sterk afhankelijk van de verschillende geometrische parameters.

In Fig. 0.6 wordt It_2 getoond als functie van gate lengte (links) en fin breedte (rechts). Voor N-type structuren met smalle fins is er een verbetering merkbaar in It_2 bij grotere gate lengte door een meer uniforme faling tussen de verschillende fins. Deze verbetering is zichtbaar voor de twee gebruikte normalizaties. De intrinsieke performantie wordt geanalyzeerd door te normalizeren ten opzichte van W_{intr} die de effectieve silicium breedte aanduidt, en de layout efficiëntie ten opzichte van W_{layout} die de totaal gebruikte layout breedte weergeeft. Wanneer de gate lengte echter te groot wordt, wordt het gedissipeerde vermogen te groot, zodat It_2 terug daalt. Voor brede fin structuren is er geen afhankelijkheid van It_2 ten opzichte van de gate lengte.

Wanneer de afhankelijkheid van It_2 ten opzichte van W_{fin} bekeken wordt in



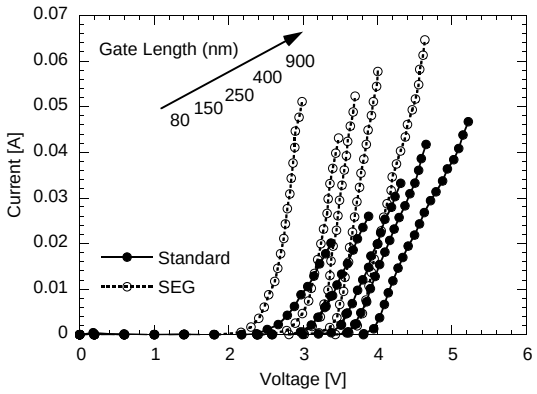
Figuur 0.5: TLP-IV curves voor N-type FinFET in bipolaire mode met verschillende gate lengtes voor zowel smalle (400 fins van 30 nm W_{fin}) als brede (enkelvoudige 40 μm) structuren.



Figuur 0.6: Genormalizeerde faalstroom It_2 als functie van de gate lengte voor smalle en brede fin N-type FinFET structuren in bipolaire mode (links). Genormalizeerde It_2 als functie van de fin breedte voor FinFET structuren met 75 nm gate lengte in bipolaire mode (rechts).

Fig. 0.6 (rechts), is er een duidelijk verschillende trend merkbaar afhankelijk van welke normalizatie gehanteerd wordt. Zowel voor NMOS als PMOS structuren stijgt de intrinsieke It_2 wanneer de fin breedte W_{fin} vermindert. Deze verbetering is te verklaren door een betere koeling van smalle fins, in vergelijking met brede fins. Aan de andere kant verslechtert de layout efficientie van It_2 bij smallere W_{fin}, doordat de fin-spacing S overhead een steeds groter deel van de layout oppervlakte in beslag neemt (Fig. 0.4).

Selective Epitaxial Growth (SEG) is standaard nodig om de toegangsweerstand van de FinFET transistoren te verminderen. Door hiervan gebruik te maken wordt het siliciumvolume van de source en drain landing pads vergroot, alsook het volume van het gedeelte van de fins tussen de landing pads en de gate, zie Fig. 0.4. Dit resulteert in ongeveer een verdubbeling van It_2, die gepaard gaat

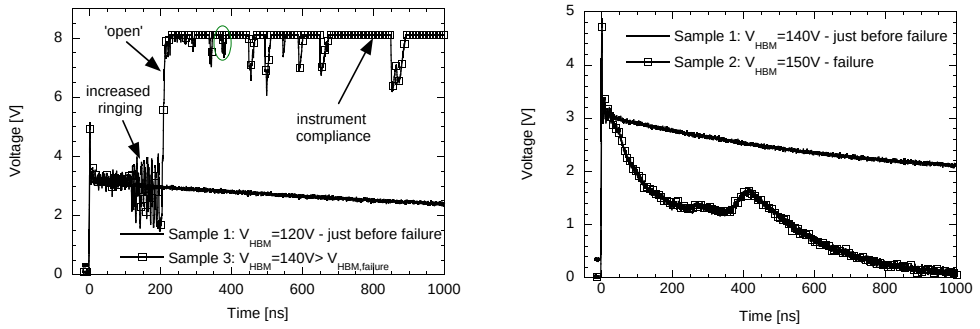


Figuur 0.7: TLP-IV curves van N-type FinFET structuren in bipolaire mode als functie van gate lengte voor wafers geprocessed met en zonder SEG. De structuren hebben een fin breedte van 25 nm en 225 fins in parallel.

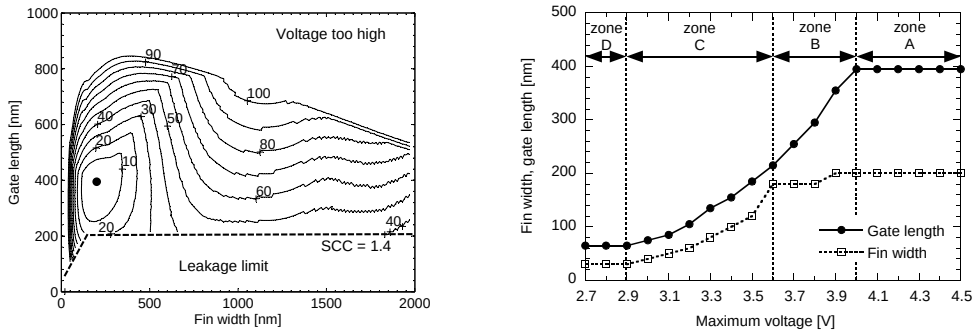
met een drastische vermindering van de aan-weerstand R_{on}, zoals te zien is in de TLP-IV curves van NMOS FinFET transistoren in bipolaire mode in Fig. 0.7.

Ook het gebruik van stress om de mobiliteit van de transistoren te verbeteren heeft een meetbare invloed op het ESD gedrag van de FinFET transistoren. In Fig. 0.8 worden de HBM spanningsgolven vlak voor en na faling weergegeven voor transistoren in bipolaire mode zonder stress (links) en met stress (rechts). Zonder stress is er bij faling eerst een oscillatie meetbaar op de spanningsgolfvorm, todat deze divergeert naar een hoog-resistieve 'open' conditie. Deze spanningsoscillaties duiden op een hoge instabiliteit rond het falingsstroomniveau. Bij faling van een groepje fins zal eerst de spanning dalen doordat er lokaal een kortsluiting tussen source en drain gevormd wordt. Omdat het aantal fins bij faling eerder beperkt is, zal de hoge stroom die vervolgens door deze kortgesloten fins vloeit, deze fins opblazen, zodat ze 'open' worden. Hierdoor zal de spanning terug stijgen. Vervolgens faalt het volgende groepje fins (oscillaties), totdat uiteindelijk alle fins 'open' zijn. Bij het gebruik van stress faalt de structuur op een hoger HBM stress niveau, en ook het falingsmechanisme is anders. Bij faling daalt de spanning tot een 'kortsluiting' doordat er meer fins tegelijkertijd falen.

Door de complexe afhankelijkheid van de verschillende ESD performantie parameters (lekstroom, houdspanning, aan-weerstand en faalstroom) van de geometrische en process parameters is het nodig om gebruik te maken van een ontwerpmethodologie om een optimale ESD oplossing te bekomen die rekening houdt met de verschillende randvoorwaarden. Deze ontwerpmethodologie gebruikt de geëxtraheerde ESD performantie parameters uit de beschikbare meetdata als input. Door middel van lineaire interpolatie kunnen de ESD

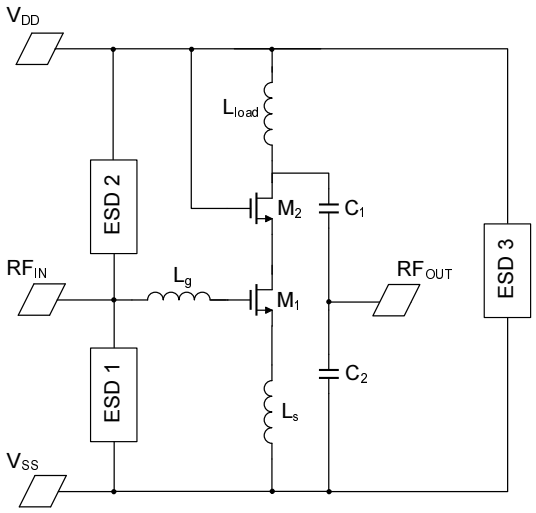


Figuur 0.8: HBM-spanningsgolfvorm voor en tijdens faling van een FinFET structuur zonder stress (links) en met stress (rechts) in bipolaire mode met 75 nm gate lengte. Wanneer de structuur zonder stress faalt, groeit eerst de oscillatie op de spanningsgolfvorm totdat ze divergeert naar een hoog-resisitieve 'open' conditie (links). Wanneer de structuur met stress faalt daalt de spanning naar een 'kortsluiting' (rechts).



Figuur 0.9: Percentage van vergrootte oppervlakte vergeleken met de optimale oplossing (punt) dat voldoet aan de opgelegde ontwerp limieten van 1 kV HBM, 4 V V_{max} en zeer goede controle over de korte-kanaaleffecten (SCC>1.4) in bipolaire mode (links). Afhankelijkheid van de optimale L_g en W_{fin} als functie van V_{max} (rechts).

performantie parameters bepaald worden voor de verschillende geometrische en process parameters. Op basis van een wiskundige algoritme kan de optimale oplossing vervolgens bepaald worden. Fig. 0.9 toont links de ideale gate lengte en fin breedte combinatie (aangeduid door het punt) om een ESD specificatie van 1 kV HBM en maximaal 4 V spanningsval te halen met de kleinst mogelijke layout. De ideale oplossing is dus niet een structuur met hele smalle of hele brede fins, maar ergens tussenin. Wanneer van dit optimum afgeweken wordt vergroot de benodigde layoutoppervlakte om aan de randvoorwaarden te voldoen heel snel, waarmee het nut van de ontwerpmethodologie bewezen wordt. Verder zorgt deze ontwerpmethodologie ook voor een dieper inzicht. Wanneer bijvoorbeeld voor een 1 kV HBM specificatie de maximale toegelaten



Figuur 0.10: Basis van on-chip ESD bescherming. Het circuit is een lage ruis versterker (LNA) die gebruikt wordt als demonstrator. ESD1-3 zijn de ESD beschermingsstructuren.

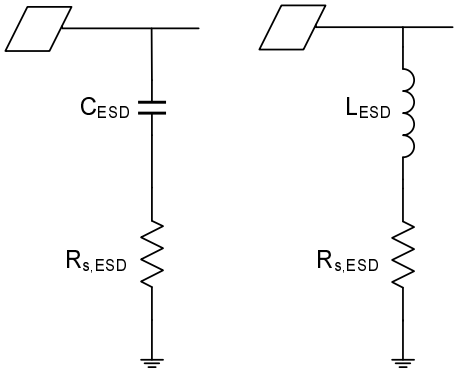
spanning verminderd wordt van 4.5 tot 2.7 V, kan men in Fig. 0.9 (rechts) verschillende zones onderscheiden hoe de optimale gate lengte en fin breedte zich moeten gedragen om tot het optimum te komen.

Al deze resultaten tonen aan dat de ESD gevoeligheid van FinFET structuren geen spelbreker is voor de introductie van FinFETs voor geavanceerde nanotechnologieën, zolang ESD reeds beschouwd wordt tijdens de technologieontwikkeling. Maar zelfs met deze kennis blijft het ontwerp van ESD bescherming voor FinFET technologie een uitdaging.

ESD Bescherming voor Smalbandige RF CMOS Circuits

In een RF front-end, is de lage ruis versterker (LNA) één van de kritische elementen. Doordat hij via een antenne met de buitenwereld verbonden is, heeft de LNA ESD bescherming nodig. Deze ESD bescherming moet zodanig ontworpen worden dat de RF performantie van de LNA zo weinig mogelijk beïnvloed wordt. Een generieke ESD protectie wordt getoond in Fig. 0.10. Elementen ESD1 en ESD2 zorgen ervoor dat de ESD stroom van de RF input afgeleid wordt naar de voeding en grond. ESD3 zorgt voor ESD bescherming tussen voeding en grond.

Om zo weinig mogelijk impact te hebben op de RF performantie van de LNA wordt traditioneel de capaciteit van de elementen ESD1 en ESD2 zo laag mogelijk gehouden. Een lagere capaciteit betekent echter kleinere ESD elementen en dus ook lagere ESD performantie. Het equivalente schema van een capacitieve ESD beschermingsstructuur wordt getoond in Fig. 0.11 (links). Bij



Figuur 0.11: Equivalent schema van capacitieve (links) ESD beschermingsstructuren, zoals diodes of grounded gate NMOS, en inductieve (rechts) ESD beschermingsstructuren.

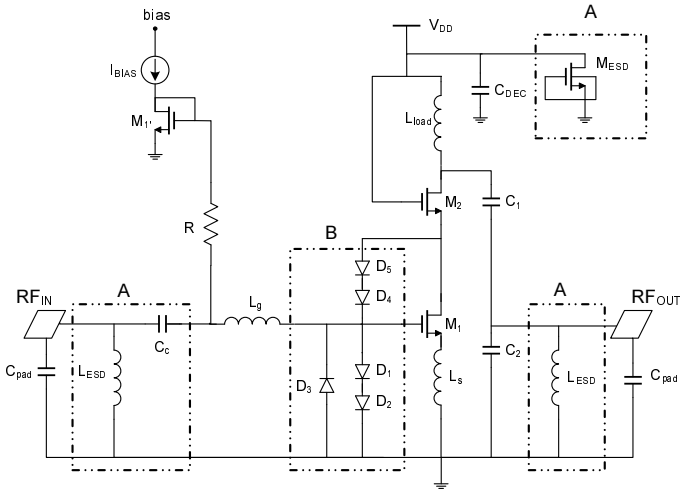
stijgende RF frequentie zal de impedantie volgens (1) verminderen, waardoor de maximale toegestane capaciteit en dus grootte van de ESD structuur omwille van de RF specificaties van de LNA ook vermindert. Capacitieve ESD bescherming wordt dus moeilijker en moeilijker naarmate de RF frequentie hoger wordt, en uiteindelijk zelfs onbruikbaar.

$$|Z_{ESD}| = \left| R_{s,ESD} + \frac{1}{j\omega_{RF} C_{ESD}} \right| = \sqrt{R_{s,ESD}^2 + \frac{1}{\omega_{RF}^2 C_{ESD}^2}} \tag{1}$$

Men kan ook gebruik maken van inductieve ESD bescherming zoals getoond in Fig. 0.11 (rechts). De impedantie hiervan verhoogt met stijgende RF frequentie volgens (2), zodat deze oplossing beter wordt naarmate de frequentie hoger wordt. De spoel naar grond wordt toegevoegd als 'plug-and-play', dus zonder het oorspronkelijke RF ontwerp te wijzigen.

$$|Z_{ESD}| = |R_{s,ESD} + j\omega_{RF} L_{ESD}| = \sqrt{R_{s,ESD}^2 + \omega_{RF}^2 L_{ESD}^2} \tag{2}$$

Om de limieten van capacitieve en het potentieel van inductieve ESD bescherming aan te tonen wordt een identieke 5 GHz LNA in een 90 nm CMOS technologie gebruikt als demonstrator. Het schema van de LNA met de inductieve ESD bescherming L_{ESD} wordt getoond in Fig. 0.12. De ontkoppelcapaciteit C_C is nodig in combinatie met L_{ESD} om de transistor M_1 van instelspanning te kunnen voorzien. Door toevoegen van de klassieke dual diode bescherming of van de inductieve ESD bescherming worden de RF specificaties van de LNA gehaald. Er is echter een groot verschil in ESD performantie.



Figuur 0.12: Het schema van de lage ruis versterker met een spoel naar grond als ESD bescherming. Rechthoek A duidt de standaard ESD bescherming aan en B de extra ESD bescherming.

De LNA met dual diode ESD bescherming faalt bij 500 V HBM stress tussen RF_{IN} en V_{SS} omdat de maximale toegelaten spanning over het gate oxide van transistor M_1 overschreden wordt. Door een spoel als ESD bescherming te gebruiken kan de ESD stroom in deze stress combinatie meteen van RF_{IN} naar V_{SS} gaan, zonder over de powerclamp M_{ESD} te hoeven gaan. Echter, wanneer deze ESD stroom door L_{ESD} gaat, wordt er een overspanning opgebouwd, die via de ontkoppelcapaciteit C_C op de gate van M_1 gekoppeld wordt. Hierdoor kan de LNA beschermd worden tot 2.5 kV HBM. Door gebruik te maken van extra kleine diodes aan de gate van M_1, Box B in Fig. 0.12, wordt deze overspanning beperkt, en stijgt het HBM beschermingsniveau tot 5.5 kV met slechts minimale RF impact. Het HBM niveau kan verder nog verhoogd worden door gebruik te maken van Above-IC spoelen. Door hun hogere kwaliteitsfactor vermindert de overspanning en stijgt het HBM niveau tot 6 en >8 kV zonder en met extra diodes respectievelijk.

Omwille van de overspanningen die gegenereerd worden wanneer stroom door een spoel vloeit, is het nodig om naast HBM ook de CDM performantie van de inductieve ESD bescherming te bestuderen. Dit gebeurt aan de hand van on-chip VFTLP metingen tussen de verschillende mogelijke pin-combinaties. Zo kunnen zwakke ESD paden opgespoord en gecorrigeerd worden. Een overzicht van de VFTLP resultaten tussen RF_{IN} en V_{SS} wordt gegeven in Tabel 0.1. De extra diodes verhogen de VFTLP performantie, net zoals bij HBM, terwijl gebruik van Above-IC zorgt voor ongeveer een verdubbeling van de VFTLP sterkte.

Tabel 0.1: Samenvatting van VFTLP meetresultaten (200 ps stijgtijd en 3 ns pulsbreedte).

VFTLP RF_{IN}+ V_{SS}-	**Normal BEOL**	**Above-IC**
No clamping diodes	0.9 A	1.7 A
With clamping diodes	1.3 A	2.7 A

Tabel 0.2: Samenvatting van ESD meetresultaten van de 60 GHz LNA.

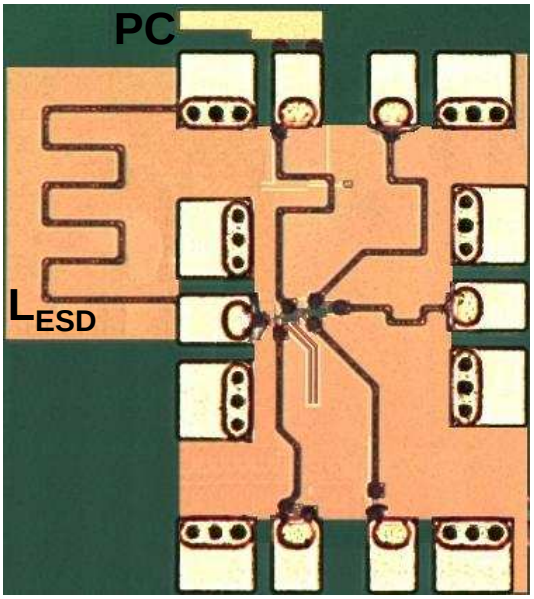
	RF_{IN}+V_{SS}-	V_{DD}+RF_{IN}-
HBM [kV]	>8 kV	6.3 kV
VFTLP [A]	>10.6 A	7.3 A

Inductieve ESD bescherming is niet afhankelijk van de front-end, maar wordt voornamelijk bepaald door de back-end kwaliteit, die eerder constant blijft bij technologieschaling. Daarom wordt een even goed HBM beschermingsniveau, namelijk >5 kV, verkregen voor een 5 GHz LNA met inductieve bescherming, geïmplementeerd in zowel een 45 nm planaire als een 45 nm FinFET technologie. Bij gebruik van de klassieke dual-diode ESD bescherming zakt de ESD performantie van 2.5 kV voor de planaire technologie tot 850 V voor de FinFET technologie door de vermindering in sterkte van de ESD diodes.

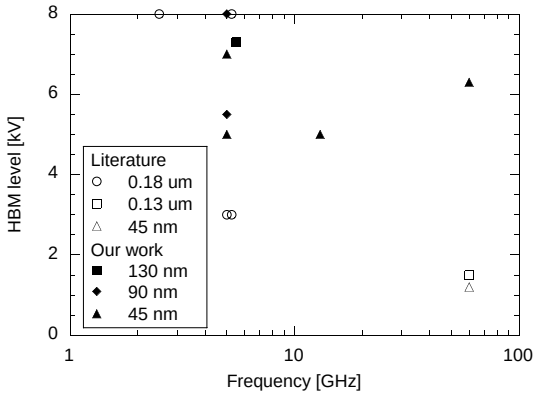
Door het verhogen van de RF frequentie kunnen spoelen met lagere inductantie gebruikt worden met minder wikkelingen, waardoor de benodigde oppervlakte verkleint alsook de serieweerstand. Doordat zowel de LdI/dt als de $R * I$ component van de overspanning verminderen, verbeteren zowel de HBM als de CDM performantie. Wanneer de RF frequentie hoog genoeg is, kan de spoel geïmplementeerd worden als een simpele $\lambda/4$ microstriplijn die de RF ingang kortsluit naar de grond. Een voorbeeld hiervan wordt getoond in Fig. 0.13 voor een 60 GHz LNA. Extreem goede ESD resultaten, zowel HBM als VFTLP, kunnen bereikt worden. Een samenvatting van de meetresultaten wordt gegeven in Tabel 0.2.

Door gebruik te maken van inductieve ESD bescherming en deze verder te optimalizeren met extra diodes en een Above-IC back-end, kan een zeer hoge ESD bescherming verkregen worden voor RF circuits met hoge werkingsfrequentie en geïmplementeerd in de meest geavanceerde CMOS technologieën. Het behaalde HBM resultaat als functie van de RF frequentie van onze circuits wordt vergeleken met de literatuur in Fig. 0.14. Het is duidelijk dat inductieve ESD bescherming de beste RF-ESD resultaten behaalt.

Tot 5 GHz kunnen de klassieke dual diodes gebruikt worden voor RF-ESD

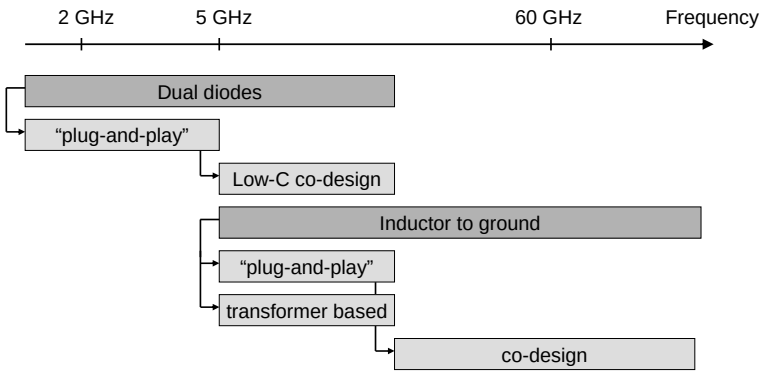


Figuur 0.13: Micrograph van een 60 GHz LNA met $\lambda/4$ microstriplijn als ESD bescherming.



Figuur 0.14: Vergelijking van ons werk (volle symbolen) met andere gepubliceerde smalband CMOS LNA resultaten (open symbolen). De HBM performantie [kV] is geplot als functie van RF frequentie [GHz].

bescherming. Wanneer men deze wil blijven gebruiken boven 5 GHz moet men de parasitaire capaciteit mee in het RF ontwerp opnemen, de zogenaamde co-design aanpak, evenwel met een beperkte ESD bescherming als resultaat. Vanaf 5 GHz kan inductieve ESD bescherming gebruikt worden. Om geen extra oppervlakte te gebruiken voor de ESD beschermingsspoel, kan deze onder een RF matching spoel geschoven worden, waardoor een transformator gemaakt wordt. Deze aanpak vereist een complexer RF ontwerp. Naarmate



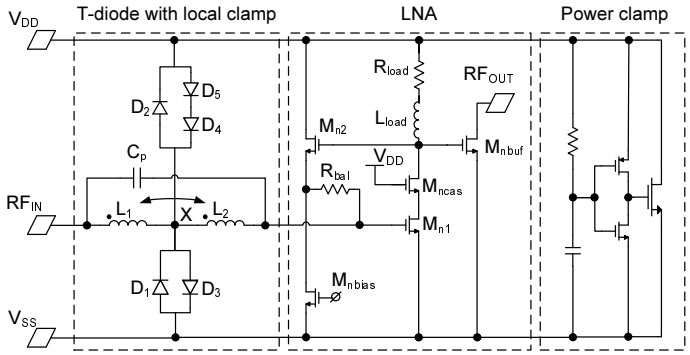
Figuur 0.15: Smalbandige RF-ESD beschermingsmethodologie als functie van applicatie frequentie.

de RF frequentie hoger wordt, wordt de benodigde oppervlakte van de ESD beschermingsspoel kleiner, zodat de eenvoudige spoel-naar-grond methode te verkiezen valt boven de transformator. Bij nog hogere RF frequenties kan het wenselijk zijn om de ESD spoel in het RF ontwerp op te nemen om zo bijvoorbeeld de extra bondpadcapaciteit weg te tunen. Een overzicht van de RF-ESD beschermingsmethodologie als functie van RF frequentie wordt weergegeven in Fig. 0.15.

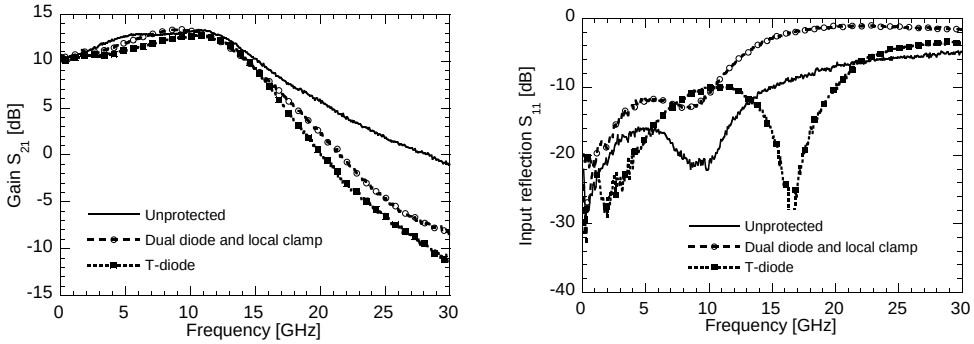
ESD Bescherming voor Breedbandige RF CMOS Circuits

Breedband RF circuits worden meer en meer geïmplementeerd in CMOS, en daarom is er een nood voor gepaste ESD bescherming voor deze circuits. Smalbandige ESD oplossingen, zoals beschreven in de vorige sectie, kunnen niet gebruikt worden omdat ze slechts werken in een smalle band rond een bepaalde frequentie. De bestaande breedband RF-ESD oplossingen zijn beperkt in RF performantie, vermogenverbruik, ESD performantie of gebruiken te veel silicium oppervlakte. Daarom worden in dit hoofdstuk twee nieuwe breedbandige RF-ESD oplossingen gepresenteerd.

De capacitieve belasting van een klassieke dual diode ESD oplossing zorgt ervoor dat deze methode slechts beperkt gebruikt kan worden bij hogere RF frequenties, zoals besproken in de vorige sectie. Door gebruik te maken van een transformator rond de ESD diodes, kan hun parasitaire capaciteit onzichtbaar gemaakt worden over een hele brede frequentieband, de zogenaamde T-diode oplossing. Op deze manier wordt een artificiële transmissielijn gemaakt die zowel een ingangs- als een uitgangsimpedantie van 50 Ω heeft. Omdat op deze manier redelijk grote capaciteiten kunnen weggetuned worden, kunnen we zelfs gebruik maken van 'lokale clamping' aan de RF ingang, zoals getoond in Fig. 0.16. Diodes D_1 en D_2 vormen de klassieke dual diode oplossing, terwijl diodes D_3-D_5 ervoor zorgen dat de ESD stroom lokaal aan de RF-ingang kan



Figuur 0.16: Schema van ESD beschermde wideband RF LNA met T-diode en lokale clamping.

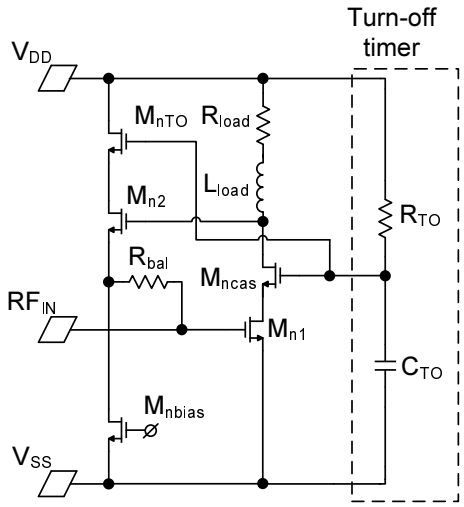


Figuur 0.17: Gemeten versterking S_{21} (links) en input matching S_{11} (rechts) van: onbeschermde LNA, LNA met dual-diode en lokale clamp ESD bescherming, en T-diode ESD bescherming met lokale clamp.

wegvloeien, zonder over de power clamp te moeten gaan. Het aantal diodes in serie van de lokale clamping hangt af van de benodige instelspanning voor de LNA. L_1, L_2 en C_p, Fig. 0.16, vormen samen met de ESD diodes de T-diode. Op deze manier wordt een DC-tot-16.1 GHz breedband LNA, geïmplementeerd in 90 nm digitale CMOS, beschermd tegen ESD.

Wanneer men deze dual diode met lokale clamping gebruikt zonder de T-diode, degradeert de input matching bandbreedte met 3 GHz, ten opzichte van het onbeschermde circuit volgens Fig. 0.17 (rechts). Door gebruik te maken van de T-diode als ESD bescherming verbetert de input matching van de breedband LNA zelfs van 14.5 GHz voor de onbeschermde LNA tot 20.1 GHz, Fig. 0.17 (rechts), terwijl de versterking nagenoeg ongewijzigd blijft, Fig. 0.17 (links). De HBM performantie verbetert van 1.5 kV zonder lokale clamping tot 4 kV met lokale clamping voor stress tussen V_{DD} en RF_{IN}.

Bij bepaalde pin combinaties kan tijdens ESD stress een parasitair stroompad



Figuur 0.18: LNA topologie met ESD afschakelcircuit.

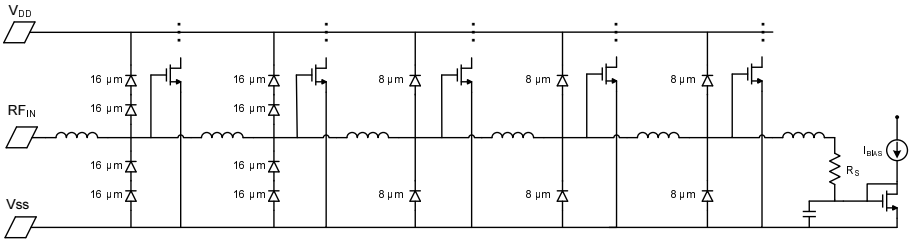
gevormd worden door de LNA kern, bijvoorbeeld door de feedback transistor M_{n2} of de cascode transitoren M_{n1} en M_{ncas}, Fig. 0.16. Een elegante methode bestaat erin deze parasitaire paden uit te schakelen tijdens ESD door middel van een ESD afschakelcircuit, Fig. 0.18. De RC-timer R_{TO} en C_{TO} zorgen ervoor dat beide parasitaire stroompaden afgeschakeld zijn tijdens ESD stress. Deze methode kan eenvoudig geïmplementeerd worden en neemt geen extra plaats in, omdat in een RF circuit typisch heel veel ontkoppelcapaciteiten aanwezig zijn die gebruikt kunnen worden als C_{TO}.

Voor stress tussen V_{DD} en RF_{IN}, vormt de feedbackweerstand R_{bal} de zwakke schakel. Zelfs met lokale clamping vemindert de HBM performantie van 4 kV tot 2.25 kV door toevoeging van R_{bal}. De HBM sterkte wordt terug hersteld tot 4 kV door gebruik te maken van het extra afschakelcircuit. Een overzicht van de ESD resultaten wordt weergegeven in Tabel 0.3. Deze afschakelmethode is een algemene ESD beschermingstechniek die niet beperkt wordt tot het gebruik voor breedband RF circuits.

Een tweede breedband RF oplossing is een optimalisatie van de gedistribueerde ESD bescherming die typisch gebruikt wordt bij gedistribueerde versterkers (Distributed Amplifier DA). Bij dergelijke ESD bescherming worden er ESD componenten voorzien aan iedere versterkingstrap. Het geheel van de verschillende ESD componenten moet een voldoende ESD bescherming geven. Wanneer de ESD elementen in de verschillende trappen even groot genomen worden (Equally Sized Distributed ESD ES-DESD), kunnen de versterkingstrappen identiek ontworpen worden, maar de ESD efficiëntie vermindert bij iedere trap. Een optimalizatie hiervan maakt de ESD elementen in de eerste trap het grootste en verkleint deze bij iedere volgende trap. Een voordeel hiervan is

Tabel 0.3: Samenvatting van on-wafer HBM meetresultaten [kV].

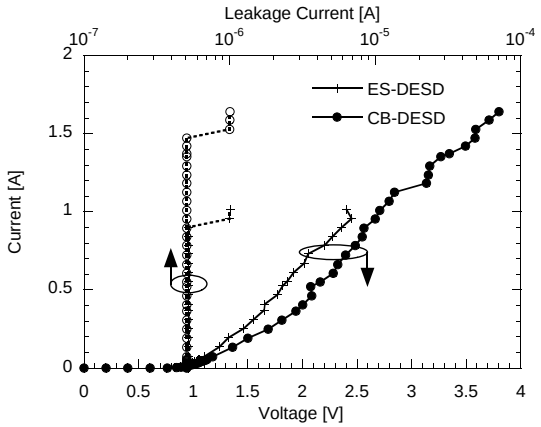
$R_{\mathbf{bal}}$	**Local clamping**	**Turn-off 500 ns**	**Turn-off 200 ns**	**Turn-off 20 ns**	**HBM [kV]** $V_{\mathbf{DD}}$+$RF_{\mathbf{IN}}$-	**HBM [kV]** $V_{\mathbf{DD}}$+$V_{\mathbf{SS}}$-
-	-	-	-	-	1.5	3
-	X	-	-	-	4	-
X	X	-	-	-	2.25/2.4	4.75
X	X	X	-	-	4	7
-	-	X	-	-	3.75	6.5
-	-	-	X	-	3.75	-
-	-	-	-	X	3.75	-



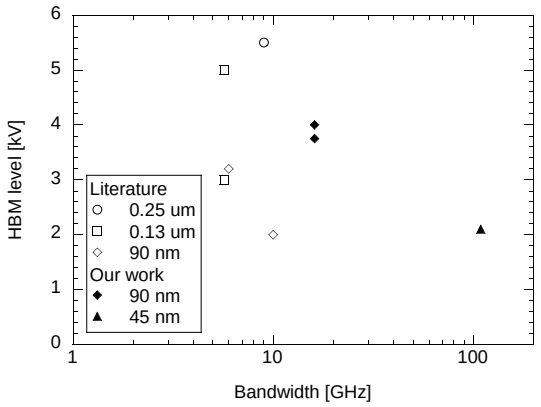
Figuur 0.19: Schema van de gate transmissie lijn van de DA met CB-DESD bescherming.

een betere algehele ESD efficiëntie, maar hierbij moet iedere versterkingstrap afzonderlijk ontworpen worden. Om het RF ontwerp zo eenvoudig mogelijk te houden en toch een betere ESD performantie dan bij ES-DESD te halen kan men een centraal gebalanceerde gedistribueerde ESD (Center Balanced Distributed ESD CB-DESD) strategie gebruiken. Hierbij worden de ESD diodes in de eerste twee versterkingstrappen dubbel zo groot gemaakt en met twee in serie geplaatst, zoals te zien is in Fig. 0.19. Op deze manier is de totale parasitaire capaciteit van de eerste twee trappen ongeveer even groot als in de laatste drie trappen en kunnen bijgevolg de versterkingstrappen identiek blijven. Deze oplossing is geïmplementeerd voor een 1-110 GHz DA met vijf trappen, in een 45 nm CMOS technologie met Above-IC back-end.

Omdat de eerste twee trappen twee diodes in serie hebben zal tijdens ESD stress de derde trap als eerste aangaan. Vervolgens wordt de ESD stroom verspreid over de vierde en vijfde trap, totdat de spanning aan de eerste trap hoog genoeg is zodat de twee diodes beginnen geleiden. Op dit moment nemen dan ook de eerste trap en uiteindelijk de tweede trap deel aan de ESD geleiding, zodat de ESD stroom over de vijf trappen verdeeld wordt. Doordat de stroom meer uniform verdeeld wordt over de verschillende trappen wordt een 65 % hogere faalstroom bekomen bij CB-DESD tijdens TLP metingen tussen RF_{IN}+ en V_{DD}- vergeleken met ES-DESD, zoals te zien is in Fig. 0.20.



Figuur 0.20: TLP-IV meting voor stress tusssen $RF_{IN}+$ en V_{DD}-. CB-DESD heeft 65 % verbeterde It_2 ten opzichte van ES-DESD.



Figuur 0.21: Vergelijking van ons werk (volle symbolen) met andere gepubliceerde breedband CMOS LNA resultaten (open symbolen). De HBM performantie [kV] is geplot als functie van RF frequentie [GHz].

In Fig. 0.21 worden deze twee nieuwe breedband RF-ESD oplossingen vergeleken met de beschikbare oplossingen in literatuur. Met de T-diode en CB-DESD kan een heel goede ESD bescherming verkregen worden voor hele breedbandige RF circuits, zelfs geïmplementeerd in zeer geavanceerde CMOS technologieën.

Conclusies

ESD is geen spelbreker voor de introductie van FinFET technologie, op voorwaarde dat een ontwerpmethodologie gebruikt wordt om het delicate layout optimum en de geschikte process opties te selecteren. Verder kunnen er ESD oplossingen geïmplementeerd worden voor smal- en breedbandige RF circuits die zowel een uitstekende RF als ESD performantie halen.

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Chapter 1

Introduction

The reliability of the microelectronic devices and circuits is a major factor that determines both their manufacturability and application lifetime. Design for reliability should be implemented during technology, device and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. The specific reliability problem studied in this PhD is caused by ElectroStatic Discharge (ESD) events.

1.1 Reliability in Advanced CMOS Technologies

With the continuous downscaling of Complimentary Metal Oxide Semiconductor (CMOS) technologies, reliability has become a major bottleneck, on the one hand due to the continuous increase in internal electrical fields and current densities, and on the other hand due to the introduction of new materials and device architectures with unknown reliability behavior. When the device geometries are scaled into the range needed for 65 nm CMOS technologies and below, the available reliability margins are strongly reduced, in some cases even down to zero. As a result, the reliability community will be obliged to look more in detail to what exactly is determining these margins, and how we can change our reliability assessment methodology to gain new reliability space for the most advanced technologies.

A big variety of failure mechanisms needs to be investigated, such as hot carrier degradation, time-dependent dielectric breakdown, negative bias temperature instability, electromigration, stress voiding, interconnect dielectric instability and breakdown, and electrostatic discharge. Each of these reliability mechanisms has its own set of issues associated with technology scaling. This PhD focusses on reliability problems associated with ESD events.

Figure 1.1: The Burj Dubai is world's tallest ESD protection structure.

1.2 Electrostatic Discharge in Micro-Electronics

The most famous type of ESD is lightning. In fact, lightning is nothing else but ESD on a large scale, with voltages up to 10^7 V and currents up to 30 kiloamperes. The world's tallest and most expensive ESD protection structure is the Burj Dubai skyscraper located in Downtown Dubai, United Arab Emirates. It has a giant lightning-rod on its top to safely discharge the lightning events as shown in Fig. 1.1.

Triboelectric charging of objects results from electron transfer during friction of two objects. For example, a person can acquire charges by simply walking across a room. ESD is the transfer of an electrostatic charge which occurs when two objects of different electrostatic potential are brought close together.

The amount of charge induced depends on various parameters, such as the position of the relevant materials in the triboelectric series, the relative humidity, the texture of the material surfaces, speed of separation, area of contact, etc. When such a charged person or object then approaches a grounded conductor, for example a pin of a packaged Integrated Circuit (IC), an Electrostatic

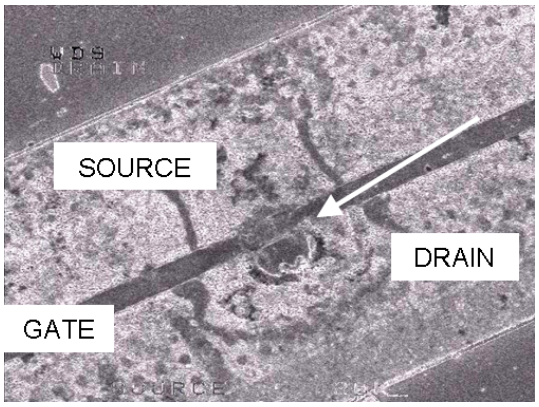

Figure 1.2: SEM picture of a grounded gate NMOS stressed in forward diode mode. A short between source and drain is observed [Thijs 03].

Discharge (ESD) event occurs, characterized by a high current (∼A) during a few ns. An ESD event of amplitude of 3000 V or below (corresponding to a current level of typically 2 A) will not be detected by humans by sensory perception. However, such ESD event can cause various types of damage in an IC, resulting in catastrophic failure.

An example of ESD damage is shown in Fig. 1.2, where silicon melting occured due to current filamentation. Other ESD failure types are for example contact spiking and gate oxide breakdown. Gate oxide breakdown is caused by voltage overshoots which occur when the ESD protection device does not turn on fast enough. Several examples will be shown throughout this thesis.

ESD problems can be avoided either by prevention, achieved by taking antistatic measures to avoid buildup of static charges, or by adding adequate on-chip protection circuits to protect the inner circuits against ESD. The focus of this PhD is on protection, rather than on prevention.

According to the ESD Association [ESDA], on average ESD destroys about 16 to 22 % of electronic components before they are installed into a system. After assembly, anywhere from 33 to 70 % of digital devices fail soon after customers purchase because ESD may only damage a component, enabling it to function for a brief time before total failure [Schu 08]. ESD represents anually a loss of billions of dollars due to repair, rework, shipping, labor and overhead costs associated with the damage, which highlights the importance of fundamental understanding of ESD aspects and design of efficient ESD protection.

The constantly changing technologies and applications make the design of proper protection very challenging. Two major challenges lie ahead for the ESD design engineer. Firstly, as CMOS technology keeps scaling down, new technology options arise and their ESD robustness should be preferably consi-

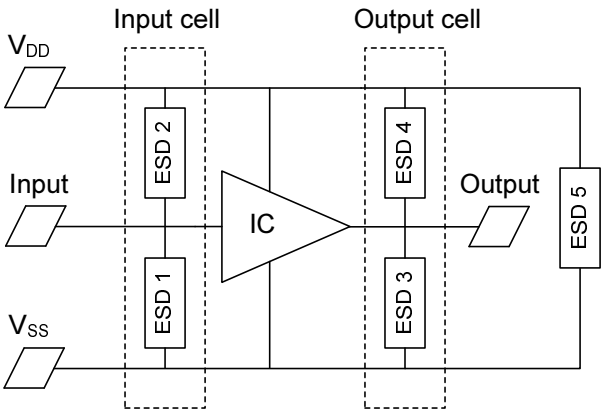

Figure 1.3: Generic on-chip ESD protection methodology. ESDx are the ESD protection elements.

dered in the early technology development phase as these technology evolutions might lead to a 'drastic' reduction in ESD performance. Secondly, CMOS technology scaling and development allows for Radio-Frequency (RF) design in CMOS. These applications have very stringent requirements regarding noise and impedance matching, which are often considered to be incompatible with good ESD performance [Vold 06]. This even leads to some RF products without any ESD protection. When RF applications are processed in these advanced technologies, the two previous mentioned challenges are even combined.

1.3 Basic Concepts of ESD Protection

To avoid circuit damage during ESD stress, ESD protection elements need to be placed around the integrated circuit (IC), which can safely remove the ESD current, similar as the lightning-rod in Fig. 1.1. The ideal ESD protection element is basically a switch which is open during normal operation and closed during ESD. The basic ESD protection elements are covered in section 1.4.

A generic on-chip ESD protection methodology is shown in Fig. 1.3, where ESDX denotes the different ESD protection elements, placed around the IC. These elements can divert the ESD current either in a single direction, e.g. a diode, or in both directions, e.g. a grounded-gate NMOS. The latter are called bi-directional ESD protection elements. By placing adequate ESD protection elements, a pre-defined current path is created for the ESD current, hence avoiding core damage. For full chip ESD protection, all pin-to-pin combinations need to be protected. Therefore, ESD protection is needed on all inputs, outputs, between power lines and grounds.

Good ESD protection elements should

- clamp the ESD voltage to shunt the ESD stress current
- turn-on fast enough
- carry large currents
- have low on-resistance
- occupy minimum area at the bond pad
- have minimum capacitance
- introduce minimum series resistance
- be immune to process drifts and process location
- be robust for numerous pulses
- offer protection for various ESD stress models (HBM, CDM, etc.)
- not interfere with IC functional testing.

The ESD design window can be defined as the region in which the ESD protection elements need to operate, as shown in Fig. 1.4. On one hand, the window is limited by the normal operation regime, with which the ESD protection should not infere. On the other hand, the window is limited by the IC reliability, caused by gate oxide breakdown, turn-on of parasitics, etc. A typical snapback device IV characteristic is shown in the ESD design window in Fig. 1.4. In such devices, at a certain moment a parasitic device inside will turn on which allows efficient dissipation of the ESD current. Examples are shown in section 1.4. These devices need to turn on at their trigger point (Vt_1, It_1) before core damage occurs. The holding voltage (V_h) denotes the minimum voltage to maintain the parasitic device action and should be at a safe level above V_{DD} to avoid latchup issues. After snapback, the parasitic device dissipates the ESD current with a certain on-resistance (R_{on}) until its failure point (Vt_2, It_2) is reached. It_2 should be above the minimum required ESD current level.

1.4 Basic ESD Protection Devices

In this section, the basic ESD protection devices (diode, grounded-gate NMOS (ggNMOS), Silicon Controlled Rectifier (SCR) and active clamp) are summarized. Several measurement examples are presented further in this thesis.

Diode

Diodes are excellent ESD protection devices when operated under forward bias. A cross-section is shown in Fig. 1.5. The anode is formed by the P+ terminal and the cathode by the N+ terminal. Anode and cathode can be separated by either STI isolation or by a poly gate, and their difference in ESD performance will be discussed further in section 2.5.3.1. The diode can be created either in an nwell or pwell. When placing diodes in series, nwell diodes are required to avoid shortening of the P+ anodes via the P-substrate resistance.

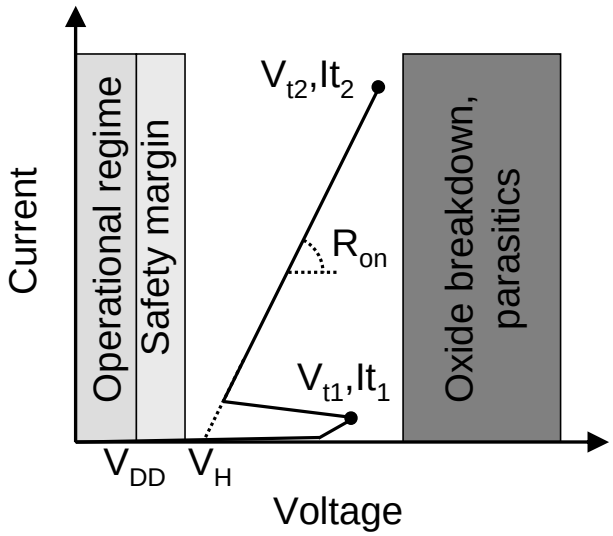

Figure 1.4: ESD design window.

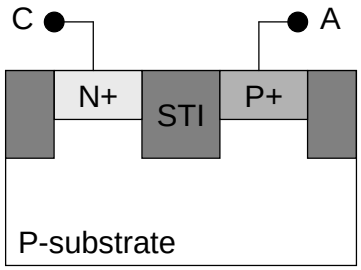

Figure 1.5: Cross-section of a diode.

Diodes have a low turn-on voltage around 0.7 V and exhibit a low on-resistance. They have a high ESD current capability, up to 50 mA/μm. Under reverse bias however, they have a high turn-on voltage and high on-resistance, leading to a low ESD current capability. Therefore, diodes can only conduct current efficiently in a single direction, namely in forward bias mode.

Grounded-gate NMOS

The cross-section of a grounded-gate nMOS (ggNMOS) is shown in Fig. 1.6. In a ggNMOS, the N+ drain forms the anode, while the source, gate and bulk are shorted together and form the cathode. Under normal V_{DD} bias conditions, the ggNMOS is not conducting as the gate terminal is grounded. However, when the voltage at the drain rises high enough, avalanche breakdown of the drain to substrate junction will occur generating electron-hole pairs. As the generated holes flow to the P+ substrate terminal, the substrate voltage under the source rises until the substrate source diode gets forward biased. At this moment, the

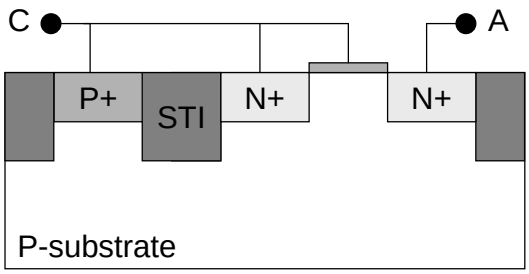

Figure 1.6: Cross-section of a grounded-gate NMOS (ggNMOS).

source will start to emit electrons which are collected at the drain. Avalanche multiplication occurs at the drain side creating a positive feedback mechanism, which allows the drain voltage to collapse (i.e. snapback). As such, a parasitic bipolar npn device is triggered which has an ESD current capability of typically 8-14 mA/μm. For negative ESD stress, the substrate-drain diode gets forward biased, making the ggNMOS a bidirectional ESD protection device. Despite its rather high ESD robustness, the ggNMOS has some important drawbacks. The parasitic snapback effect is difficult to model and simulate. Its behavior is also difficult to predict as it depends heavily on the process parameters. Uniformity problems can occur for large devices. However, even with these drawbacks, the ggNMOS remains a widely used ESD protection device.

Silicon Controlled Rectifier

The cross-section of a Silicon Controlled Rectifier (SCR) is shown in Fig. 1.7. The anode is formed by a P+ region inside an nwell while the cathode is formed by a N+ region inside a pwell. Typically, the nwell and pwell taps are shorted to the anode and cathode respectively. Similar to the ggNMOS device, the ESD operation relies on the triggering of a parasitic element. A pnpn thyristor element turns on when the SCR latches, allowing ESD current dissipation with low on-resistance and low holding voltage. The SCR can reach an ESD current capability comparable to the diodes, up to 50 mA/μm. Special care needs to be taken to reduce the SCR trigger voltage to fit inside the ESD design window as illustrated in Fig. 1.4. Techniques to reduce Vt_1 include the Low Voltage Triggered SCR (LVTSCR) or the Diode Triggered SCR (DTSCR), as will be discussed further in section 2.5.3.1.

Active clamp

ESD current can also be dissipated by a transistor in active MOS mode, simply by making it wide enough as the MOS drive current is proportional to the transistor width. Since the gate needs to be grounded during normal operation conditions to avoid excessive leakage currents, a transient ESD detection circuit is needed which biases the gate during the ESD discharge and keeps it grounded otherwise. Such trigger circuit often involves the use of an RC-timer circuit.

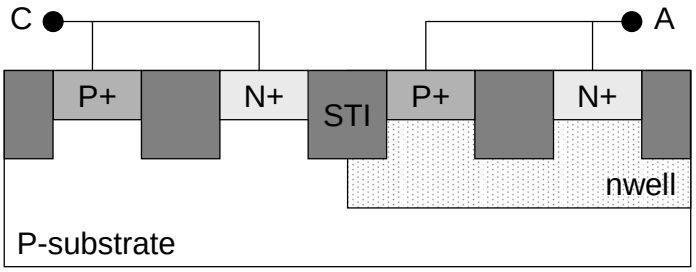

Figure 1.7: Cross-section of a Silicon Controlled Rectifier (SCR).

The active clamp is much larger than a ggNMOS for the same ESD current capability due to the lower ESD robustness of the active mode (∼2 mA/μm) compared to the bipolar mode (∼8-14 mA/μm). However, an active clamp has the benefit that its behavior is easy to predict and simulate and that it can dissipate the ESD current with a very low voltage drop.

1.5 ESD Challenges for Technology Scaling

To ensure that CMOS scaling remains on track according to Moore's law, in the past, different technology options were introduced, such as silicides, lightly doped drains (LDD), Silicon On Insulator (SOI), etc. These technology options had an enormous negative impact on the ESD performance, leading to countermeasures such as ESD specific processing masks, for extra ESD implants and silicide blocking, and also innovative ESD protection concepts, such as ESD protection devices below the buried oxide layer in a SOI technology [Salm 04].

When CMOS scaling reaches the nano-era, another challenge is present for the ESD designer. CMOS scaling involves continuous thinning of the gate oxide, even down to a few nanometers, making the oxide more and more susceptible towards ESD stress. The oxide breakdown voltage BV_{ox} decreases much faster than the trigger voltage Vt_1 and holding voltage V_h of the grounded-gate NMOS device when technology scales down as illustrated in Fig. 1.8. As such, the ESD design window from Fig. 1.4, shrinks with each new technology generation as shown in Fig. 1.9. This means that traditional ESD protection cannot be used anymore as the sum of all voltage drops along the ESD path easily exceeds the breakdown voltage of the gate oxide of the core circuit.

For the 65 nm node and below any overshoot due to slow turn-on of the ESD protection device needs to be carefully monitored, in order not to damage the core circuit. Nowadays, a lot of research is being done towards finding new ESD protection devices, optimizing trigger-speed of the ESD protection

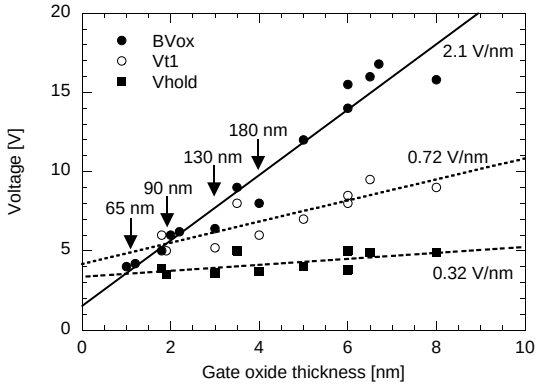

Figure 1.8: Oxide breakdown voltage (BV_{ox}) and trigger (Vt_1) and holding voltage (V_h) of grounded-gate NMOS as a function of CMOS technology scaling [Merg 04].

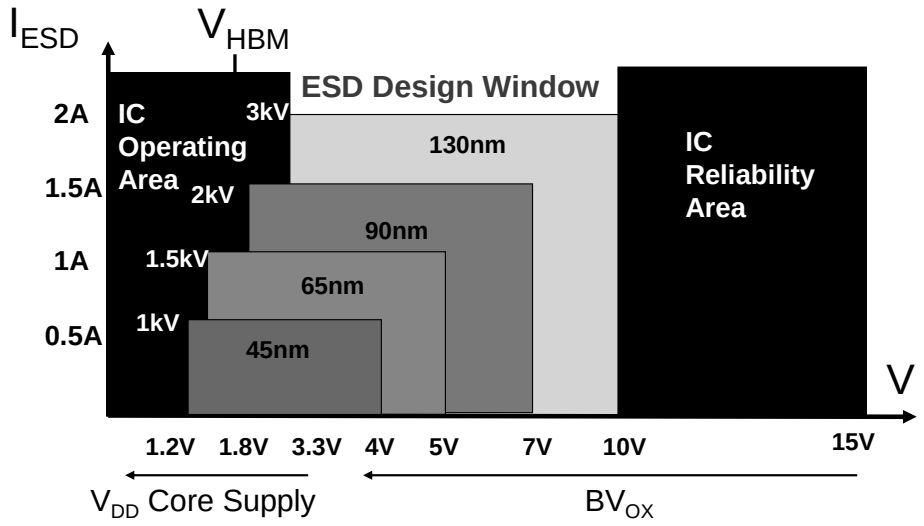

Figure 1.9: Impact of technology scaling on ESD design window [Duvv 08].

device and developing new ESD protection methodologies, such as distributed ESD protection clamps and local clamping without relying on any power clamp (PC) [Bren 05] [Klev 00] [Amer 02]. To further continue CMOS scaling, more and more advanced techniques have to be introduced to cope with the challenges of nanometer-sized devices. Examples of these techniques include the introduction of high-K materials, metal gates, elevated source and drain, ultra-shallow junctions and strain engineering. ESD engineers have to follow this technology development very closely to detect any ESD problems early and to provide suitable solutions for them.

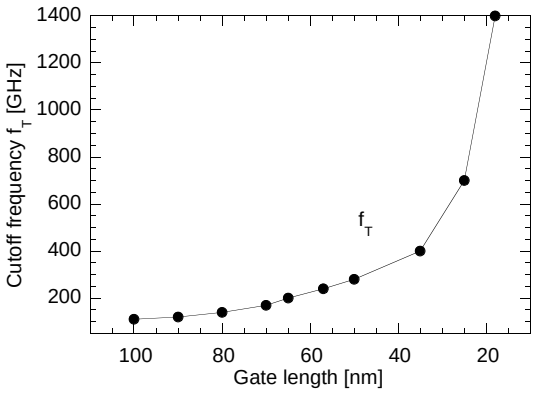

Figure 1.10: Evolution of cut-off frequency f_T with decreasing gate length [ITRS].

According to the International Technology Roadmap for Semiconductors (ITRS) 2007 [ITRS], gate lengths of a transistor will reach the size of 9 nm in 2016. Even if lithography and etching techniques can provide these dimensions, bulk CMOS will run into a number of Short Channel Effects (SCE) associated with transistor scaling. New devices start to arise, out of which multi-gate MOSFET devices show promising performance. In fact, parallel paths are predicted by ITRS to reflect the most likely scenario: some companies will extend planar bulk CMOS as long as possible, others will switch to Fully Depleted SOI and/or multiple gate devices earlier. Eventually, the ultimate MOSFET device will be a multiple gate device and hence its susceptibility towards ESD stress is studied in the first part of the thesis.

1.6 ESD Challenges for Radio Frequency CMOS

Due to increasing cutoff frequencies, f_T, CMOS is rapidly moving up to frequencies that were once the exclusive domain of the III-Vs, see Fig. 1.10. This enables RF circuits to be implemented in low cost CMOS and allows integration of digital and analog functionality within a single CMOS chip. This new range of applications requires ESD protection with is suitable both for the technology and the application.

Fig. 1.11 shows the RF-ESD Figure Of Merit (FOM) as introduced in [PhDLinten] for 2 kV HBM robustness in 90 nm CMOS (black) using traditional dual diode ESD protection. This FOM is defined as the area in the voltage-capacitance plane defined by the oxide breakdown voltage BV_{ox} as upper bound, the gate voltage at the transistor V_{gs} during 2 kV HBM stress using dual diodes as lower bound, the minimal capacitive load C_{min} to achieve 2 kV

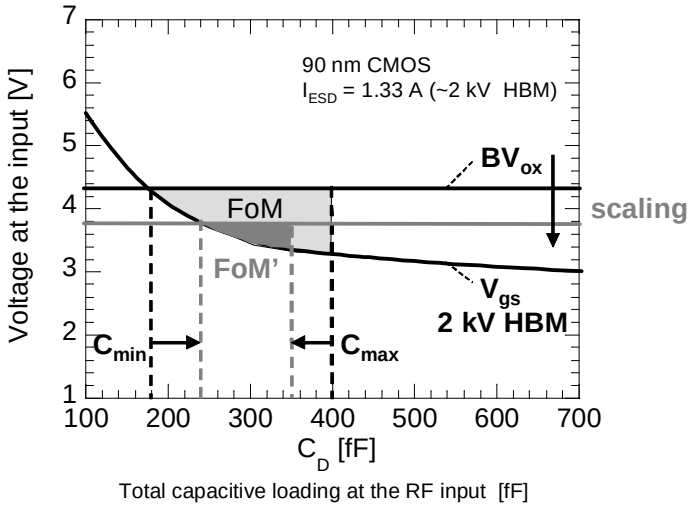

Figure 1.11: ESD design window for 2 kV HBM protection in 90 nm CMOS (black) with dualdiode input ESD protection and diode powerclamp. Scaling (gray) decreases the Figure Of Merit because of reduced oxide breakdown voltage and higher enabled RF operating frequencies.

HBM robustness as left bound and finally the maximum capacitive load C_{max} which can be tolerated by the application as right bound. With scaling of technology the oxide breakdown voltage decreases, which results in a decrease in the FOM because of the increased minimum required capacitance C_{min} (proportional to diode size). Further, technology scaling enables also higher RF operating frequencies, which pushes the maximum tolerable parasitic capacitance C_{max} down, resulting in a second factor decreasing the RF-ESD FOM to FOM'. Therefore, the use of the classical dual diodes ESD protection will become extremely difficult when RF frequency increases.

Two classes of RF circuits exist: narrowband and wideband. In case of narrowband RF circuits, the circuit is operating in a narrow band around a certain RF frequency. The added ESD protection should remain invisible at this frequency only. Contrary, for wideband circuits, the ESD protection should remain invisible for the full RF band of the circuit, which can easily occupy a few GHz. Therefore, different RF-ESD techniques are required for each type and are discussed in the second and third part of the thesis for narrowband and wideband RF circuits respectivley.

1.7 Objectives of the Thesis

This thesis has two main objectives, namely to investigate the ESD robustness of the upcoming FinFET technology and to propose ESD solutions which are compatible with narrow- and wideband RF applications.

Our first main objective is to investigate whether ESD is a potential showstopper for the introduction of FinFET technology. This is achieved by analyzing the ESD capability of basic ESD protection devices implemented in FinFET technology, such as gated diodes and MOS transistors operating in both positive and negative polarities. The 3D-nature of FinFET devices offers an increased set of geometrical parameters compared to planar transistors. Their impact on the ESD robustness needs to be evaluated. Further, as different process options are introduced to improve the overall FinFET performance, also their impact on the ESD performance of the different devices needs to be qualified.

The second main objective is to provide adequate ESD protection for RF applications. RF circuits are being implemented more and more in advanced CMOS technologies and reach ever higher operating frequencies, demanding for new RF-ESD solutions. The objective is to propose new protection methodologies for both narrow- and wideband RF circuits meeting these requirements. The solutions need to be qualified for their RF and ESD impact and need to be benchmarked against traditional and new innovative solutions. A specific emphasis on Charged Device Model (CDM) robustness is also required.

1.8 Outline of the Thesis

A summary of the different chapters of this thesis is provided below.

Chapter 2: ESD Characterization and Analysis Techniques

Commonly used ESD characterization and analysis techniques are summarized in the first part of the chapter. These ESD test methods are extended to give more information regarding transient device behavior under both Transmission Line Pulse (TLP) and Human Body Model (HBM) conditions and extracting of the real holding voltage and current for snapback devices.

Chapter 3: ESD Protection in FinFET Technology

In this chapter, the ESD robustness of the new emerging FinFET technology is evaluated. A fundamental understanding of the physics of the devices under ESD stress conditions is the main part of this chapter. To acquire this understanding, extensive test structures are designed and characterized, while Technology Computer Aided Design (TCAD) computer simulations are used for gaining deeper physical insights. Based on this knowledge, a new ESD

protection methodology is developed.

Chapter 4: ESD Protection for Narrowband RF CMOS Circuits

The implementation of adequate on-chip ESD protection for narrowband RF CMOS applications is addressed in this chapter. This requires addressing both design and technology limiting challenges. As operation frequencies keep on increasing, the simple dual-diode ESD protection is not viable anymore as the parasitic capacitance of the diodes will degrade the impedance matching of the RF circuit. Therefore, other innovative solutions are needed for adequate RF-ESD protection. One of the most promising solutions was found to be inductor-based ESD protection. However, a major concern for RF ESD protection is the Charged Device Model (CDM) type ESD discharge. Inductors are known to cause high voltage overshoots during fast rising pulses. When designing RF circuits in advanced nano-technologies, the challenges are even more severe. Different RF circuits in both planar and FinFET technologies are protected against ESD stress and their RF and ESD performance is evaluated.

Chapter 5: ESD Protection for Wideband RF CMOS Circuits

This chapter addresses ESD protection for wideband RF CMOS circuits. Two innovative RF-ESD alternatives are proposed and both their RF and ESD performance are evaluated and discussed.

Chapter 6: Conclusions, Future Work and Outlook

The main results obtained from this work are summarized and a brief outlook is given towards future research.

Chapter 2

ESD Characterization and Analysis Techniques

Standard ESD qualification tools yield only pass-fail measurements while Transmission Line Pulse (TLP) can additionally be used for quasi-static device analysis. Human Body Model (HBM) testing with voltage and current capturing (HBM-IV) is the best ESD characterization and analysis tool to obtain both quasi-static and transient device information under realistic ESD stress conditions.

2.1 Introduction

ESD testing is divided into two main categories. Component-level ESD testing is used to determine whether components such as integrated circuits (ICs) will be able to survive the manufacturing process in ESD-controlled areas. On the other hand, the purpose of system-level ESD testing is to see whether systems can survive ESD events occuring in the real world. There exists a grey area between component- and system-level ESD testing as Original Equipment Manufacturers (OEM) want to predict system-level ESD robustness based on component-level capability.

Over the years, several component- and system-level ESD stress models have appeared, trying to mimic the different ESD discharge types. The most widely used ESD stress models for component-level ESD qualification are described in section 2.2: Human Body Model (HBM) [HBM 07], Machine Model (MM) [MM 99] and Charged Device Model (CDM) [CDM 99]. In section 2.3, first the general system-level ESD test as standardized by the International Electrotechnical Commission (IEC) [IEC 01] is described. Secondly, the recently proposed model called Human Metal Model (HMM) [Peach 08] is discussed,

which tries to bridge the gap between system-level and component-level ESD.

Based on these models, ESD measurement equipment has been developed to qualify the IC for the different types of ESD stress. During such tests, all pin-to-pin combinations of an IC have to be able to withstand the ESD stress. Since such models only yield pass-fail results, an engineering tool called Transmission Line Pulse (TLP) testing has been developed [Malo 85] where the device response during the ESD discharge could be studied as discussed in section 2.4. Later, specific variants of TLP, such as Very Fast TLP (VFTLP) [Gies 98] and Capacitive Coupled TLP (CCTLP) [Wolf 05] have been designed specifically to investigate the device reponse under CDM ESD stress conditions.

In section 2.5 we will describe how we have enhanced these ESD characterization and analysis techniques to give more information regarding transient device behavior under both TLP and HBM conditions and to allow extraction of the real holding voltage and current for snapback devices.

This thesis focusses only on on-wafer component ESD stress without further discussing system-level ESD stress.

2.2 Component-Level ESD Stress Models

In this section, a detailed description is given of the three most important ESD stress models used today for product qualification: HBM, MM and CDM. These ESD tests only yield pass-fail results by using Direct Current (DC) leakage current measurements after each applied ESD pulse as failure criterium.

2.2.1 Human Body Model (HBM)

The Human Body Model (HBM) describes an ESD discharge event, occuring when a person becomes charged (through motion, walking, etc.) and then discharges by touching an IC with its finger. This discharge is modeled by the equivalent circuit shown in Fig. 2.1, where a 100 pF capacitor C_{HBM} is discharged through a 1.5 $k\Omega$ discharge resistor R_{HBM}. Note that this resistance represents the contact resistance of the finger to the IC, and not the internal resistance of the human body (which is very low, since it consists up to 60 % of water). First, C_{HBM} is charged using a high voltage source by closing switch S_1. The voltage to which it is charged is referred to as the HBM precharge voltage V_{HBM}. Subsequently, switch S_1 is opened and switch S_2 closed, such that C_{HBM} discharges through R_{HBM} into the device under test (DUT). C_1, L_1 and C_B are parasitic elements of the tester which further define the discharge waveform [Verh 93] and are 1.5 pF, 7.5 μH and 40.5 pF respectively for the HBM tester used: model Hanwa HEDW5000M. Note that

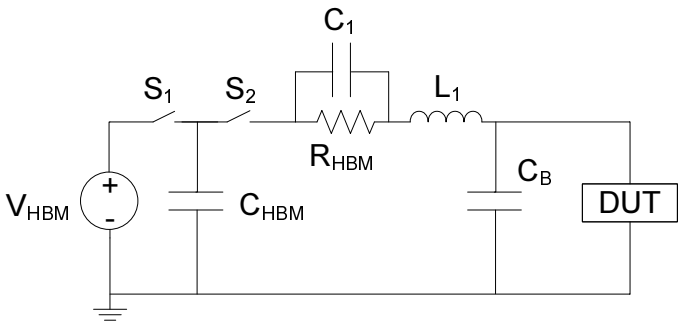

Figure 2.1: Equivalent HBM discharge schematic.

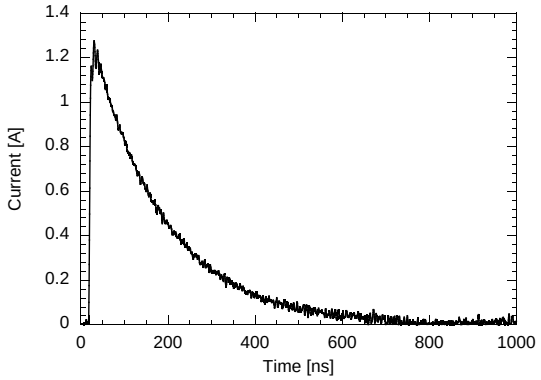

Figure 2.2: Measured HBM discharge current for a HBM precharge voltage of 2000 V.

even though the HBM robustness is defined in terms of its precharge voltage, it is rather a high current event than a high voltage event due to the high discharge resistor. The current pulse shape is standardized according to the ESD Association [ESDA] standard test method (STM) 5.1 [HBM 07], the Joint Electron Device Engineering Council (JEDEC) standard [HBM 07b] or the MIL standard [Mil 96]. It rises within 2 ns to 10 ns and decays during 150 ns. The amplitude of the pulse is defined by the tester pre-charge voltage divided by the 1.5 $k\Omega$ discharge resistance. For a pre-charge voltage of 1000 V the corresponding current peak is about 0.66 A. A 2 kV HBM discharge current pulse is shown in Fig. 2.2.

The HBM robustness of a device is divided into several classes, see Table 2.1. Typically, a HBM robustness level of at least Class 2 (>2 kV) is required, corresponding to a peak current of 1.34 A. However, recently the Industry Council on ESD Target Levels [InCo 07] has launched a proposal to reduce the safe level from 2 kV down to 1 kV [LaPe 07]. The reason is that no obvious correlation of Electrical Overstress (EOS) and ESD field returns to HBM levels

Table 2.1: ESD Component Sensitivity Classification - Human Body Model (Per ESD STM5.1-1998).

Class	**Voltage Range**
Class 0	<250 V
Class 1A	250 V to <500 V
Class 1B	500 V to <1000 V
Class 1C	1000 V to <2000 V
Class 2	2000 V to <4000 V
Class 3A	4000 V to <8000 V
Class 3B	≥8000 V

of 500 V - 2 kV has been observed. Further, the costs for maintaining the 2 kV HBM levels increases exponentially for each new production technology node, see Fig. 2.3 [Duvv 07]. This cost is determined by an increased silicon area for ESD, more silicon respins, increasing engineering resources, decreased circuit performance and larger time-to-market. When reducing the level to 1 kV HBM, the costs are reduced drastically. The Industry Council argues that nowadays basic factory control of ESD can guarantee maximum HBM levels of even lower than 500 V. Therefore, we might expect another decrease of the safe levels in the coming years. JEDEC recently announced the release of JEP 155 [JEDE 08], "Recommended ESD Target Levels for HBM/MM Qualification", as written by the Industry Council.

One important side remark needs to be made as the acceptance of lowering the component-level ESD specifications is still under discussion by the Original Equipment Manufacturers (OEM). They fear that they will run into trouble as they want to predict system-level ESD robustness based on component-level capability.

2.2.2 Machine Model (MM)

The Machine Model is very similar to the Human Body Model, but now the 1.5 $k\Omega$ resistor is removed. An equivalent model consists of a 0.75 μH inductor L_1 and a resistor R_1 between 0 and 10 Ω, which determines the damping of the oscillations, Fig. 2.4. The discharge capacitor C_{MM} is increased to 200 pF. This test originates from Japan and it represents a worst case HBM, when a discharge occurs caused by manufacturing equipment. A typical MM discharge current waveform into a short, originating from a 200 V precharge, is shown in Fig. 2.5. The discharge waveform is specified by the ESDA [MM 99] and JEDEC [MM 97] standards. The higher capacitance and lower series resistance

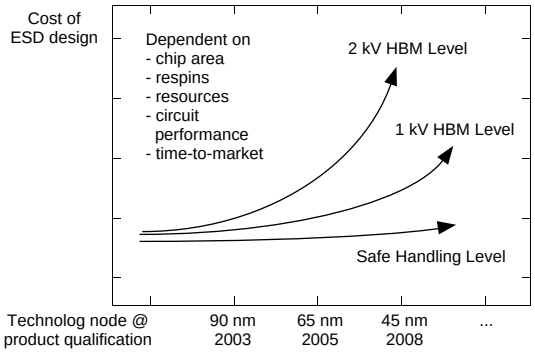

Figure 2.3: The projected cost of ESD requirements as a function of calendar year and the technology node, comparing current customer requirements versus lower recommended target and safe level requirements for handling in an ESD protected area with basic ESD control measures. [Courtesy C. Duvvury]

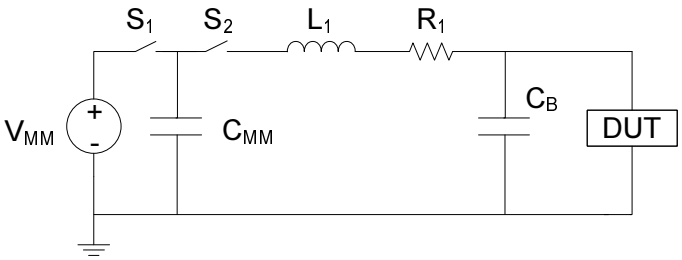

Figure 2.4: Equivalent MM discharge schematic.

results in higher current densities occuring at lower precharge levels. Further, a bipolar current waveform is obtained, Fig. 2.5, originating from the highly oscillating waveform, which is caused by the nearly zero discharge resistance.

Similar as for HBM, the MM robustness of a device is divided into several classes, Table 2.2. Typically, a MM robustness level of at least Class M3 (>200 V) is required. The Industry Council on ESD Target Levels proposes to reduce also the safe MM level to 30 V. This MM level should be guaranteed by passing the new 1 kV HBM specification in both polarities, thereby replacing MM testing. However, in some cases the pulse reversal has a dramatic influence on the ESD behavior of the device, such as during dynamic avalanching [Whit 06]. Additional testing according to MM can always be done as a verification of the expected correlation. Many users still request to continue the MM test since Japanese users have much more MM test results available than HBM or CDM.

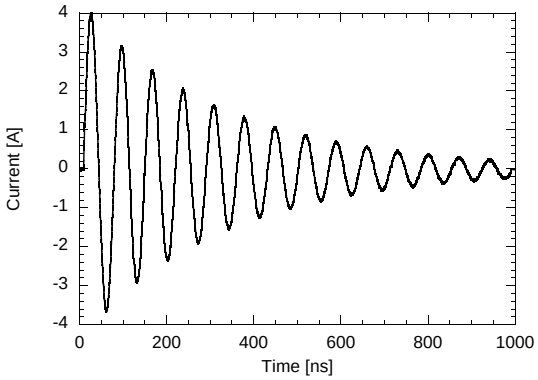

Figure 2.5: Measured MM discharge current for a MM precharge voltage of 200 V.

Table 2.2: ESD Component Sensitivity Classification - Machine Model (Per ESD STM5.2-1999).

Class	**Voltage Range**
Class M1	<100 V
Class M2	100 V to <200 V
Class M3	200 V to <400 V
Class M4	≥400 V

2.2.3 Charged Device Model (CDM)

The most recent ESD stress model is CDM, which causes most of the field-failures. In this stress model, the package gets charged itself, for example by sliding through a plastic tube. When one of the pins of the package touches a conductive surface, all the charges from the package discharge through this single pin. Contrary to HBM and MM, which have discharges occuring between two pins, CDM is a single-pin discharge event. An equivalent electrical schematic reproducing a CDM pulse is shown in Fig. 2.6. Note that now the discharge capacitor C_{CDM} is part of the DUT itself. R_1 and L_1 are 10 Ω and 10 nH for example. R_{CDM} is the total resistance of the discharge path. A typical simulated 250 V CDM discharge current is shown in Fig. 2.7. This peak current heavily depends on the type of package being used as it is proportional to the package capacitance. Different packages will yield different CDM discharge currents. CDM current is characterized by a fast rise time (less than 500 ps), high peak currents and a short pulse duration (a few ns) as defined by the ESDA [CDM 99] or JEDEC [CDM 08] standard. Currently, the Industry Council is reviewing the CDM standard. The different CDM

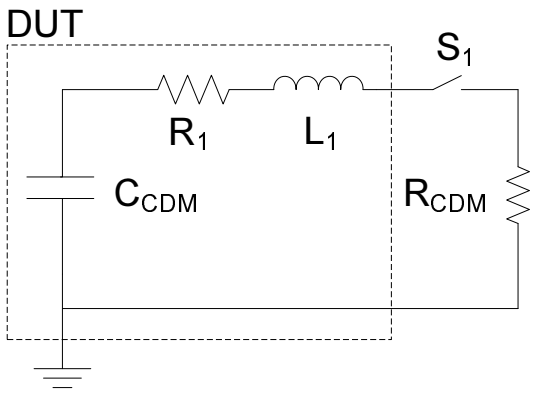

Figure 2.6: Equivalent CDM discharge schematic.

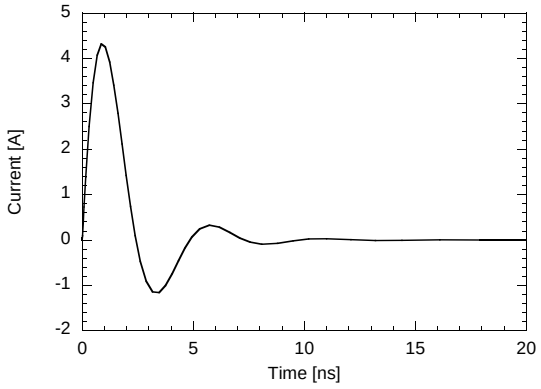

Figure 2.7: Simulated CDM discharge current for a CDM precharge voltage of 250 V.

classification levels are shown in Table 2.3, where a good ESD protection would have at least Class C3 (>250 V). In Fig. 2.8, an overlay is shown between the recommended HBM, MM and CDM discharge currents from Fig. 2.2, Fig. 2.5 and Fig. 2.7 respectively.

2.3 System-Level ESD Stress Models

In this section, a brief description is given of the general system-level ESD test IEC 61000-4-2 and the recently developed HMM, which can be considered as system-level ESD testing on components.

Table 2.3: ESD Component Sensitivity Classification - Charged Device Model (Per ESD STM5.3.1-1999).

Class	**Voltage Range**
Class C1	<125 V
Class C2	125 V to <250 V
Class C3	250 V to <500 V
Class C4	500 V to <1000 V
Class C5	1000 V to <1500 V
Class C6	1500 V to <2000 V
Class C7	≥2000 V

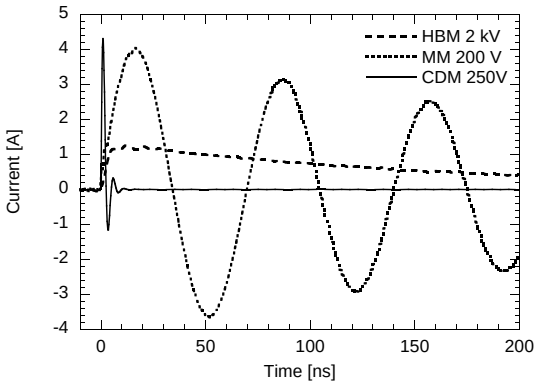

Figure 2.8: Comparison of typical HBM, MM and CDM discharge currents.

2.3.1 IEC 61000-4-2

Electronic equipment may suffer from electromagnetic energies whenever discharges occur from persons to nearby objects. The increased use of microelectronic components requires a clear definition of this problem and to seek a solution in order to enhance system reliability. Therefore, a standard testing procedure is needed to qualify equipment for their immunity against such system-level ESD stress. Typically, an ESD discharge gun, capable of generating such ESD waveforms, is used for system-level ESD testing. The requirements of ESD guns are standardized in [IEC 01], together with the test setup and test procedures. An example of a system-level ESD test being performed is shown in Fig. 2.9, where an ESD gun is discharged directly into a system. Different specifications exist regarding required minimum damage levels but also required minimum disturbance levels when the system is powered up.

Figure 2.9: IEC 61000-4-2 testing being performed. [Courtesy of DLSEMC]

2.3.2 Human Metal Model (HMM)

Since correlation studies [Stad 04] between component-level and system-level ESD stress, using various standard ESD testing methods, yield very little or no correlation, there is a need to try to predict the ESD performance under system-level stress conditions already at component-level. Recently, the ESDA has proposed a new measurement method, called Human Metal Model (HMM), which simulates the case when a person is touching a pin of a grounded electrical component using a metal tool [Peach 08]. This component-level test uses the same stress waveform on the system-level standard IEC 61000-4-2, [IEC 01], which was described in section 2.3.1.

A typical 1 kV HMM discharge current is shown in Fig. 2.10. The current shape is charaterized by an initial fast peak current of 3.75 A/kV amplitude, followed by an HBM-like pulse, which is defined by 2 A/kV at 30 ns and 1 A/kV at 60 ns. Applying such system-level ESD pulse shapes already at component- of even at wafer-level can give valuable insights and ideally become the basis for a deeper study of the correlation between system- and component-level ESD test methods.

The first results indicate a large dependency of the correlation factor between the HBM and HMM precharge voltages, on the type of protection device being considered. This is illustrated in Fig. 2.11, for a 90 nm CMOS diode, a 90 nm CMOS Low Voltage Triggered Silicon Controlled Rectifier (LVTSCR) and a 50 V Bipolar CMOS DMOS (BCD) High Voltage (HV) clamp respectively. Further analysis lies beyond the scope of this thesis. More results can be found in [Scho 08b].

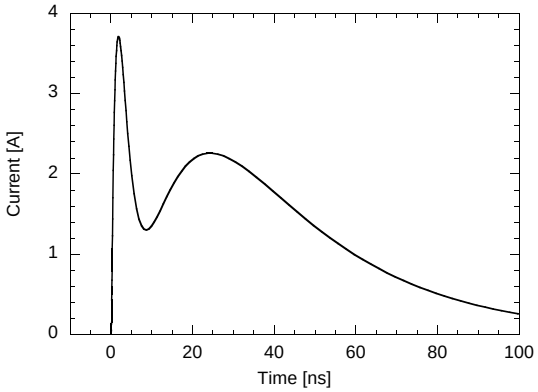

Figure 2.10: Simulated 1 kV HMM discharge current.

2.4 Transmission Line Pulse Measurements (TLP)

Since the previous ESD stress models yield only pass-fail results, an engineering tool called Transmission Line Pulse (TLP) measurements has been developed, which gives information on how the device reacts during component level ESD stress. TLP was first introduced by Intel in 85 [Malo 85]. Until recently, the TLP test method was considered the only non-destructive technique to study the internal ESD behavior in integrated circuits, however we will demonstrate another technique called HBM-IV in section 2.5.3.

If one would try to measure a device with DC up to ESD current levels, which are in the order of Amps, the device would fail early due to self-heating caused by the high instantaneous power dissipation. Therefore, very short rectangular pulses are created, using transmission lines, with a pulse duration in the same order as the ESD-timeframe. This prevents self-heating and allows device qualification in the ESD time-, voltage- and current-domain. TLP is not designed to give accurate measurement results in the low-current region (below a few mA), where DC remains preferred. Recently, the ESD Association published the release of the ESD Associations Transmission Line Pulse (TLP) ESD Standard Practice document, [TLP 02] and a Standard Test Method, [TLP 07].

It should not be forgotten that TLP remains an engineering tool which tries to reproduce the failure mechanism under HBM stress. Such a rectangular pulse is artificial and does not occur under real operating conditions. In fact some people even proposed to replace HBM with TLP as qualification tool to get rid of any HBM-TLP miscorrelation issues... which fortunately did not happen...

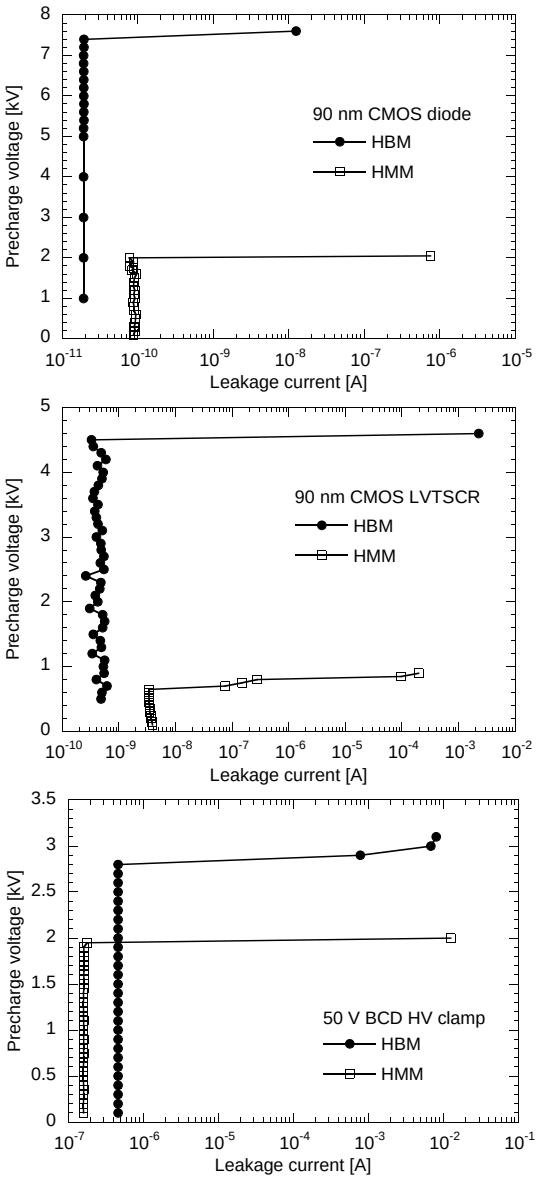

Figure 2.11: Leakage evolution during HBM and HMM testing. A correlation factor of 3.7 is found for a 90 nm CMOS diode (top), 5 for a 90 nm CMOS LVTSCR (middle) and 1.5 for a 50 V BCD HV clamp (bottom) respectively.

2.4.1 Standard 100 ns TLP

Standard TLP has a typical pulse duration of 100 ns and a rise time between 2 and 10 ns. The 100 ns pulse duration was chosen, such that similar TLP and HBM current levels have roughly the same energy content.

A principal schematic of a Time-Domain Reflectometry (TDR) TLP tester is shown in Fig. 2.12. Also TLP systems based on Time-Domain Transmission (TDT) exist [Hyat 00]. In case of TDR, a high voltage source charges up a transmission line of 10 m length, which translates into a pulse width of 100 ns. When switch S_1 closes, the transmission line is discharged. A pulse travels to the DUT via a second shorter transmission line. This pulse is called the incident pulse. When it arrives at the DUT, a reflected pulse is generated based on the impedance of the DUT. The voltage and current of both the incident and reflected pulse are captured, and they are partly overlapping. An example of corresponding voltage and current measurements is shown in Fig. 2.13, for a Diode Triggered Silicon Controlled Rectifier (DTSCR) ESD protection device. This device is further explained in Section 2.5.3. Both voltage and current pulses are captured right after triggering. First, the incident pulse is captured, starting at 20 ns. At around 32 ns, the reflected pulse arrives at the voltage and current probes. Since initially, the SCR device is in an off-state, the reflected voltage pulse has the same polarity and almost same amplitude as the incident pulse. Both voltage pulses are added. When the trigger voltage is reached, at around 35 ns, the device turns on, leading to a voltage snapback and current increase. An average is taken from both the voltage and current waveforms in their quasi-static part, typically between 70 % and 90 % of their pulse width. This quasi-static voltage-current point is then plotted in a TLP-IV graph. The transient information indicating device turn-on, see Fig. 2.13, is ignored. However, we can make use of this valuable information as explained in section 2.5.2.

A full TLP test consists of applying such TLP pulses for increasing voltage levels of the HV source, yielding each time a voltage-current point, which is plotted in the TLP-IV graph. After each stress pulse, a leakage current measurement is performed to see whether any change has occured comparing to the initial leakage current of the DUT before the TLP test, which would indicate device failure. This leakage current is typically plotted versus the TLP current in the same TLP-IV graph on a double X-axis on top. Fig. 2.14 shows such a TLP-IV graph for the Diode Triggered Silicon Controlled Rectifier (DTSCR) ESD protection device. The typical quasi-static TLP parameters for ESD snapback devices, such as the SCR, are also shown in Fig. 2.14: trigger voltage Vt_1, holding voltage V_h, failure voltage Vt_2 and second (thermal) breakdown current It_2. In this thesis, It_2 is defined as the TLP current level at which any change in leakage current is measured, whereas some people prefer

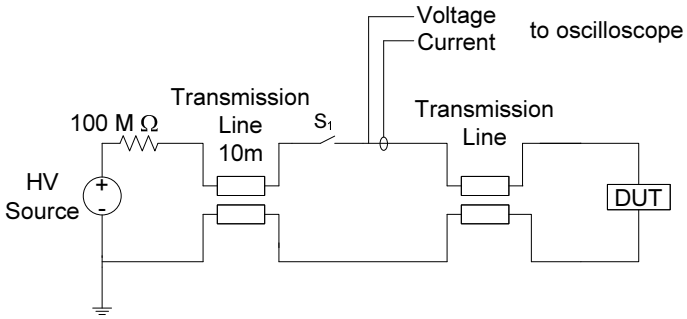

Figure 2.12: Electrical schematic of TDR-TLP measurement setup.

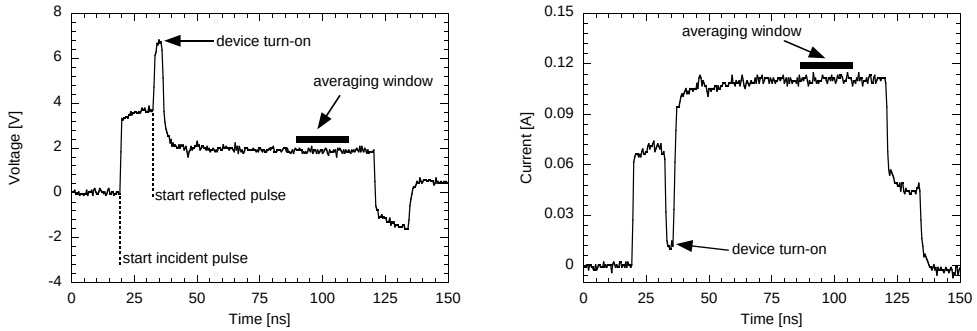

Figure 2.13: Transient voltage (left) and current (right) waveform of a SCR device, right after triggering.

to use a 10 % leakage change or an absolute threshold of e.g. 1 μA. For this example, an unexpected decrease in leakage current is noticed at a current level of 2 A. This decrease could either be caused by SCR or trigger path degradation. Futher investigation would be required to determine whether this leakage decrease is catastrophic. This could be done by performing multiple TLP stress pulses at a current level of about 2.2 A and to check for further leakage changes. However, we define this 2 A current level as the failure level It_2, representing a worst case scenario. Other people might choose It_2 to be 2.3 A, depending on their failure criterium.

2.4.2 Very Fast TLP (VFTLP)

Very Fast TLP (VFTLP) was first introduced by Gieser [Gies 98]. VFTLP has pulse widths of 1-5 ns and a rise time of typically 200 ps. As such, VFTLP has similar characteristics as CDM and hence correlates better to CDM than standard TLP. However, no one-to-one correlation exists, since VFTLP is a unipolar two-pin test and CDM a bipolar single pin event as described in section 2.2.3. Also CDM is package dependent, whereas VFTLP is mainly

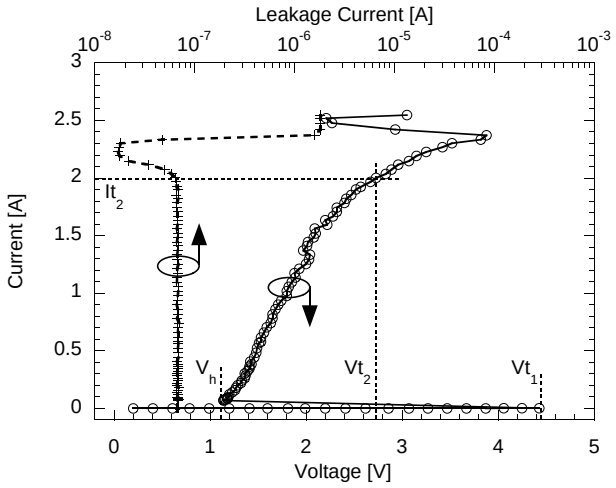

Figure 2.14: Example TLP-IV curve of a DTSCR device.

used on-wafer. Still, VFTLP can be useful for transient device analysis and modelling in the CDM time-domain. A rough correlation exists between VFTLP and CDM according to [CDM 08], which is about 90 V/A for small packages and 45 V/A for large packages based on the CDM peak current values.

VFTLP-testers can be equipped with high-quality RF needles to minimize system parasitics. However, we prefer the use of common probe needles with a very short ground return loop. This method has various advantages. First of all, no expensive RF needles are required (and no high costs are needed when the needles need replacement). Secondly, no specific ESD test-structure layout needs to be designed which is compatible with the fixed RF-probe pitch. Finally, since the current path under CDM conditions is not clearly known and differs from VFTLP, it is important to be able to measure all pin combinations with VFTLP to identify the weakest parts, already at wafer-level. When using VFTLP on circuit level, RF needles cannot be used when trying to stress all different pin-to-pin combinations due to their fixed needle pitch. In chapter 4 and chapter 5, examples are given when VFTLP is applied on circuit level.

Interpretation of VFTLP

A comparison of 100 ns TLP with 1 and 3 ns VFTLP on a DTSCR device is shown in Fig. 2.15. When comparing 100 ns TLP with 3 ns VFTLP, it is clear that almost the same quasi-static parameters, Vt_1, V_h and R_{on} are obtained for this device. Note that the noise level increases for VFTLP, due to two combined elements. First, when decreasing the pulse width from 100 ns down to 3 ns/1 ns, less points are present in the averaging window, increasing the noise. Secondly, for VFTLP the oscilloscope needs to capture fully both the incoming

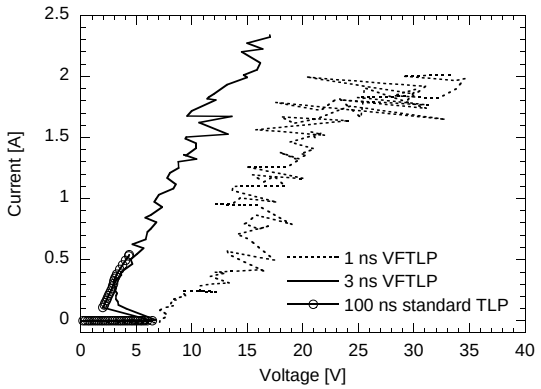

Figure 2.15: Comparison of 100 ns TLP and 1 ns and 3 ns VFTLP IV curves for a DTSCR. The last point shown each time is It_2.

and reflected waveforms, since the overlapping is done only afterwards using software. The limited dynamic range of the Analog-Digital (AD)-converter in the oscilloscope increases the noise in the measurements.

Due to the reduced self-heating because of the smaller pulse width, a 4 times higher It_2 is measured when using VFTLP. However, when comparing this 3 ns VFTLP measurement with 1 ns VFTLP, the explanation is less straightforward. One might wrongly come to the conclusion that when stressing the device with a 1 ns pulse duration, the device would fail earlier than when using a 3 ns pulse width because of the lower It_2 and the higher voltages as seen in Fig. 2.15. One must always keep in mind that a 3 ns pulse will always be worse than a 1 ns pulse due to a higher power dissipation and that in Fig. 2.15 transient IV-curves are compared instead of quasi-static.

To correctly understand this IV graph, Fig. 2.16 shows a zoom of the beginning of the transient 100 ns TLP voltage waveform, using the same rise time of 200 ps as for VFTLP. This transient TLP waveform has been obtained from the same device as in Fig. 2.15, according to the method described in section 2.5.2. For 100 ns TLP, the averaging window needs to be taken in the quasi-static part of the curve, which is between 70 % and 90 % of the pulse. Since the rise time is the same as for VFTLP, a 3 ns VFTLP pulse will initially behave exactly the same as the 100 ns pulse. After a pulse duration of 3 ns, the pulse will vanish. In practice, this is exactly the same as shifting the averaging window from the 100 ns pulse to 70 % - 90 % of the 3 ns pulse width, as indicated in Fig. 2.16. Only a little difference is seen in voltage level, since the device has almost completely turned on at the 3 ns averaging window. Therefore, almost no difference is seen (except for It_2) between the 100 ns TLP and 3 ns VFTLP curves, Fig. 2.15.

However, as clearly seen in Fig. 2.16, the device respons is too slow to turn

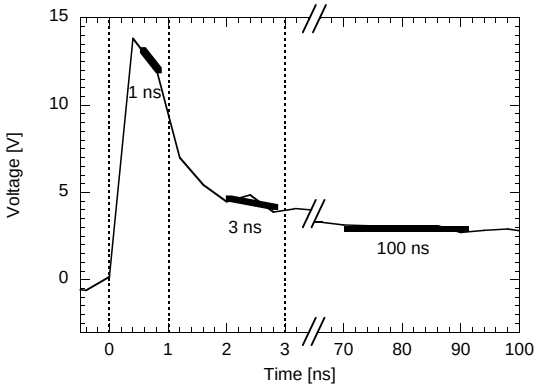

Figure 2.16: Beginning of the transient voltage reponse under a 100 ns TLP stress with 200 ps rise time, similar to VFTLP. The different averaging windows are indicated.

the device on within 1 ns. This results in high voltages and low current levels for the 1 ns VFTLP-IV curve. The absence of snapback in the IV-curve is another indication that this device cannot turn on within 1 ns. The correct interpretation of Fig. 2.15 is that the 1 ns VFTLP differs from the 3 ns VFTLP in a transient way, but not in a quasi-static way. The 1 ns curve is not worse than the 3 ns, moreover, higher It_2 values are even expected for 1 ns pulse width because of reduced heating.

2.4.3 Capacitive Coupled TLP (CCTLP)

Another test method called Capacitive Coupled TLP (CCTLP) was developed in 2003 by the Fraunhofer-Institut [Wolf 05]. Since VFTLP is a two-pin test and CDM a single-pin event, no correlation might exist between VFTLP and CDM. CCTLP uses VFTLP pulses into one pin of an integrated circuit while the current path is closed by means of the capacitance between the device and ground, Fig. 2.17. This method uses specially designed package emulators with a defined background capacitance, which corresponds to the background capacitance of a packaged device which is charged up and discharged during CDM stress. Recently, the authors have shown that their method can yield the same failure signatures as field failures and CDM tests [Wolf 07].

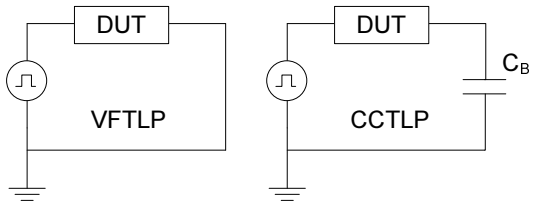

Figure 2.17: Equivalent discharge schematics for the VFTLP and the CCTLP test setup.

2.5 Enhanced ESD Characterization and Analysis Techniques

In this section, we discuss new ESD characterization equipment which has been developed and also present novel analysis based on existing measurement equipment.

In section 2.5.1, a multi-level TLP system is developed based on TLP, to obtain correct measurement results of the device behavior for points underneath the loadline of the test system. In general, only quasi-static device information is obtained from a TLP pulse, where both voltage and current are averaged, typically between 70 % and 90 % of the pulse duration, see section 2.4.1. In section 2.5.2, a method is developed to obtain transient device information from such TLP-pulses as well. Since TLP is an artificial type of ESD stress (no rectangular pulses occur under real nature conditions), another measurement system is proposed to obtain both transient and quasi-static device information under more real-life ESD stress conditions in section 2.5.3, namely HBM-IV.

2.5.1 Multi-level TLP

ESD protection circuits often comprise devices with a non-linear current-voltage characteristic, like snapback devices. The basic technique used to determine the ESD behavior of such non-linear ESD devices requires the use of a rectangular pulse tester, also known as TLP tester, see section 2.4.1. Although each combination of impedance and architecture of the TLP tester will have its own advantages and limitations [Hyat 00], all such TLP systems will determine more or less the same ESD parameters of the device-under-test, except for one - the holding point.

As illustrated in Fig. 2.18, for a given measurement setup, points below the load line (A or B) after snapback cannot be measured. While using a TLP system with high impedance (e.g. 500 Ω, line B) could yield accurate measurement of the holding point, it requires higher charging/driving voltages,

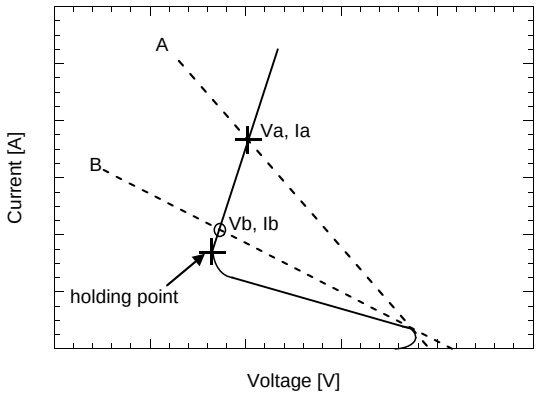

Figure 2.18: TLP IV curve and the influence of system load line.

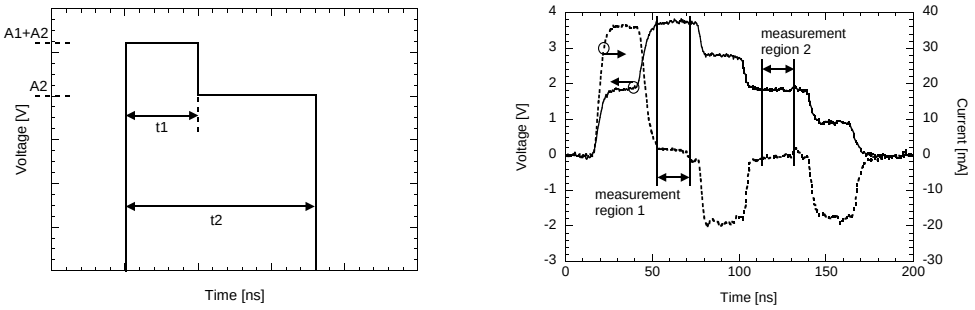

Figure 2.19: Rectangular input pulse sequence proposed under the MTLP test methodology (left) and the resulting voltage and current waveforms on an open load (right).

high voltage cables, higher attenuations and losses in the cables, etc., thereby complicating the measurement procedure and degrading the pulse shapes. For 50 Ω impedance systems (e.g. line A), lower charging voltages can be used but sometimes a large part of the IV curve cannot be measured.

We developed a novel TLP test methodology named as Multilevel TLP (MTLP) test, where multiple TLP systems with different system impedances/load lines are not required for accurate and comprehensive TLP IV measurements. With MTLP, the device-under-test is triggered into snapback using the first part of a multilevel pulse, with amplitude 'A1+A2' during time 't1', see the left graph of Fig. 2.19. While the DUT is being maintained in this conductive state, the amplitude of the pulse is lowered to 'A2' for a time 't2' which then forms the second part of the multilevel pulse. The right graph in Fig. 2.19 shows such a resulting multilevel pulse on an open circuit, with the two measurement regions indicated.

The benefit of MTLP is demonstrated in Fig. 2.20, where an example is given

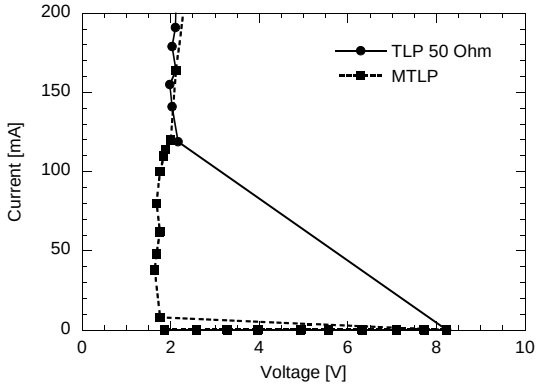

Figure 2.20: A comparison between TLP 50 Ω and MTLP measurements performed on a LVTSCR device.

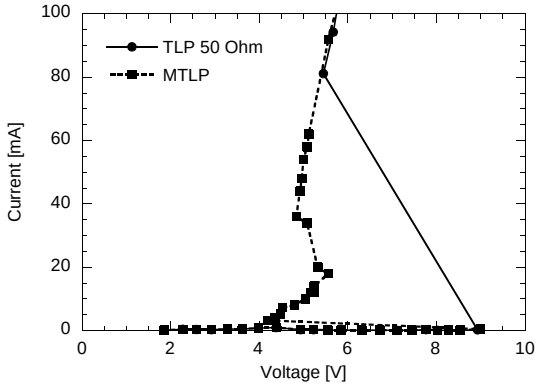

Figure 2.21: A comparison between TLP 50 Ω and MTLP measurements performed on a NPN device.

comparing the 50 Ω TLP measurement results with MTLP on a LVTSCR, processed in a 90 nm CMOS technology. MTLP gives accurate measurement results of the holding voltage and current which is important information to ensure latchup immunity of SCR protection devices. Another example includes detection of a double snapback mechanism in a npn device caused by base push-out which otherwise remained hidden with regular TLP, Fig. 2.21. More details and other examples are described in [Daen 04].

Further, MTLP could be used to induce the same device physics which occur during a system-level discharge event (section 2.3.2) which is characterized by an initial higher pulse followed by a lower pulse.

2.5.2 Transient analysis using TLP

While TLP testing is well known and efforts are ongoing to standardize the test method [TLP 07], extracting the information on the transient device response from the actual TLP pulses is less explored [Gies 98]. The information present in both the TLP voltage and current pulses is significant as it can provide in-depth information on the device transient response. This, in turn, yields direct information whether the ESD protection strategy meets the ESD design window requirements or not.

On the other hand, TLP testers have a certain amount of parasitic inductance from probe needles, ground loops, wiring, etc., which cannot be totally removed. These inductances definitely react to the fast rising pulses of the TLP tester and result in voltage overshoots in the pulse transition period (rising and falling edges). Which part of the observed overshoots in the transient pulse is characteristic for the device and which is due to the system parasitics is neither clear nor known.

A prerequisite for transient waveform analysis is the access to un-clipped voltage and current waveforms. In a typical TLP measurement system, a software algorithm optimizes the vertical scale of the oscilloscope for maximum resolution in the TLP averaging region, as was discussed in section 2.4.1. For example, voltage overshoots can induce positive clipping of the waveform when the device snaps back from a high trigger voltage to a low holding voltage as illustrated in Fig. 2.22 on the top right. For quasi-static standard TLP, accurate determination of the holding voltage is important. However, for waveform analysis, transient information such as voltage overshoots is key, which would be lost due to the waveform clipping. A new software algorithm was used to drive the vertical scale of the oscilloscope, avoiding any waveform clipping. Of course, the price to pay is reduced measurement resolution due to the limited dynamic range of the AD-converter in the oscilloscope, which is demonstrated hereafter by an example. The same device as in Fig. 2.14 has been measured, but now the full voltage and current waveforms have been captured without any clipping, shown in Fig. 2.22 on the bottom right. The derived IV curves are shown at the left side of Fig. 2.22 and are limited to their It_2 value of 2 A. As can be seen, more noise is introduced in the IV-curve when full waveform capturing was used, especially at the higher current levels. When not interested in waveform analysis, but only in the standard quasi-static TLP device analysis, waveform clipping should be allowed to achieve the highest resolution over the averaging region. Further, an algorithm can be developed where first the full waveforms, and subsequently the optimized, clipped waveforms are captured by the scope by applying two consecutive pulses of the same amplitude. After applying both pulses, a single DC measurement can be performed to detect device failure. Note that applying two consecutive stresses could induce some

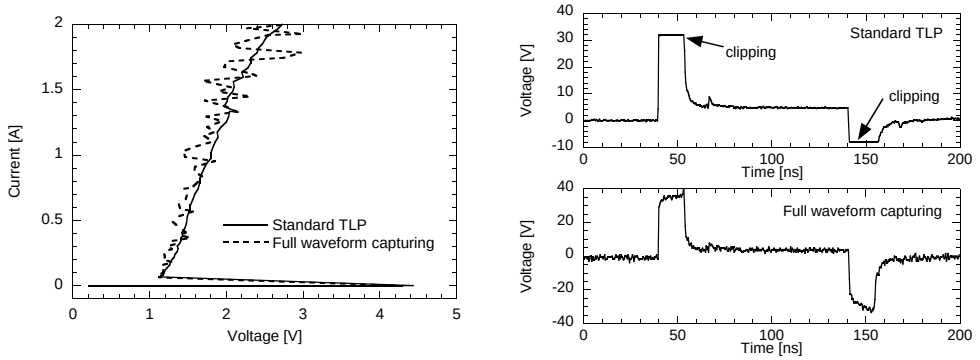

Figure 2.22: Full voltage and current waveform capturing leads to reduced measurement accuracy, especially at higher current levels. The resulting TLP curve is shown on the left, while the right shows the voltage waveforms at a current level of 1.5 A.

cumulative stress, which needs to be investigated for each device type.

Fig. 2.23 shows the electrical equivalent circuit of a TLP tester including its parasitic elements, series resistance R_s and inductance L_s. They model the parasitic contributions from the elements in between the DUT and the measurement oscilloscope (needles, cables, connectors, etc.). The voltage and current are not measured at the device level but at measurement plane A in Fig. 2.23. Therefore, only parts of the incident and reflected waveforms are overlapping, giving the typical TLP waveforms as seen in Fig. 2.24. However, since the measurement system impedance is known to be 50 Ω, the voltage and current can be calculated back to measurement plane B in Fig. 2.23, [Trem 07]. The resulting voltage and current waveforms on a short are shown in Fig. 2.25. The current has a nice rectangular pulse, but the voltage contains an overshoot/undershoot at the rising/falling edge of the current pulse. This effect is clearly not related to the DUT as it is short-circuit load, and therefore must be attributed to a TLP tester artifact.

The desired voltage and current waveforms are at the device level, measurement plane C in Fig. 2.23. For the short circuit load, the voltage across should be zero. Therefore, this data can be used to extract the values of the equivalent network representing the parasitics of the TLP tester as described above. While R_s represent the series losses, L_s represents the inductance contribution, both as seen at the B plane. R_s can be extracted using the standard short TLP calibration procedure, while L_s is extracted from the time dependent voltage, V(t), and current, I(t), equations, as explained below.

During a short-circuit load measurement, the voltage and current pulse at

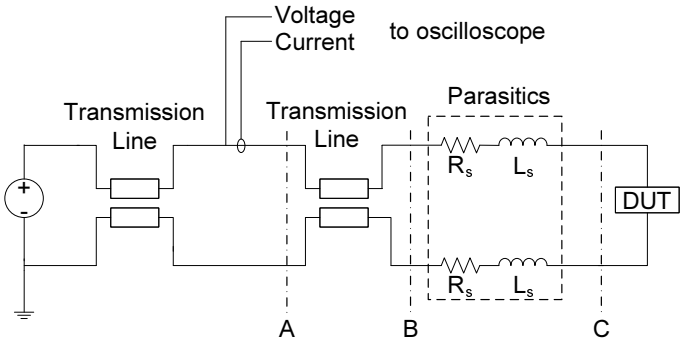

Figure 2.23: Electrical schematic of a realistic TDR TLP tester using a pulse generator and including the system parasitics. The dashed lines indicate the measurement planes A, B and C.

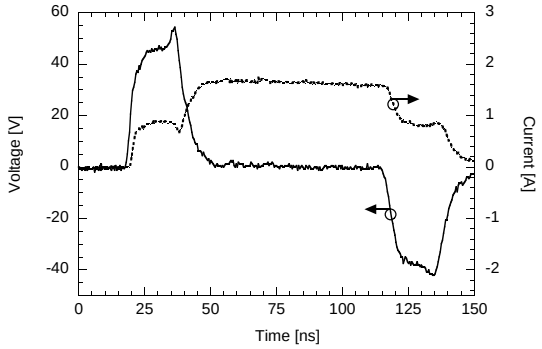

Figure 2.24: Voltage and current pulses measured on a short at reference plane A, marked in Fig. 2.23.

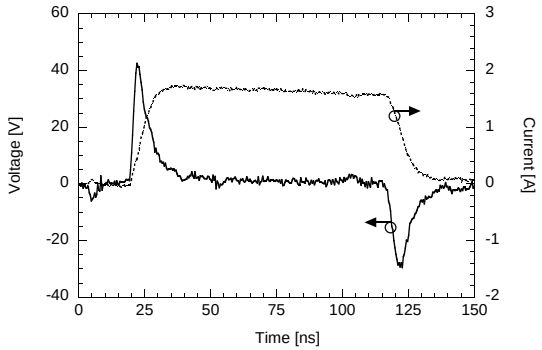

Figure 2.25: Voltage and current pulses measured on a short at reference plane B, marked in Fig. 2.23.

plane B basically follow the simple equation:

$$V(t) = 2R_s I(t) + 2L_s \frac{dI(t)}{dt} \tag{2.1}$$

From this formula, the total series inductance $2 \cdot L_s$ can be calculated. Since the current waveform needs to be differentiated, only meaningful information is obtained during the rising and falling edges of the current pulse. Despite the smoothing algorithm used to compensate the noise generated by the differentiation operation only an average value of the inductance can be deduced.

A proper way to circumvent this problem is by considering the equation in the Laplace domain:

$$\mathcal{L}(V(t), s) = (2R_s + 2sL_s)\mathcal{L}(I(t), s) \tag{2.2}$$

In this form, the transformed V(t) and I(t) signals appear at each side of the equation to fit. As the Laplace transform involves integration, it preserves the smoothening effect intended. Moreover, both fit parameters appear as linear functions of the variables involved. To properly exploit the information content present in the V(t) and I(t) signals, the numerical equivalent of the Laplace transform was implemented by sampling the Laplace transform function,

$$\mathcal{L}(f(t), s) = \int_0^\infty f(t)e^{-st}dt \tag{2.3}$$

with s values equal to the inverse of the measurement timing vector. This extraction method leads to a R_s value of 0.55 Ω and a L_s value of 73 nH, obtained by a least squares fit.

Analysis based on frequency domain measurements on the TLP tester (S-parameter) can also be performed to obtain the parasitic elements, [Trem 07]. The advantage is that more accurate results can be obtained. It takes into account the frequency dependence of the cable losses and gives the timing information between the measurement and the device by modeling the whole system. However, the drawback is the use of a separate network analyser.

After determining the parasitic elements of the system, they can be used to recalculate the 'real' voltage across the DUT, measurement plane C in Fig. 2.23. A similar approach can be followed as for the determination of the parasitic elements, working either in the time, Laplace or frequency domain. Equation (2.4) shows the de-embedding in the time domain. More details

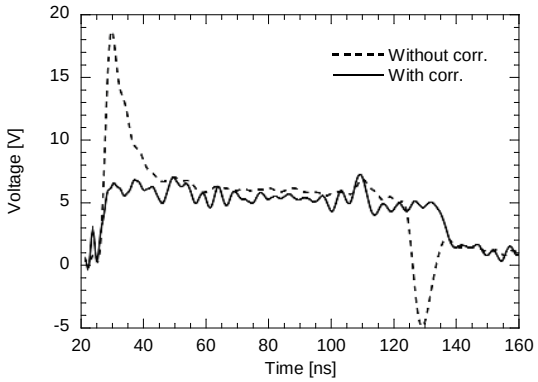

Figure 2.26: Measured and corrected voltage waveform for a 90 nm technology ggnMOS device for a 500 mA TLP current pulse.

are given in [Trem 07] for the parasitic contribution removal procedure in the frequency domain.

$$V_{DUT}(t) = V(t) - 2R_s I(t) - 2L_s \frac{dI(t)}{dt} \tag{2.4}$$

A case study is presented, based on a grounded gate NMOS (ggnMOS) device processed in a 90nm CMOS technology. This device triggers at ∼8 V, and has a holding voltage of ∼5 V as determined by a standard TLP measurement. Applying this method to the aligned voltage waveform, the corrected waveform can be extracted, as shown in Fig. 2.26, where it is overlaid with the uncorrected waveform. It can be seen that prior to implementing the correction, a peak of 18.5 V appears which is due to the system overshoot. This is because, (1) the ggnMOS is known to trigger in less than 200 ps and (2) the TLP tester voltage probe bandwidth is only 500 Mhz. Thus, the TLP tester voltage response is limited by the voltage probe sensitivity (∼2 ns) and therefore the overshoot seen is an artifact. Note that the updated version of the TLP system currently in use, employs a 50 Ω voltage measurement technique and therefore has a 2 GHz bandwidth. Fig. 2.26 shows that after correction of the system parasitics, the voltage across the device is reduced to 5 V. Since the obtained quasi-static trigger voltage was 8 V, this proves that the device is triggered by dV/dt triggering as explained further on.

While analyzing the transient voltage waveforms of the ggnMOS device without any correction, it was observed that the transient voltage overshoot increases with increasing TLP stress current levels. This is shown in Fig. 2.27 as dashed lines (without correction) for the ggnMOS device. After implementing the correction for the tester parasitics described before, however an inverse behavior at the device transient voltage response is observed, as shown in Fig. 2.27

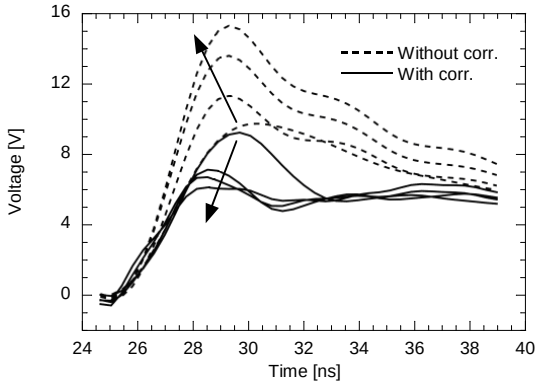

Figure 2.27: Corrected (line) and uncorrected (dash) voltage waveforms for the ggnMOS device at different current levels. Arrows indicate increasing TLP current levels: 100, 200, 300, 400 mA respectively (up, for the un-corrected data and down, for the corrected data).

with a continuous line (with correction). This decreasing maximum voltage is attributed to the transient triggering effect, the so-called dV/dt triggering of the device. As the TLP current increases, the dI/dt value also increases, leading to a lower transient triggering voltage. Thus, the 'real' decreasing maximum voltage across the device after it is turned-on, hidden by the voltage overshoot associated to the needles, is now clearly made visible. Conversely, the increasing over-voltage seen in the uncorrected data does not represent the real behavior of the device and could lead to a wrong interpretation of the device behavior (e.g., transient over-voltage due to this device leading to an unexpected failure at a circuit input).

The example given above illustrates the benefit of transient analysis of TLP waveforms for physical device understanding. But what about the absolute TLP overshoot voltages? Are they real? Since TLP is an engineering tool, one has to investigate how TLP overshoots correlate with overshoots occuring under real-life ESD stress events, such as HBM. A basic intrinsic difference between TLP and HBM is the system impedance. TLP is 50 Ω, whereas HBM is 1500 Ω. This means that in the case of HBM, the current will be forced, almost independently of the device. In the case of TLP, both voltage and current will depend on the device. Section 2.5.3 discusses a method to obtain both quasi-static and transient device information from a HBM pulse. The results clearly show that large differences can occur between TLP and HBM testing, explaining possibly some of the HBM-TLP miscorrelations observed earlier in literature. Transient TLP analysis is useful for device understanding and comparison of different devices, however no absolute values can be obtained, only trends.

2.5.3 HBM-IV

In this section, a new ESD measurement system is developed which uses HBM pulses to obtain both quasi-static and transient device information. The benefit over TLP is that ESD pulses closer to real-life ESD are used instead of artificial rectangular pulses. First the system is described, after which two case-studies are used to demonstrate the benefit of HBM-IV over conventional TLP. HBM-IV is also used further on in this thesis to evaluate the ESD robustness of different devices besides TLP. Similar to HBM-IV, a similar MM-IV can be created. However MM-IV falls beyond the scope of this work.

Conventional HBM testers only yield pass-fail results. The obtained failure level shows how much ESD stress a device is able to withstand. However, no information of the device response under such ESD stress can be obtained and often miscorrelation is observed between TLP and HBM test results. By equiping the HBM test system with a voltage and current probe, the test system transforms into a research tool, rather than being limited to a product qualification tool. With such a setup, the voltage and current during a HBM stress are captured as function of time. For each time point of the obtained waveform data, current is plotted over voltage, thereby forming the HBM IV curve. An example is shown in Fig. 2.28, where a diode is stressed with 1000 V HBM. A HBM IV curve reveals three distinct regions: an overshoot part showing the device turn-on (A), an oscillating part around the peak current (B) and a stable linear part (C) during the falling HBM current. The first two parts show the transient device behavior under ESD stress, whereas the latter represents the quasi-static device behavior. With one HBM pulse it is possible to characterize simultaneously the transient and quasi-static device behavior of a device under HBM stress conditions. In case of TLP, the measurement of an IV curve, which is built-up point by point, can take easily a couple of minutes. On contrary, a single HBM-IV pulse yields the same IV curve within less than a second, and on top yields additional transient information. Of course, some amount of step stressing is still required to determine the HBM failure level.

Each HBM voltage and current measurement is very sensitive to parasitic elements due to its fast, high-current nature. An electrical schematic showing the most important system parasitics of the HBM tester is shown in Fig. 2.29. Voltage and current are measured as close as possible to the needle, measurement plane A in Fig. 2.29. However, these waveforms are distorted due to the needle parasitics, R_s and L_s (measurement plane B in Fig. 2.29). These parasitic elements cause an additional voltage drop around the current peak and the linear region of the HBM IV curve, C in Fig. 2.28, which needs to be calibrated out. Also the current transformers, which are used to measure the discharge current, are usually limited in their bandwidth. Commercially available current transformers, which are suitable for on-wafer HBM measure-

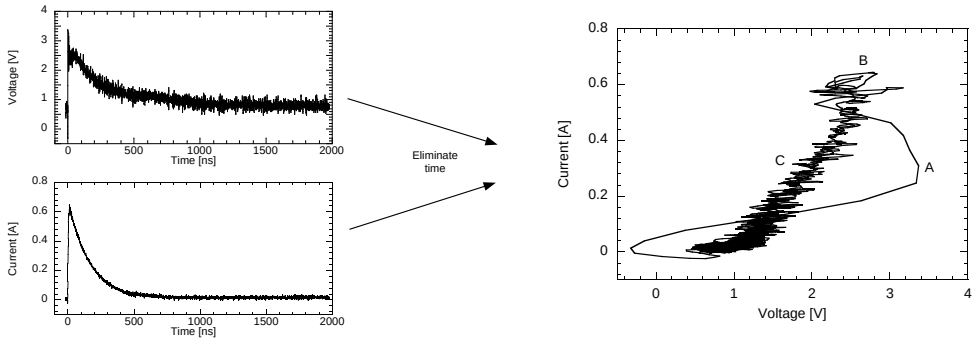

Figure 2.28: HBM IV curve obtained from a diode for a HBM precharge voltage of 1000 V.

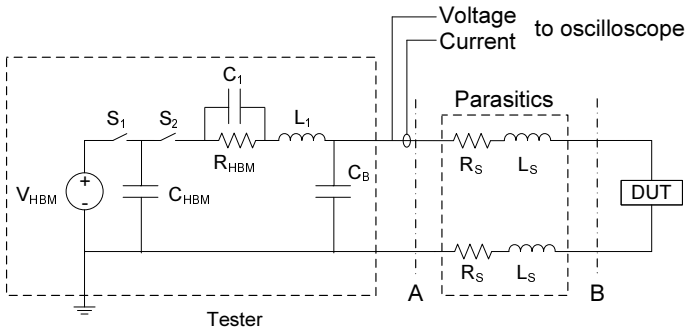

Figure 2.29: Electrical schematic of a HBM tester including the system parasitics. The dashed lines indicate the measurement planes A and B.

ments, have a bandwidth between 25 kHz and 2 GHz. The limitation for lower frequencies distorts the measurement of the falling part of the current waveform and needs to be corrected. Due to the limited power of the signal spectrum at high frequencies of the voltage and current, additional filtering is required in the frequency domain. The full calibration method is described in detail in [Scho 07], [Scho 07b] and [Scho 08].

To study and demonstrate the capability of the described methodology, two case studies are presented. First the turn-on behavior of an advanced sub-micron CMOS ESD protection device is studied. Secondly, the transient behavior of a high voltage CMOS ESD clamp is described.

2.5.3.1 Case study - Diode Triggered Silicon Controlled Rectifier

HBM measurements are performed on Diode Triggered Silicon Controlled Rectifier (DTSCR) devices [Merg 03] [Bren 05]. Four trigger diodes are used, to ensure low leakage during normal operation at bias conditions of 1.8 V,

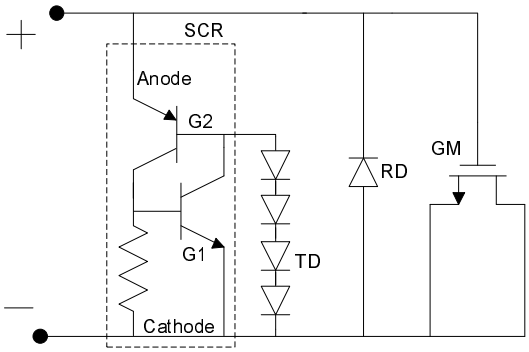

Figure 2.30: Schematic of a Diode Triggered Silicon Controlled Rectifier with four trigger diodes (TD) and one reverse diode (RD) for negative stress polarity. A gate-monitor is attached in parallel to detect failure due to voltage overshoots.

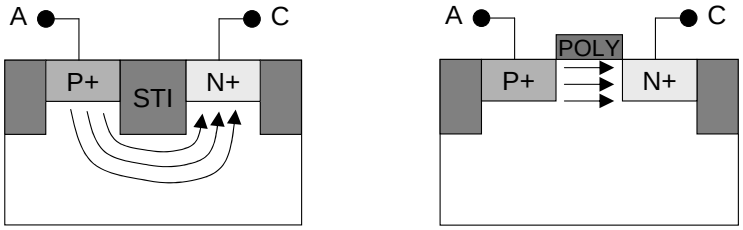

Figure 2.31: Cross-section of STI-defined (left) or poly-defined/gated (right) diode. Arrows indicate the current flow.

Fig. 2.30. The number of diodes also defines the trigger voltage of the protection device. In some cases a gate-monitor is attached in parallel to detect destructive voltage overshoots.

Three different SCR variations A, B and C are used for this study. Type A is the reference device with small trigger diodes and a small Anode-G2 junction inside the SCR. Type B is a speed-optimized version of Type A, found in literature, where both the trigger diodes and the Anode-G2 junction are equally wide as the SCR body to improve the turn-on speed [Merg 03]. We proposed a third version, Type C for which we kept the same sizes as in Type B, but both the Anode-G2 junction and the trigger diodes are changed from shallow-trench-isolation (STI)-defined (left) to poly-defined (right) in Fig. 2.31.

TLP measurements are performed on all three SCR types without gate monitor. The quasi-static TLP parameters are extracted and Table 2.4 shows that all SCR types give comparable results. However, when measuring these three types of SCR devices in a configuration with a gate monitor in parallel using HBM and TLP, the acquired results are varying as seen in Table 2.5. It_2 and V_{HBM} are much lower than expected, indicating a voltage overshoot during

Table 2.4: TLP-IV parameters for the three types of SCR: V_h - holding voltage, Vt_1 - trigger voltage, R_{on} - on-resistance and It_2 - TLP failure level.

	Type A	**Type B**	**Type C**
Device	SCR_ref	SCR_all_STI	SCR_all_poly
$\boldsymbol{V_h}$ **[V]**	1	1	1
$\boldsymbol{Vt_1}$ **[V]**	4.2	3.8	3.8
$\boldsymbol{R_{on}}$ **[Ω]**	1.1	1.1	1.2
$\boldsymbol{It_2}$ **[A]**	1.9	1.9	1.9

Table 2.5: TLP and HBM failure levels for the three types of SCR devices with a gate monitor in parallel.

	Type A	**Type B**	**Type C**
Device	SCR_ref	SCR_all_STI	SCR_all_poly
TLP $\boldsymbol{It_2}$ **[A]**	0.7	1.45	1.9
$\boldsymbol{V_{HBM}}$ **[kV]**	0.5	2.6	4.6

the TLP and HBM pulse that damages the gate oxide of the monitor. These voltage overshoots are limiting the ESD robustness of the device types A and B. For device type C no failure due to oxide breakdown of the gate monitor was observed as the same TLP It_2 level was measured with gate monitor as without. Therefore, it fails due to SCR failure.

To obtain deeper physical device understanding, HBM-IV curves can be investigated. Fig. 2.32 shows the HBM-IV curves of raw, corrected and corrected-filtered measurement data from a 4000 V HBM pulse, applied to device type A without gate monitor. The influence of the system parasitics can be clearly seen. Without correction of measurement data the voltage overshoot is much higher (28 V peak) than the one after correction (7 V peak). Also the linear part of the HBM-IV curve is different. The slope (or on-resistance) is lower after applying the calibration methodology to the measurement data. The filtering removes the noise from the linear part of a HBM-IV curve but also reduces slightly the overshoot voltage. An overlay of a calibrated HBM-IV curve with a calibrated TLP IV curve obtained from the same device shows good correlation, Fig. 2.33. Holding voltage and on-resistance are identical for HBM and TLP.

However, Fig. 2.34 demonstrates that different types of SCR devices show a different transient behavior for the same 500 V HBM pulse amplitude. Device type A is the slowest device and builds up the highest overshoot voltage during

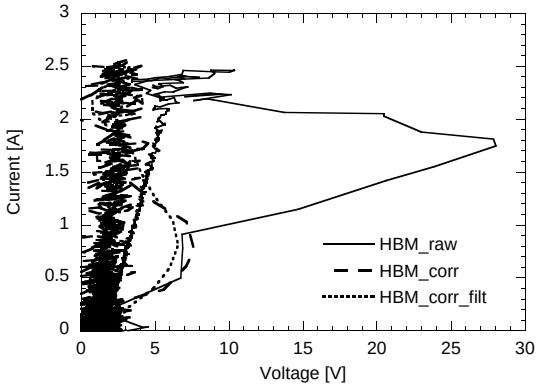

Figure 2.32: HBM-IV curves obtained from a 4000 V HBM pulse applied to device type A: HBM_raw - uncorrected data, HBM_corr - corrected data, HBM_corr_filt - corrected and filtered data.

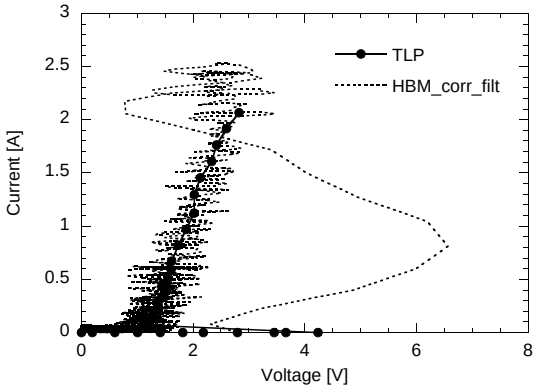

Figure 2.33: Overlay of 4000 V HBM-IV and TLP IV obtained from device type A.

the rising of the HBM pulse. Device type B turns on faster than type A. It builds up less overshoot. The highest improvement is obtained by using poly instead of STI for the trigger diodes and inside of the SCR. Device type C builds up the lowest overshoot, which corresponds to the highest turn-on speed in comparison to type A and B. This leads to an increased HBM robustness when stressing the configuration with gate monitor in parallel, Table 2.5. Due to the improvements type C fails at a HBM stress level of 4.6 kV whereas type B fails at 2.6 kV. Note that the absolute overshoot voltages in Fig. 2.34 are lowered due to the filtering and in reality are above the TLP trigger voltage Vt_1.

Fig. 2.35 shows the transient behavior of an STI diode and a poly diode during the same 500 V HBM stress. The overshoot voltage of the STI diode is higher

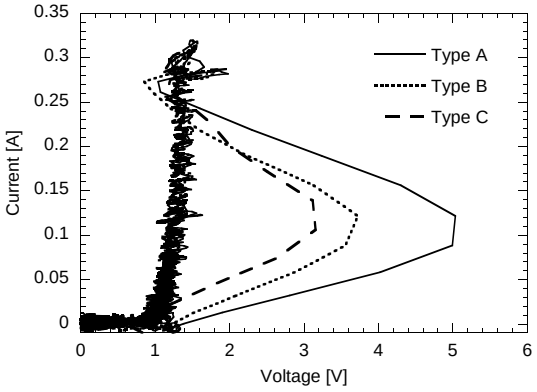

Figure 2.34: HBM-IV curves obtained from different SCR devices for the same HBM stress level: 500 V.

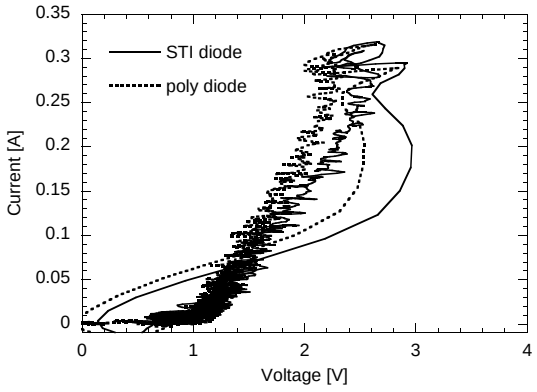

Figure 2.35: Overlay of HBM-IV curves obtained from a poly and a STI diode of the same width and spacing between n+ and p+ active regions, HBM stress level: 500 V.

which is due to a slower device turn-on. Due to their lower distance between anode (A) and cathode (C), Fig. 2.31, poly diodes turn-on faster than STI diodes. In poly diodes the current can flow horizontally and does not have to flow below the STI. Poly diodes can be designed even faster because of the lower allowed spacing between n+ and p+ active in comparison to STI diodes. Additionally the on-resistance of the poly diode is lower.

These results can be used to explain the different TLP failure level It_2 of the device types A, B and C with a gate monitor in parallel. Overshoot voltages occurring during the HBM stress cause the failure of the gate monitor. Therefore in respect to the peak value of the overshoot voltages a clear correlation is found to It_2 obtained during TLP stress in Fig. 2.36. Slow device triggering and the resulting high overshoot voltage are directly corresponding to a low

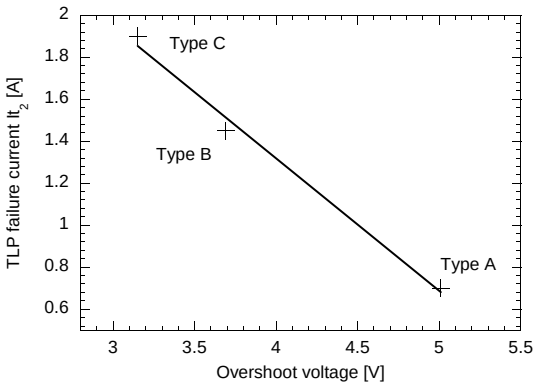

Figure 2.36: Correlation between It_2 obtained from TLP and peak overshoot voltage obtained from 500 V HBM stress for different SCR device types.

TLP failure level It_2.

Our proposed speed optimized version, Type C, was shown to trigger faster than the DTSCR devices available in literature, by employing faster gated diodes. It was shown to efficiently protect the gate monitor up to much higher ESD levels.

2.5.3.2 Case study - HV snapback device

This section uses HBM IV to analyze the turn-on behavior of a high voltage Vertical Diffused MOS SCR (VDMOS-SCR) processed in a 100 V BCD technology. The TLP measurement is shown in Fig. 2.37. The trigger voltage (Vt_1) of the VDMOS-SCR is 115 V and its failure current (It_2) is >7.5 A. The device passes also an on-wafer 8 kV HBM ESD stress test.

The transient turn-on behavior of the device under TLP conditions is evaluated by looking at the calibrated and aligned voltage and current waveforms according to section 2.5.2 during a 2.5 A TLP stress. The voltage increases to a stable voltage of Vt_1, 115 V. After a few nanoseconds at this voltage level, which is the time needed for the HV-device to turn-on [Lint 08], the voltage drops to V_h and current starts to flow. No voltage overshoot is present. The device needs some time to reach this voltage depending on the rise time of the TLP pulse. When stressing the device with a 100 ns TLP pulse with 2 ns rise time, the device needs in total about 13 ns before current starts to flow. When using 200 ps rise time instead, the trigger voltage is reached after 8 ns, however still without any voltage overshoot.

The individual HBM voltage and current waveforms are shown in Fig. 2.39 (left) for a 4000 V HBM stress (equivalent to 2.6 A). When looking closer to

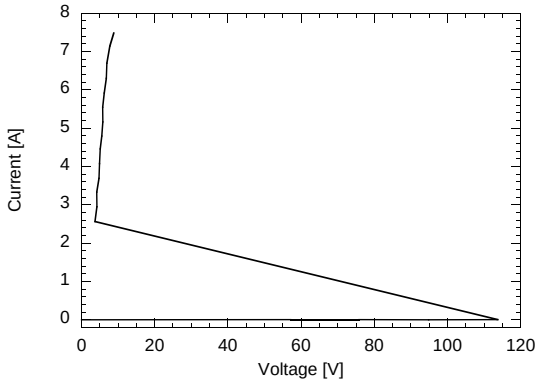

Figure 2.37: Quasi-static TLP IV curve obtained from a VDMOS-SCR device.

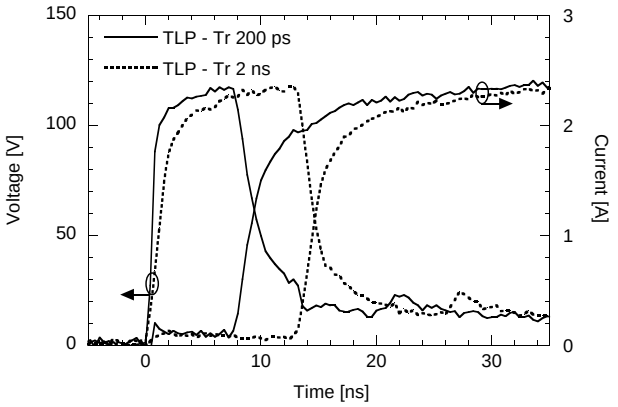

Figure 2.38: Calibrated TLP (200 ps and 2 ns rise time) voltage and current waveforms obtained from a VDMOS-SCR device, stress level: 2.5 A.

the first 10 ns, Fig. 2.39 (right), both a voltage peak (up to 190 V) and a current peak (up to 3 A) are measured. This behavior differs a lot from the TLP result, which had neither voltage nor current overshoot. This could be a cause for TLP-HBM miscorrelation. A HBM-IV curve can be extracted and is shown for both 1000 V and 4000 V in Fig. 2.40. A large voltage overshoot is seen (points A and A') and also a current overshoot (points B and B') over the expected levels (points C and C') according to the HBM precharge voltage. The voltage overshoot is almost 60 % higher than Vt_1 and the current peak for 1000 V precharge is more than double of the expected value of 0.66 A. Note that the fast snapback of the VDMOS-SCR, together with the 500 MHz bandwidth limitation of the voltage probe [Scho 07b], give rise to the negative voltage peak in the voltage waveform.

The shape of the voltage and current waveform is determined by the interaction of the device with the HBM test circuit. Prior to ESD device turn-on, the

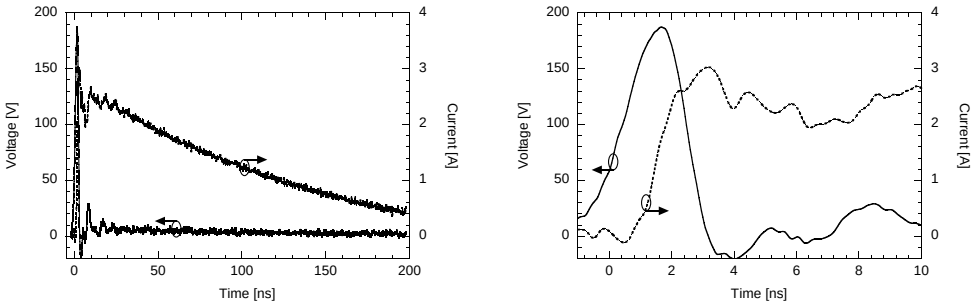

Figure 2.39: Left: Calibrated HBM voltage and current waveforms obtained from a VDMOS SCR device, stress level: 4000 V (equivalent to 2.6 A). Right: Zoom on device turn-on.

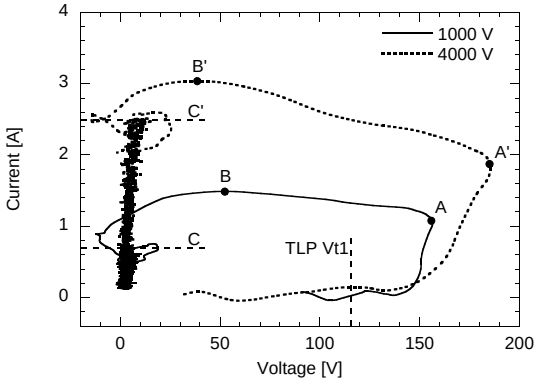

Figure 2.40: HBM-IV curve generated from transient voltage and current waveforms on a VDMOS SCR device, for 1000 V and 4000 V HBM stress levels. Point A indicates voltage overshoot, point B indicates current overshoot and point C indicates the expected current level based on the HBM precharge voltage.

initial charges on the 100 pF HBM capacitor are redistributed over the parasitic tester capacitances consisting of the test board capacitance C_B and the voltage probe capacitance C_{PROB} and over the internal device capacitance C_{DUT}, Fig. 2.41. C_B is in the order of 30 pF, C_{PROB} equals 8 pF, while C_{DUT} can reach several pF's. The dynamics of the charge redistribution depend heavily on the system parasitics.

Since the device needs a certain time in the order of ns untill full conductivity modulation can be achieved [Lint 08], the charge redistribution continues even when Vt_1 is reached. This means that more charges are accumulated on C_B, C_{PROB} and C_{DUT} resulting in a voltage overshoot over Vt_1. Then, when the device turns-on, all these capacitances discharge into the device, without the presence of any series resistor, generating a large CDM-like discharge (i.e. large

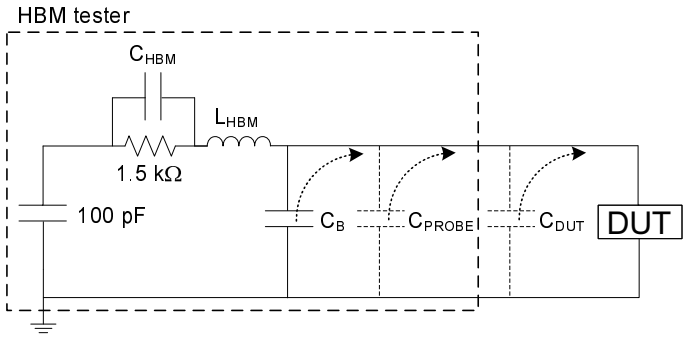

Figure 2.41: HBM test setup. The dashed arrows indicate the additional discharge currents during turn-on. C_B denotes the board capacitance, C_{PROB} the voltage probe capacitance and C_{DUT} the capacitance contribution from the DUT.

current peak). After turn-on, the HBM current source maintains its nominal current for the duration of the pulse.

Both voltage and current overshoots can be reproduced by mixed-mode TCAD simulations [Lint 08]. When the parasitic tester capacitances C_B and C_{PROB} are set to zero, the current overshoot vanishes in the simulation. In practical applications such as large power arrays, the array's capacitance will slow the rise of the incoming HBM pulse. However, the discharge of its correspondingly large stored energy during snapback is an effect that must not be neglected.

Since the tester and DUT capacitances are the cause for the observed overshoots, the impact of the presence of the voltage probe on the voltage and current overshoot needs to be evaluated. As expected, Fig. 2.42 shows that by removing the voltage probe and hence removing C_{PROB}, the current peak is reduced. However the peak remains clearly present due to C_B and C_{DUT}.

To further study the influence of the capacitive loading of the voltage probe on the HBM voltage and current waveform measurements, an additional capacitor with different values is mounted at the needle tips. Values of 6.8 pF and 22 pF are chosen for the capacitors. The capacitors are used with and without connected voltage probe to gain more variations. Together with the input capacitance of the voltage probe (8 pF) 6 variations are available. With the described setup an HBM stress is applied to a VDMOS-SCR device. For every capacitance value the current waveforms have been captured. In case of connected voltage probe, also the voltage waveforms have been captured. From each waveform the maximum amplitude is obtained and plotted versus the used capacitance value. Fig. 2.43 shows maximum voltage and current obtained with a HBM pre-charge level of 4 kV. As expected, the maximum current increases with increasing additional capacitance. However, it is important to notice that

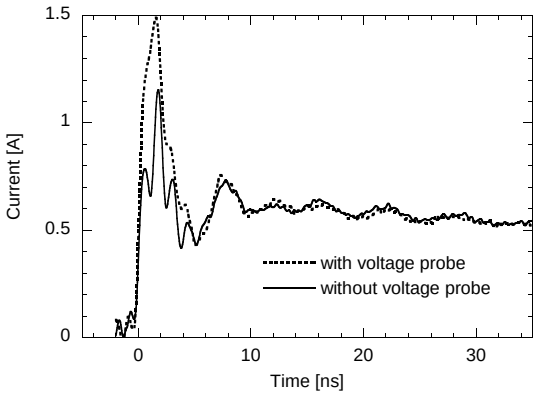

Figure 2.42: Transient current measurements (zoom on first 30 ns) obtained from a VDMOS SCR device during a 1000 V HBM stress with and without voltage probe. The additional capacitance of the voltage probe increases the current peak.

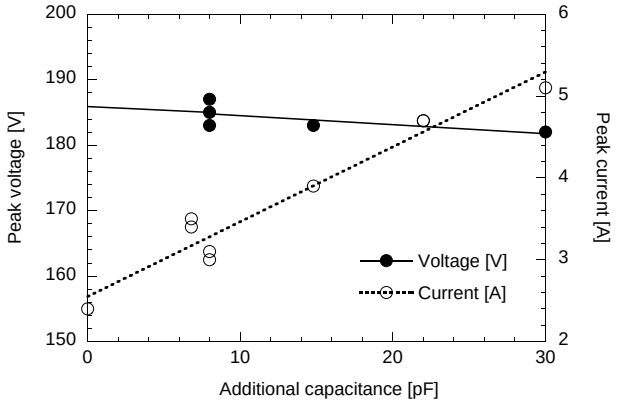

Figure 2.43: Maximum voltage and current during a 4000 V HBM stress level on a VD-MOS SCR device as a function of additional parasitic capacitance (equivalent to 2.6 A).

the maximum voltage stays almost constant and is mainly determined by the DUT. This means that by adding the voltage probe, the voltage overshoot is not influenced.

For accurate voltage and current measurements of such high-impedance devices, the current peak should be measured without the voltage probe, while addition of the voltage probe for the voltage measurement is not interacting with the voltage pulse and can therefore be used without any need for de-embedding.

2.6 Conclusions

In this chapter, first an overview was given of the different standard ESD stress models. TLP and its variants were shown to yield additional device information besides only pass-fail results. Enhanced characterization and analysis techniques were demonstrated based on TLP and HBM. Multi-level TLP was shown to yield device information which was not limited by the system loadline, and therefore allows for accurate holding voltage determination. Transient device analysis was performed on classical TLP measurements by capturing the full voltage and current waveforms. This method introduced techniques to remove the system parasitic contributions revealing the true device behavior. Finally, a very powerful method called HBM-IV was demonstrated, which could yield besides the exact same quasi-static device parameters as obtained from TLP also transient turn-on information, in only a fraction of the measurement time compared to TLP. Two different case studies revealed discrepancies between 'artificial' 50 Ω TLP and 'more real-life' HBM, highlighting the usefulness of this new method.

Chapter 3

ESD Protection in FinFET Technology

Despite a small silicon volume to dissipate the heat from ESD discharges, it is demonstrated that FinFET devices can have reasonably good ESD robustness, depending strongly on layout and process parameters. Different normalization techniques are required for correct data interpretation. A design methodology is needed to determine the optimal device solution for a given set of ESD and functional constraints.

3.1 Introduction

The reliability of sub-micrometer devices and circuits is a major issue that determines both their manufacturability and application lifetime. Design for reliability should be implemented during technology, device and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. As CMOS keeps scaling down, new technology options arise and their ESD robustness should be preferably considered in the early technology development phase as these technology evolutions might lead to a 'drastic' reduction in ESD robustness as it has been the case in the past when new technology features, such as silicides and Lightly Doped Drain (LDD), were introduced [Amer 02].

According to the International Technology Roadmap for Semiconductors (ITRS) 2007 [ITRS], the physical gate length of a transistor will reach the size of 9 nm in 2016. Even if lithography and etching techniques can provide these dimensions, bulk CMOS will run into a number of Short Channel Effects (SCE) associated with transistor scaling, such as Drain-Induced Barrier Lowering (DIBL), punchthrough and velocity saturation. New devices start to arise,

out of which multi-gate MOSFET devices show promising performances. The FinFET transistor is the most widely studied multi-gate architecture for technology-scaling below 32 nm due to its excellent control of SCE and its compatibility with standard CMOS processing [Choi 04].

In [Russ 05] and [Russ 07], it was shown that early FinFET structures displayed an extremely low TLP failure current It_2 for parasitic bipolar action. In the succeeding work [Goss 06], localized heating was demonstrated to be the cause for the high sensitivity and consequently FinFET optimization requires understanding of the thermal effects.

First, the FinFET technology used in this work is described in section 3.2. After discussing the normalization methodology in section 3.3, section 3.4 describes the impact of all FinFET geometrical parameters, such as fin width, gate length, fin spacing, fin height, number of fins and BOX thickness for MOS devices and gated diodes. Their ESD performance is benchmarked against advanced bulk and Partially Depleted SOI (PDSOI) CMOS technologies in Section 3.5. Section 3.6 discusses the impact of different process options, such as extension implants, fin doping, Selective Epitaxial Growth (SEG), Silicide Blocking (SB) and strain. Gated diodes are discussed in more detail in section 3.7, regarding their RF performance, transient behavior and compact modeling. Finally, an ESD protection design methodology which takes into account some of these complex dependencies on layout and processing is described in section 3.8. This allows finding the minimum area solution which fulfills all imposed design constraints.

3.2 FinFET Technology

State-of-the-art FinFET devices developed at IMEC use a high $-\kappa$ gate dielectric and a metal gate. Metal gate is the preferable option over polysilicon gate since it allows obtaining correct N- and P-MOS threshold voltages V_T without using channel doping. The absence of channel doping also permits the drastic reduction of the dopant fluctuation effect. The devices are processed on SOI wafers with 65 nm Si film thickness on top of a 145 nm Buried Oxide (BOX). The gate stack consists of a 100 nm polysilicon on top of a Metal-Organic Chemical Vapour Deposition (MOCVD) metal gate (TiN), a 2 nm high $-\kappa$ HfSiON layer and 1 nm interfacial SiO_2. The TiN gate has its workfunction in the middle of the bandgap such that symmetric V_T's for NMOS and PMOS can be achieved without any fin doping. After Ni-silicidation, a tensile Contact Etch Stop Layer (tCESL) layer of 0.8 GPa is used to introduce strain for improved carrier mobility. All devices used in this chapter have strain unless indicated otherwise and the impact of the absence of strain is studied in section 3.6.5. More technological details can be found in [Coll 05].

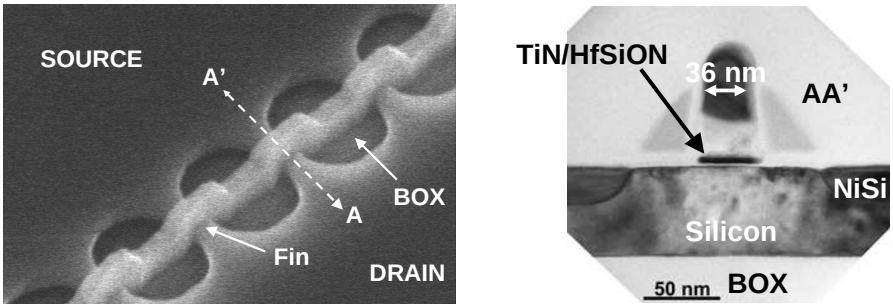

Figure 3.1: Top-down SEM (left) and cross sectional TEM image along cut-line A-A' (right) of a typical FinFET device with a thin MOCVD TiN metal gate on HfSiON dielectric.

A Scanning Electron Microscope (SEM) image and a cross-section Transmission Electron Microscope (TEM) of the fabricated devices are shown in Fig. 3.1. FinFET devices have more geometrical dimensions than conventional planar devices. A 3D layout view of a multi-fin FinFET device is shown in Fig. 3.2. Both a horizontal view and vertical cross-section are shown in Fig. 3.3 with all geometrical parameters indicated. In addition to gate length L_g, the fin width, W_{fin}, is defined by the active etch mask and the height of each fin, H_{fin}, is defined by the Si film thickness. Further we can define the distance between S/D contact area or S/D landing pads and gate L_{SD}, size of the S/D landing pads L_{cont}, spacing between two adjacent fins S, overlap gate on fins W_{ext}, number of fins N and thickness of the BOX T_{BOX}. W_{fin}, W_{ext}, L_g, L_{SD}, L_{cont} and N can be chosen by the designer. H_{fin}, S and T_{BOX} are currently fixed by the process and are 65 nm, 170 nm and 145 nm respectively. L_g is 45 nm minimal, W_{fin} 30 nm minimal, L_{SD} is 100 nm minimal and L_{cont} is chosen to accommodate two rows of contacts for all devices. All contacts have a square shape of 150 nm by 150 nm and are separated by 250 nm. Also devices of a single 'fin' of 40 μm are considered. The reader might argue the use of the word 'fin' for these devices, as they are in essence planar SOI devices.

3.3 Normalization Methodology

For interpretation of the results, different device width normalization techniques are possible for FinFETs due to the larger number of geometrical dimensions compared to planar devices. It should always be indicated which normalization was used.

First, there is normalization possible towards intrinsic silicon width W_{intr} (3.1).

$$W_{intr} = NW_{fin} \tag{3.1}$$

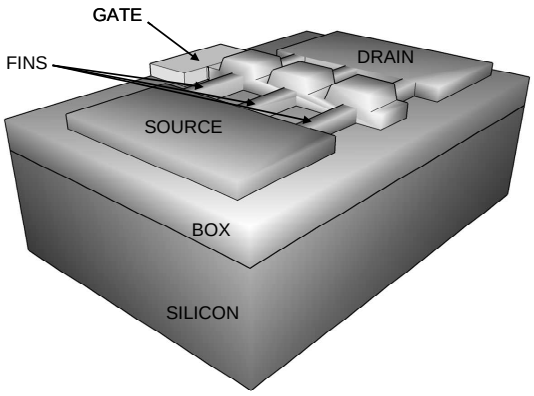

Figure 3.2: Simplified 3D layout view of a FinFET device (not to scale).

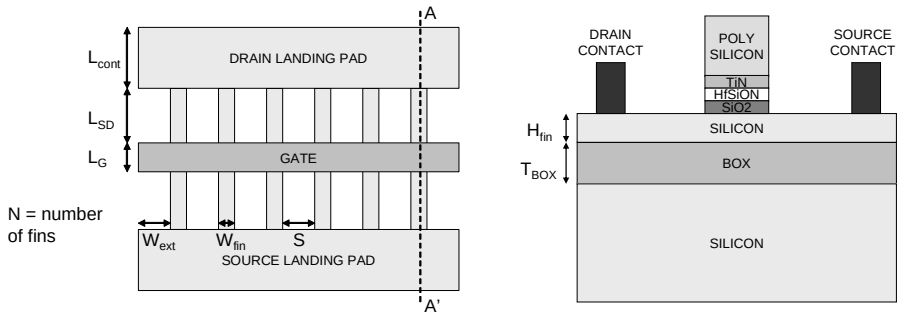

Figure 3.3: Simplified horizontal view (left) and vertical cut along cut-line A-A'(right) of a FinFET device indicating the different geometrical parameters (not to scale).

This normalization is preferred when current is flowing through the full cross-section (W_{fin}*H_{fin}) of the fins, e.g. as will be shown for MOS devices operating in parasitic bipolar mode and for gated diodes. This is a measure for the intrinsic ESD performance of the device, which relates to the current density in the silicon volume.

Secondly, a normalization can be used to investigate the layout efficiency of the device, considering the total layout width W_{layout} (3.2).

$$W_{layout} = NW_{fin} + (N-1)S \tag{3.2}$$

W_{layout} includes the overhead due to the fin-to-fin spacing S. The gate overlap on fins W_{ext} and the size of the poly contacts are neglected. An additional layout optimization could be performed by folding the transistor and sharing different source and drain regions, reducing the overall layout area. The total layout width normalization is most important for an I/O layout engineer since it is related to the total space occupied by the devices on chip.

Thirdly, the normalization can take into account the fact that FinFET devices have a total channel width W_{chan} (3.3), defined by the top and sidewalls of the fin, per silicon footprint area. This normalization relates to the total drive current of a MOS transistor. For a given amount of drive current of an output driver, the ESD robustness of the standalone driver is then known.

$$W_{chan} = N(W_{fin} + 2H_{fin}). \tag{3.3}$$

Finally, a synthetic view of all normalization can be made giving a rough number to compare different technologies. To exploit the FinFET 3D channel benefit, an effective width W_{eff} (3.4) is proposed which corrects the intrinsic width W_{intr} by the ratio of W_{layout} and W_{chan}.

$$W_{eff} = W_{intr}\frac{W_{layout}}{W_{chan}} \tag{3.4}$$

As such, the effective width normalization relates to intrinsic performance, the total drive current and the layout efficiency of the device. This method is more applicable when MOS current is flowing, and therefore is used for MOS devices operating in active MOS mode. For this normalization, the device was considered to behave as a triple-gate transistor. For W_{fin} of 10 nm and below, the contribution of the top channel can be neglected and the device acts like a double-gate transistor. This is also the preferred normalization when comparing FinFET ESD performance with other technologies. Note that for wide fin devices, all three normalizations yield almost identical results.

To avoid the use of three different normalization formulas and to allow easy computation of each normalization, a generic formula (3.5) is derived which is valid in all cases, depending on the values of W_{norm} and S_{norm} as given by (3.6)-(3.11).

$$W_{gen} = \frac{NW_{fin}(W_{fin} + \frac{N-1}{N}S_{norm})}{W_{norm}} \tag{3.5}$$

To normalize for intrinsic performance,

$$W_{norm} = W_{fin} \tag{3.6}$$

$$S_{norm} = 0, \tag{3.7}$$

to normalize for layout efficiency,

$$W_{norm} = W_{fin} \tag{3.8}$$

$$S_{norm} = S, \tag{3.9}$$

to normalize for effective performance according to (3.4),

$$W_{norm} = W_{fin} + 2H_{fin} \tag{3.10}$$

$$S_{norm} = S. \tag{3.11}$$

3.4 Geometrical Dependencies

The influence of the geometrical parameters, L_g, W_{fin}, N, H_{fin}, S and T_{BOX} in Fig. 3.3, on the different ESD performance parameters is investigated in this section. Section 3.4.1 discusses the parasitic bipolar operation mode where ESD stress is applied to the drain, while source and gate are grounded. Section 3.4.2 discusses the reverse polarity, where the device is operating in active MOS mode. Gated diodes are discussed in section 3.4.3.

3.4.1 MOS devices - parasitic bipolar mode

ESD stress is applied to the drain, while source and gate are grounded. The MOS devices are thus first in off-mode and later operated in parasitic bipolar mode, which means that each fin forms its own parasitic bipolar transistor. The analysis done in this section applies to both dedicated MOS ESD protection devices operating in bipolar mode and to MOS output drivers which could be made self-protecting based on these results.

TLP measurements of narrow and wide fin NMOS and PMOS FinFET devices are shown in Fig. 3.4 and Fig. 3.5 respectively for different gate lengths. The last point indicated in each IV-curve corresponds to the maximum failure current It_2. After the next TLP stress level, an increase in leakage current was noticed, indicating device failure. Extraction of It_2, Vt_1, V_h and R_{on} is indicated in Fig. 3.4. The narrow fin devices have a W_{fin} of 30 nm and N is 400, resulting in W_{intr} of 12 μm and W_{layout} of 80 μm, according to section 3.3. The wide fin devices consist of a single 'fin' of 40 μm wide resembling a planar SOI device. Since the parasitic bipolars have their bases floating, no snapback is seen in the TLP I-V curves. This floating body effect is typical for any SOI process [Amer 02], even though for planar SOI a body contact could be provided from the device side. The trigger voltage is not BV_{CBO} as e.g. for bulk technologies, but the device starts to conduct current immediately at the lower BV_{CEO}. This means that the trigger voltage, Vt_1, and holding voltage, V_h, are equal [Amer 02], which helps for uniform turn-on of all fingers. Both

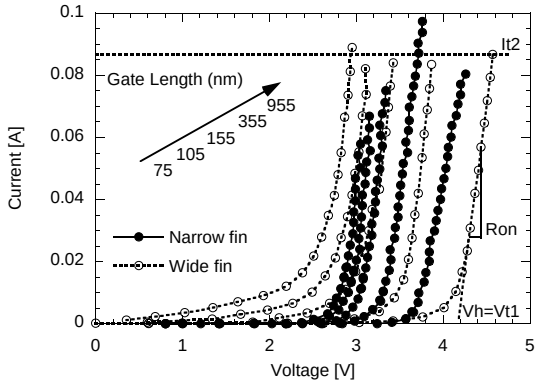

Figure 3.4: TLP-IV curves for different gate lengths of N-type FinFET in bipolar mode for both narrow (400 fins of 30 nm W_{fin}) and wide (single 40 μm) fin devices.

Fig. 3.4 and Fig. 3.5 show that small gate lengths cannot control SCE for wide fin devices, leading to a significant amount of current flow, even at voltages of 2 V and below. More details on leakage current control are discussed in section 3.6.2.

Based on the TLP measurements in Fig. 3.4 and Fig. 3.5, the different ESD performance parameters can be investigated. However, since TLP is an engineering tool, the correlation between TLP and HBM needs to be investigated. Fig. 3.6 shows calibrated HBM-IV curves (see also section 2.5.3) of the same set of narrow fin devices as those of Fig. 3.4. The HBM measurements were done using the method of [Scho 07b] with a 10 V step resolution of the HBM stress levels. A higher failure current is measured during HBM than during TLP. During HBM, this current level represents the peak value which occurs only during a few ns, whereas the maximum TLP current is present during the full 100 ns TLP pulse. With HBM, exactly the same trends can be observed as with TLP and as such, the different ESD performance parameters can be investigated based on TLP. A correlation ratio of roughly 1.5 kV/A is measured between HBM and TLP, which equals the theoretical correlation of the HBM peak current (I_{peak}=V_{HBM}/1.5 kΩ) and the TLP current level.

3.4.1.1 Gate length dependence

The impact of L_g is investigated on the different ESD performance parameters It_2, V_h and R_{on}.

Failure current It_2

It_2 as a function of L_g for both NMOS and PMOS is shown in Fig. 3.7

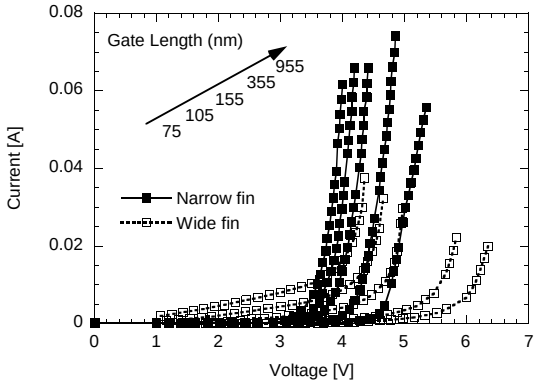

Figure 3.5: TLP-IV curves for different gate lengths of P-type FinFET in bipolar mode for both narrow (400 fins of 30 nm W_{fin}) and wide (single 40 μm) fin devices.

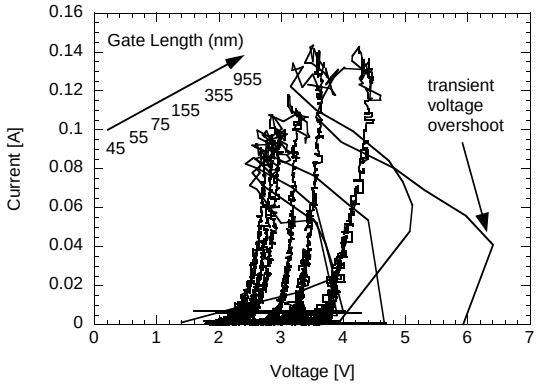

Figure 3.6: HBM-IV curves for different gate lengths of N-type FinFET in bipolar mode for narrow fin devices (400 fins of 30 nm W_{fin}).

and Fig. 3.8 respectively, using the different normalizations as discussed in section 3.3. For narrow fin NMOS and PMOS devices, It_2 increases with increasing gate length and slightly drops down for the largest gate length. At high current levels, the current tends to localize in a few fins near the onset of failure, as described in [Goss 06]. This 'non-uniform failure' is not a matter of 'non-uniform turn-on' in multifinger devices. Remember that the floating base and thus absence of snapback ensures all fingers to turn-on. In [Goss 06], failure analysis was used to show that fusing of single fins was the cause of failure. Increasing L_g for narrow fin devices does not only increase the silicon volume below the gate and hence its heat capacity, but it also seems to have the same effect as a ballast resistance which improves the current uniformity at high current levels. This explains the increase of It_2 with increasing L_g. When further increasing L_g also the voltage drop increases

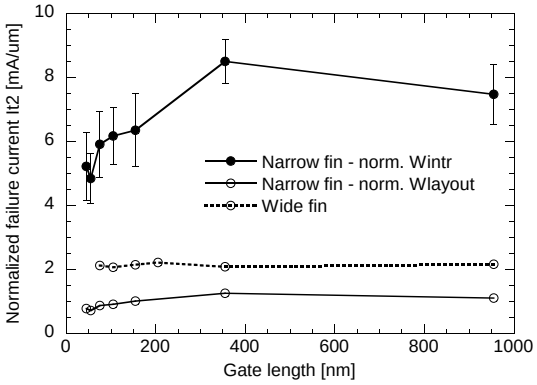

Figure 3.7: Normalized It_2 as a function of gate length for narrow and wide fin N-type FinFET devices in bipolar mode.

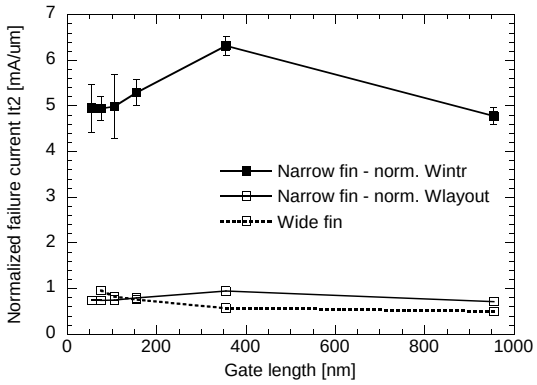

Figure 3.8: Normalized It_2 as a function of gate length for narrow and wide fin P-type FinFET devices in bipolar mode.

(increased V_h and R_{on}, Fig. 3.9 and Fig. 3.11 respectively, explained in the next subsections). As a consequence, the dissipated energy is increased, which leads to a maximum It_2 at medium L_g, Fig. 3.7 and Fig. 3.8. For 45 nm L_g for narrow fin NMOS devices, the very small increase of It_2 compared to 75 nm, is due to incorrect normalization because of a fin-widening due to the Optical Proximity Correction (OPC) of the active etch mask. The shortest L_g leads to shortest fin length and thus the fins are inevitably processed at slightly larger fin width.

For wide fin NMOS devices, It_2 is independent of L_g. For a single fin of 40 μm, much less problems exist with current uniformity at high current levels, since now the current is located within one single wide fin, and not amongst different narrow fins. However, it is important to notice that the failure is located at a constant current level, rather than a constant power level. This

can be attributed to isothermal current instability which is initiated by impact ionization under high field conditions [Vash 08]. Locally a high Joule power level is generated which results in a filament formation and finally local burnout. This means that even within a single wide fin there can still exist a degree of non-uniformity.

In contrast to wide fin NMOS devices, Fig. 3.7, for PMOS devices It_2 is decreasing significantly for the largest L_g, Fig. 3.8. This can be attributed to their high holding voltage (5-6 V) needed for bipolar action as seen in Fig. 3.5 and Fig. 3.9. As such, these devices are failing because of gate-oxide breakdown at the drain-gate overlap region instead of thermal failure of the fins. This is described in more detail in section 3.4.1.3 where several parallel blocks of devices are considered. In case of thermal failure, scaling of the failure level with the number of parallel blocks should be obtained, which is not the case for wide PMOS devices with large L_g.

A possible explanation for the current localization, described in [Goss 06], could be the existence of local Schottky contacts between the S/D silicide (NiSi) and the body of the FinFETs [Hoff 05]. These results were obtained from similar IMEC silicon samples. Such a Schottky contact is a result of over-silicidation of the fins where the Ni-silicide can overrun the lowly doped extension region and grow into the channel region. The ESD robustness is very sensitive to over-silicidation. However, in a more mature technology, the problem of over-silicidation should be greatly reduced. Many arguments point to the negative impact of the over-silicidation. First, the over-silicidation is worst for narrow fin devices [Coll 07], where much more statistical variation is measured than for wide fin devices. Secondly, over-silicidation is less problematic for PMOS devices as Boron retards the silicidation [Coll 07] [Dixi 06]. This can explain the increased It_2 for PMOS devices with smallest gate length when compared to NMOS and the reduced L_g dependency, Fig. 3.7 and Fig. 3.8. Also, much less statistical variation in It_2 was measured on PMOS than on NMOS devices. The error bars indicating the standard deviation of It_2 for NMOS and PMOS devices in Fig. 3.7 and Fig. 3.8 for W_{intr} normalization show the increased variability for NMOS. Finally, over-silicidation is reduced by processing options like silicide blocking and SEG, which directly translates into an increased ESD performance as described further in section 3.6.

For wide fin NMOS devices, It_2 is equal to 2 mA/μm and independent of L_g, Fig. 3.7. The ESD robustness for narrow fin NMOS devices is 0.5 to 1 mA/μm when normalized to W_{layout}. However, the robustness regarding W_{intr} is 5 to 8 mA/μm, representing an even higher intrinsic It_2 than the results reported for planar SOI devices [Kepp 06]. This is explained by looking at the fin width dependence of It_2 in section 3.4.1.2.

Holding voltage $V_{\mathbf{h}}$

The condition for the onset of parasitic bipolar action (at low current levels) [Amer 02] is

$$\beta(M-1) \geq 1, \tag{3.12}$$

where β is the common-emitter bipolar current gain and M the multiplication factor. M depends on the breakdown voltage V_{bd} according to [Mill 57]:

$$M = \frac{1}{1-(\frac{V_j}{V_{bd}})^n}, \tag{3.13}$$

with V_j the junction voltage and n a fitting parameter ranging from 2 to 6 depending on the type of junction. As can be seen, the holding voltage V_h (V_j where (3.12) is fulfilled) depends on both β and V_{bd}. V_h is extracted according to Fig. 3.4, and increases with increasing L_g (Fig. 3.9) because the base width of the parasitic bipolar is increased which decreases β. Therefore, higher M is needed to satisfy condition (3.12) and thus higher voltages are obtained. V_h saturates with increasing L_g since M increases exponentially with junction voltage. V_h of PMOS is higher when compared to NMOS due to the reduced hole versus electron mobility and the lower avalanche multiplication factor of the hole- versus electron-current [PhDTrémouilles].

We have verified that the breakdown characteristic is independent of L_g in the range of electric fields which correspond to the holding voltages measured in Fig. 3.9. These results were obtained by performing breakdown measurements on gated diodes (P+/Intrinsic/N+) with floating gate, 1 μm W_{fin} and different L_g, see Fig. 3.10. This same result was also measured for narrow fin devices of 20 nm with varying L_g.

As such, V_h can be tuned for narrow fin devices between 2.6 and 3.6 V for NFETs and between 3.5 and 4.6 V for PFETs. The holding voltage is clearly determined as almost no statistical variation was measured.

On-resistance $R_{\mathbf{on}}$

The high current on-resistance R_{on}, normalized to W_{intr} is shown in Fig. 3.11 as a function of L_g. For narrow fin NMOS devices, the on-resistance is relatively independent of L_g for small gate lengths, giving a measure for the access resistance of the device, which is determined by the resistance of the source/drain landing pads, the interconnects and amorphization of the silicon [Coll 07]. Due to OPC fin widening for narrow fins with smallest L_g a lower resistance is expected, however this impact is masked by the access resistance. When further increasing L_g, the additional bipolar transistor voltage drop in the base region becomes visible. Very little statistical variation was measured. Wide fin devices exhibit the same gate length dependency but

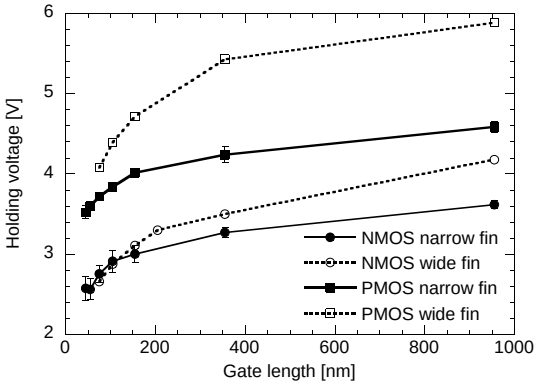

Figure 3.9: Holding voltage as a function of gate length for narrow and wide fin FinFET devices in bipolar mode.

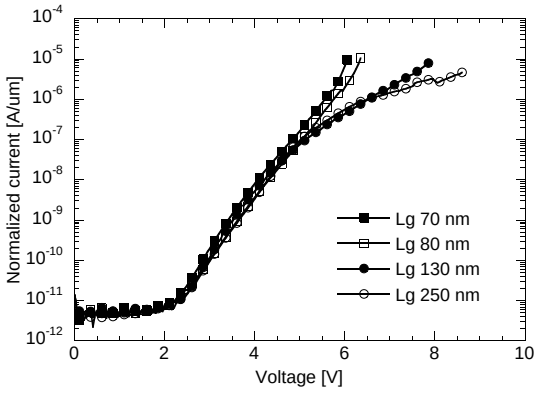

Figure 3.10: Measured breakdown characteristics normalized to W_{intr} for gated diodes with floating gate, W_{fin} 1000 nm and N 64 fins and varying L_g.

at a much higher R_{on}. This width dependence of R_{on} is further discussed in section 3.4.1.2. The resistance of the PMOS increases with increasing L_g and is larger than for the NMOS, which is partly due to the lower hole mobility. In [Dixi 06], the difference in silicide formation between NMOS and PMOS devices was studied. It was found that for NMOS devices, the sidewalls were completely silicided along the whole height of the S/D region, which was not the case for the PMOS, again due to the presence of Boron in the S/D regions. This effect futher explains the increased on-resistance for the PMOS devices.

3.4.1.2 Fin width dependence

The impact of W_{fin} is investigated on the different ESD performance parameters It_2, V_h and R_{on}.

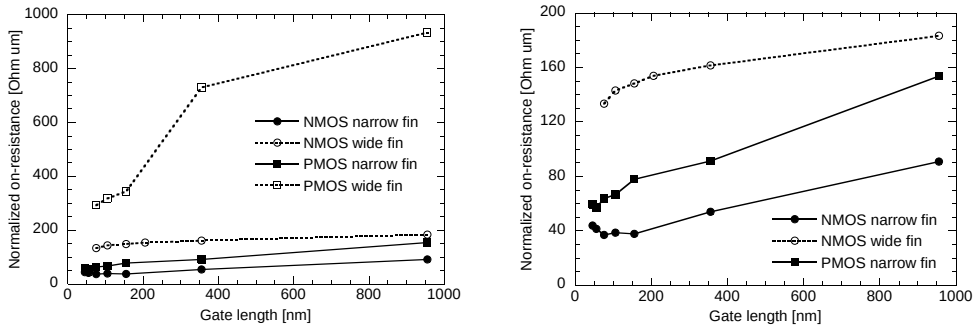

Figure 3.11: High current on-resistance normalized to intrisinc silicon width as a function of gate length for narrow and wide fin FinFET devices in bipolar mode (left: full scale, right: zoom).

Failure current It_2

In Fig. 3.12, the normalized It_2 as a function of W_{fin} is shown for NMOS and PMOS devices with a gate length of 75 nm. The largest statistical variations were measured for the narrowest fins and in general for NMOS. This again can be attributed to their higher sensitivity to over-silicidation, which has a direct negative impact on It_2. When normalizing It_2 versus W_{intr} and versus W_{layout}, different trends are observed. An increased intrinsic performance is measured for decreased fin width. This increase in It_2 can be attributed to the higher effective heat capacity of the 3D-gate, which fully surrounds the fin. Narrow fins act as regular 'cooling fins'. For wider fins, this 3D-nature of the gate disappears and the device becomes very similar to a planar device, leading to a decrease in It_2. The same dependency and relative difference in It_2 versus fin width between NMOS and PMOS is observed. However, when normalizing to W_{layout}, the trend becomes opposite. This is because for smaller fins, there is relatively more area overhead due to the fin-to-fin spacing, making them less area efficient. For wider fins, the difference between the two normalization techniques obviously disappears because of the reduced fin-to-fin spacing overhead. From Fig. 3.12 and all subsequent figures which include fin width dependency, it can be concluded that from a 1 μm wide fin onwards (for the given fin height and fin spacing), the devices can be treated as 2D planar SOI instead of 3D FinFET devices.

TCAD analysis

In this subsection, TCAD analysis has been carried out to investigate the impact of future scaling of fin width on It_2. The simplified horizontal 2D cross-section in Fig. 3.13 (top) has been used for 2D TCAD simulations for W_{fin} of 30 nm, 75 nm, 175 nm and 1 μm. These simulations are preferred over actual 3D simulations because of reduced complexity and simulation time. The NMOS devices operate in bipolar mode and have 75 nm L_g and 170 nm

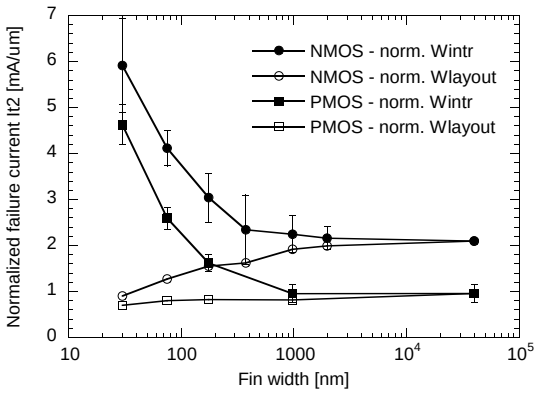

Figure 3.12: Normalized It_2 as a function of fin width for FinFET devices with 75 nm gate length in bipolar mode. Devices up to 175 nm fin width consist of 400 fins, up to 2 μm of 40 fins and the 40 μm wide device has only a single 'fin'.

fin spacing, corresponding to the dimensions of the measured devices. The simulations represent a single fin in the center of a multi-fin device. Indeed, due to the reflective boundary conditions the structure is virtually surrounded by identical structures. In case of a 40 μm fin 'planar' device, a vertical 2D cross-section as in Fig. 3.13 (bottom) could be considered. However, such a vertical cross-section requires the presence of the BOX to avoid a (virtual) second gate at the bottom and hence ensure correct boundary conditions. This would prevent a direct comparison to the horizontal simulations, where no vertical temperature gradient is possible. Therefore, only horizontal devices are used in simulation, the 1 μm fin width being representative of a wide planar device. The simplification of removing the vertical temperature gradient leads to an overestimation of the temperature, and hence only trends can be obtained.

A 15 mA 100 ns TLP pulse (which is 20 % of It_2 for 400 fins of 30 nm W_{fin}) was simulated for a NMOS device in grounded-gate configuration and the maximum temperature was recorded. Device size normalization was performed towards W_{intr}, leading to identical current densities (1.25 mA/μm) for the devices with different W_{fin} dimensions. The maximum temperature for a reference device consisting of 400 fins of each 30 nm width during such TLP pulse is shown in Fig. 3.14. At the end of the TLP pulse, the maximum temperature is 420 K, which is reached at the junction between drain and fin body. Since these devices will be shown to fail non-uniformly due to isothermal current instability at high current levels in section 3.6.5, constant current density simulations are used instead of constant power. When simulating the same current density through devices with different W_{fin}, the maximum temperature is observed to increase with increasing W_{fin} in Fig. 3.15, which is

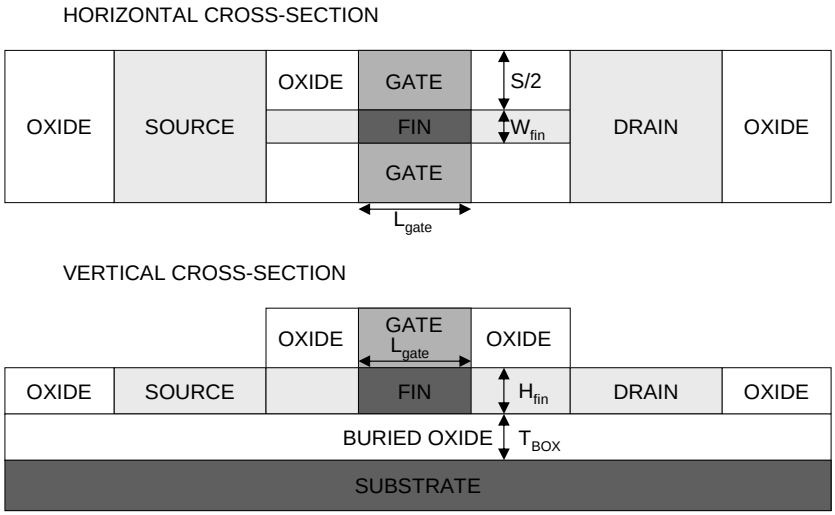

Figure 3.13: Simplified 2D TCAD horizontal (top) and vertical (bottom) cross-section of a FinFET device.

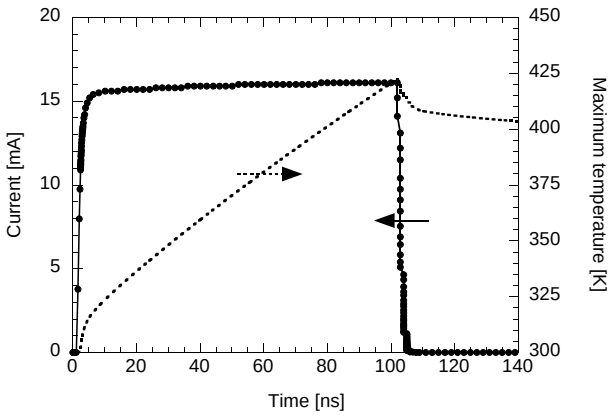

Figure 3.14: TCAD simulation of maximum temperature as function of time during a 15 mA (1.25 mA/μm) TLP current pulse for W_{fin} of 30 nm. The NMOS device in bipolar mode has 75 nm L_g.

explained by the effect of fin cooling. This results in a decreased It_2 which is confirmed by the measurements in Fig. 3.16.

Moreover, when taking the ratio of measured It_2 for each W_{fin} variation relative to 30 nm, and applying a lower TLP current pulse to the device corresponding to this ratio (0.83 mA/μm pulse for 75 nm, 0.62 mA/μm for 175 nm and 0.42 mA/μm for 1 μm), TCAD simulations show in Fig. 3.17 that all devices yield almost the same temperature behavior, within 40 K variation. This means that indeed the It_2 dependence on W_{fin} can be fully described by

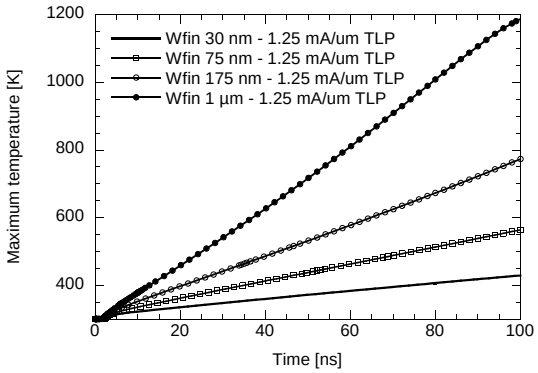

Figure 3.15: TCAD simulation of maximum temperature as function of time during a 1.25 mA/μm TLP current pulse for different W_{fin}: 30 nm, 75 nm, 175 nm and 1 μm. All NMOS devices work in bipolar mode and have 75 nm L_g.

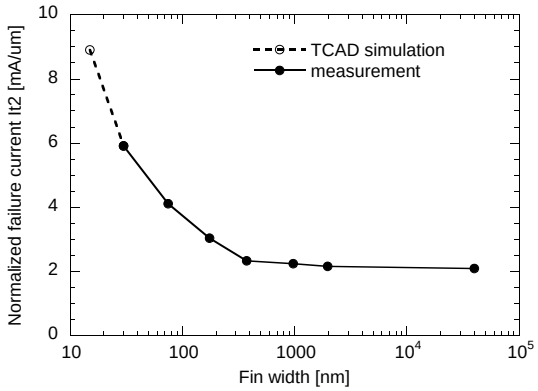

Figure 3.16: Intrinsic normalized It_2 as a function of fin width for FinFET devices with 75 nm gate length and various number of fins in bipolar mode. The 15 nm W_{fin} prediction based on 2D-TCAD simulation is included.

2D-TCAD and confirms the improved heat removal by the side gates and the source/drain landing pads for the narrower fins.

Based on these results, a prediction can be made for W_{fin} decreased below present minimum design rules, e.g. for 15 nm, by simulating for which TLP pulse the same temperature behavior is reached. In the case of W_{fin}=15 nm, the expected intrinsic performance is 8.9 mA/μm, compared to 6 mA/μm for 30 nm fin width, as can be seen in Fig. 3.16.

Holding voltage V_h

V_h as a function of W_{fin} for both NMOS and PMOS devices with short and

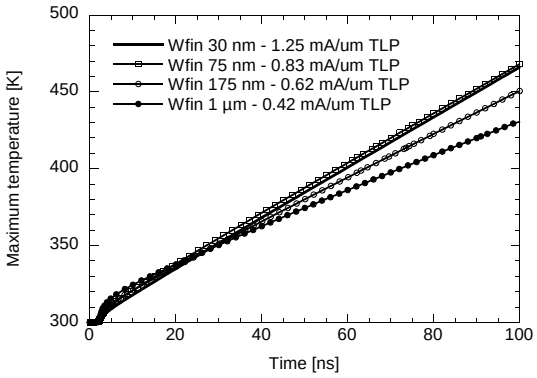

Figure 3.17: TCAD simulation of maximum temperature as function of time during different TLP current pulses according to the measured It_2 values for each W_{fin} variation.

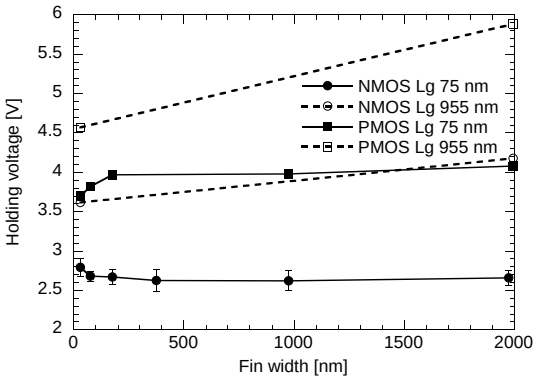

Figure 3.18: Holding voltage as a function of fin width for FinFET devices with 75 nm gate length or 955 nm gate length in bipolar mode.

long L_g is shown in Fig. 3.18. For NMOS devices with 75 nm L_g, V_h is almost independent of W_{fin}. A slight increase in V_h is measured for the narrowest W_{fin}, which can be attributed to two effects: first, the absence of free carriers due to the full depletion of the fin and secondly the possible but undesirable oversilicidation of the narrowest fins which increases carrier recombination [Hoff 05]. For PMOS devices with 75 nm L_g, V_h is almost constant with W_{fin} but decreases for the narrowest fins.

For NMOS and PMOS devices with large L_g, only two fin widths were available in the testchip (Fig. 3.18), but their holding voltage is expected first to remain constant and then to decrease with decreasing W_{fin} as well.

This behavior is explained by measuring the breakdown characteristics on gated diodes with floating gate of 80 nm L_g. A large dependence on W_{fin} is

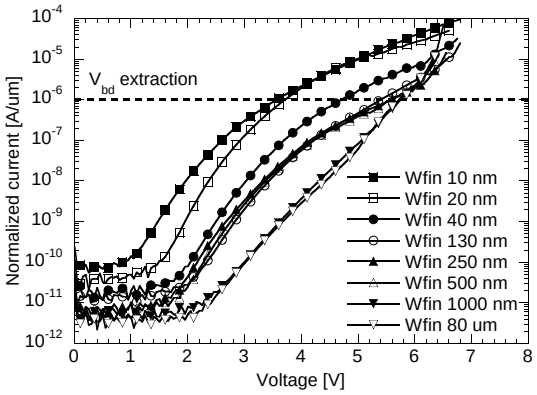

Figure 3.19: Measured breakdown characteristics normalized to W_{intr} for gated diodes with floating gate, L_g 80 nm and varying N and W_{fin}. The number of fins N depends on W_{fin}, ranging from 1 to 400. The breakdown voltage is extracted at 1 μA/μm and is shown in Fig. 3.20.

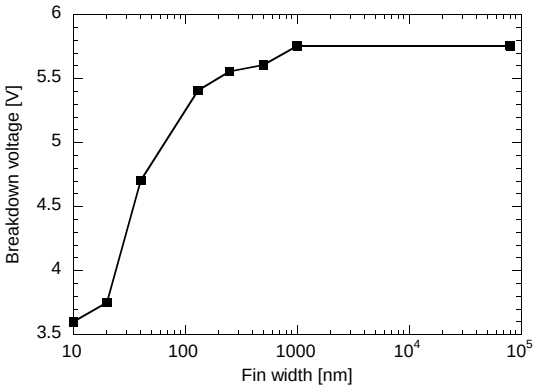

Figure 3.20: Extracted breakdown voltage for gated diodes with floating gate, L_g 80 nm and varying N as a function of W_{fin}. The breakdown voltage is extracted at 1 μA/μm.

measured even at low voltage levels (Fig. 3.19). At a normalized current level of 1 μA/μm, the junction breakdown voltage can be extracted as a function of W_{fin} (Fig. 3.20). When W_{fin} decreases, V_{bd} is seen to remain constant and eventually decrease which is similar to the V_h behavior. This V_{bd} behavior points to a complex 3D-doping profile dependency on W_{fin}.

Further, the impact of W_{fin} on V_h for PMOS devices is larger, which can be explained by the different dependency of the multiplication factor on the junction voltage for electron current M_n (NMOS case) and hole current M_p (PMOS case) as shown in Fig. 3.21 where an analytically calculated value is plotted [PhDTrémouilles]. M_p increases abruptly around the breakdown

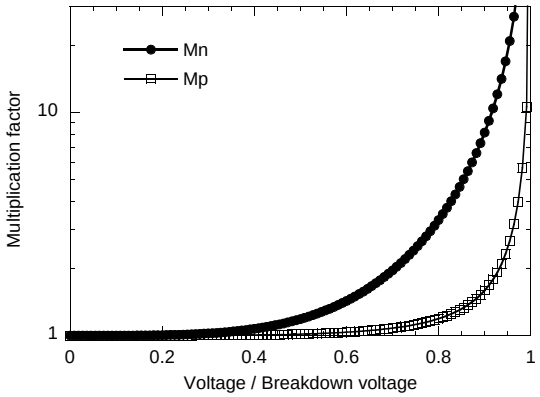

Figure 3.21: Comparison of calculated electron (Mn) and hole (Mp) multiplication factors as a function of voltage normalized to the breakdown voltage, according to [PhDTrémouilles].

voltage, while for NMOS devices a smoother variation of M_n with voltage is obtained. Therefore a shift in V_{bd} for PMOS devices translates almost entirely into a V_h shift, which explains the larger dependence for PMOS devices.

On-resistance R_{on}

R_{on} decreases with decreasing W_{fin} for both NMOS and PMOS devices when normalized to W_{intr}, as seen in Fig. 3.22, for devices with a fixed L_g of 75 nm. For narrow fins, NiSi grows from both the sidewalls and the top, so that the devices can become fully silicided, hence the lower R_{on} [Hoff 05]. A simplified schematic of the width-dependent silicidation is shown in Fig. 3.23. The statistical variation of R_{on} increases a lot when increasing the fin width. Since these devices have a gate length of 75 nm, the devices with the largest fin width lack control of SCE. Current starts to conduct already at very low voltages (Fig. 3.4), which makes extraction of the pure bipolar on-resistance very sensitive. For reference, also the normalized R_{on} versus W_{chan} is shown, which is more commonly used in technology-oriented papers. This normalization illustrates the gravity of the problem of series resistance for normal operation in FinFET devices [Dixi 05], as the resistance increases rapidly for the smallest W_{fin}.

3.4.1.3 Number of fins dependence

The scaling of the ESD robustness with the number of fins is verified through both TLP and HBM measurements. Besides changing the number of fins in a single 'finger' device, also a number of different device blocks, *nblocks*, can be placed in parallel, creating a 'multi-finger' device, where the total amount of

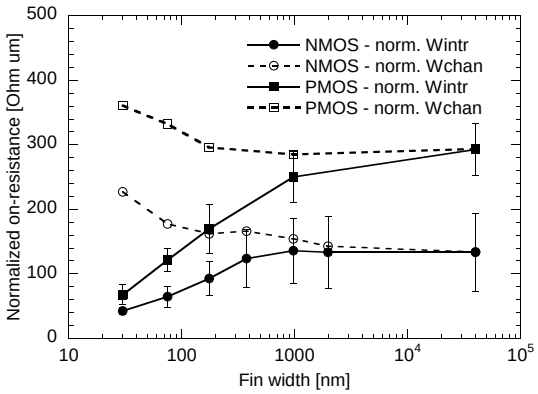

Figure 3.22: ESD on-resistance as a function of fin width for FinFET devices with 75 nm gate length in bipolar mode.

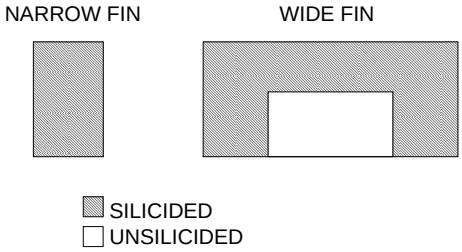

Figure 3.23: Simplified schematic fin cross-section, through the fin access region of a fully silicided narrow fin (left) and a partly silicided wide fin (right).

fins is N*$nblocks$. HBM measurements were performed on 16 parallel blocks of NMOS and PMOS devices with L_g of 75 nm and different W_{fin} ranging from 30 nm to 40 μm. The measurement results are summarized in Table 3.1. HBM withstand values of up to 3.75 kV were obtained, indicating scalability of the ESD performance up to levels as required by products. The same trends in terms of HBM performance normalized by W_{intr} as a function of W_{fin}, indicated in the last column of Table 3.1, were obtained as for TLP, see Fig. 3.12. Linear HBM scalability with $nblocks$ is demonstrated in Fig. 3.24 for N-type devices where each block consists of 400 fins of each 30 nm W_{fin} and 75 nm L_g. No direct comparison between NMOS and PMOS HBM failure levels should be made in this case as the measurements originate from different wafers. A clear comparison between NMOS and PMOS was already made in the two previous subsections.

As can be seen in Table 3.1, the HBM robustness stays constant for wide fin NMOS devices with increasing L_g, while it suddenly drops for PMOS, indicated by the shaded cells. These observations are matching the trends obtained from TLP results on single 40 μm NMOS and PMOS devices in Fig. 3.7 and Fig. 3.8

Table 3.1: Measured HBM results on 'large' NMOS and PMOS FinFET devices in bipolar mode. The HBM robustness is normalized to W_{intr}. The shaded cells indicate unexpected low performance.

Type	L_g **[nm]**	W_{fin} **[nm]**	**Number of fins x number of rows**	V_{HBM} **[kV]**	V_{HBM} **[V/μm]**
NMOS	75	30	400x16	2.4	12.5
NMOS	75	75	400x16	2.7	5.6
NMOS	75	155	400x16	3.5	3.5
NMOS	75	40000	1x16	2	3.1
NMOS	205	40000	1x16	2	3.1
PMOS	75	30	400x16	1.75	9.11
PMOS	75	75	400x16	2.4	5
PMOS	75	155	400x16	3.75	3.8
PMOS	75	40000	1x16	2	3.1
PMOS	205	40000	1x16	0.7	1.1

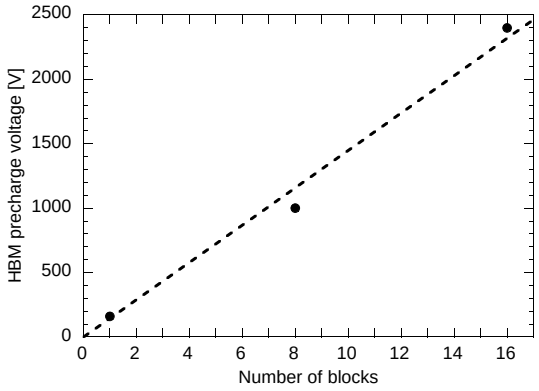

Figure 3.24: HBM robustness scaling as a function of number of blocks for N-type FinFET in bipolar mode with 400 fins of 30 nm W_{fin} and 75 nm L_g.

respectively, excluding non-uniform failure of the different device blocks of the PMOS devices to be the cause for this sudden decrease in robustness. In section 3.4.1.1, gate-oxide breakdown at the drain-gate overlap region was put forward as the possible cause for failure for wide fin PMOS devices with large L_g due to their larger holding voltage.

To further substantiate this finding, electrical failure signatures are shown in Fig. 3.25 for NMOS (left) and PMOS (right) devices. The devices have 205 nm L_g and consist of 16 blocks of a 40 μm fin. In Fig. 3.25 (left), the NMOS fails during a 2250 V HBM pulse at a current level around 0.2 A. This current level

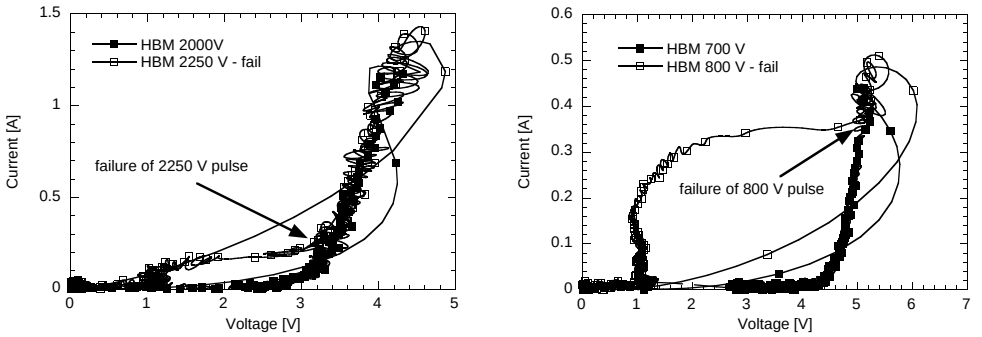

Figure 3.25: HBM-IV curves showing typical failure signatures for NMOS (left) and PMOS (right) in bipolar mode. The devices have 205 nm L_g and 16 blocks of a 40 μm fin.

is about 15 % of the peak current value. On contrary, for the PMOS device, Fig. 3.25 (right), it fails during a 800 V HBM pulse at a current level of about 67 % of the peak current value. This corresponds to a time to failure of roughly 300 ns for the NMOS device and 70 ns for the PMOS. This means that the NMOS fails almost at the end of the pulse, which is typical for power-related failures, while the PMOS fails at the beginning of the pulse, which is typical for voltage-related failures. Further, when analyzing the energy dissipated in the device as a function of time during the HBM pulse according to

$$E(t) = \int V(t)I(t)dt, \tag{3.14}$$

it is found that the total energy dissipated at the end of the pulse increases for the failure pulse compared to previous non-failing pulse in case of NMOS, Fig. 3.26 (left). On the other hand, for the PMOS, Fig. 3.26 (right), the total energy dissipated during the failing pulse is lower than during the previous passing pulse, indicating voltage-failure for the PMOS device.

A different number of parallel blocks of 40 μm wide single fin NMOS devices was stressed using TLP in bipolar condition to investigate the current uniformity of multi-block wide fin devices. Increasing the number of blocks from 1 to 4 and 16 reduces the normalized It_2 per W_{intr} (Fig. 3.27) which could indicate that some blocks did not turn on. Applying strain by tCESL improves the ESD performance. When applying additional ballasting resistance by increasing L_{SD} with 0.4 μm each, an increase in It_2 is noticed for the 16 parallel blocks. This ballasting resistance improves current uniformity. Strain was found in general to improve the ESD robustness, as described in more detail in section 3.6.5. Further, when using silicide blocking, as described in section 3.6.4, not only the robustness of a single fin device improves from 2 mA/μm to 3 mA/μm, but also the 16 parallel blocks maintain the same normalized ESD performance.

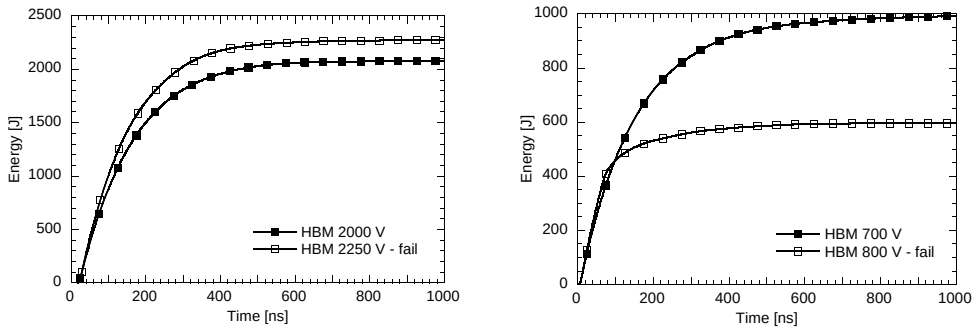

Figure 3.26: Energy dissipated in the device as a function of time during HBM pulses before and after failure, for NMOS (left) and PMOS (right) in bipolar mode. The maximum value at the end of the pulse corresponds to the total energy dissipated in the device during the stress. The devices have 205 nm L_g and 16 blocks of a 40 μm fin.

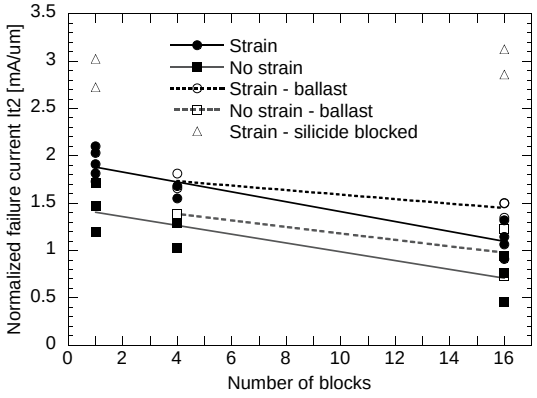

Figure 3.27: Intrinsic normalized failure current of N-type FinFET in bipolar mode as a function of number of blocks of 40 μm wide fin devices with 205 nm gate length.

3.4.1.4 Fin height dependence

A similar 2D-TCAD approach as described in section 3.4.1.2 can be used to understand the impact of reduced H_{fin}. When using a similar horizontal cross-section as in Fig. 3.13 (top) in section 3.4.1.2, the fin height is included in the device simulation by changing the area-scaling of the device. As vertical temperature gradients are disabled by such horizontal cross-section, changing the fin height by changing the area-scaling results in a perfect scaling of It_2 with H_{fin}.

However, since H_{fin} is a vertical geometrical parameter, a vertical simulation using corresponding cross-section as shown in Fig. 3.13 (bottom) is needed.

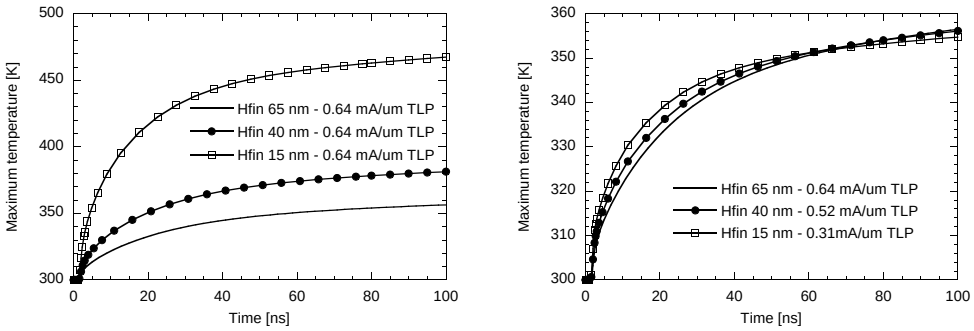

Figure 3.28: TCAD simulation of maximum temperature as function of time during a 0.64 mA/μm TLP current pulse (left) for different H_{fin}: 65 nm, 40 nm and 15 nm. All NMOS devices work in bipolar mode and have 75 nm L_g. Similar simulations using different TLP current pulses (right) allow prediction of It_2.

2D vertical TCAD TLP simulations using 0.64 mA/μm current density were performed comparing the present 65 nm H_{fin} with a scaled fin height to 40 nm and to Ultra-Thin-Body (UTB) of 15 nm [Auge 05] on NMOS in bipolar mode with 75 nm L_g. The maximum temperature during the TLP pulse is shown in Fig. 3.28 (left). Obviously, forcing the same amount of current through a thinner silicon film leads to increased heating. Using the methodology as described before, the current density needs to be reduced to 0.52 mA/μm for the 40 nm H_{fin} and to 0.31 mA/μm for 15 nm H_{fin} to yield the same maximum temperature, Fig. 3.28 (right). Based on these current ratios, an estimation of It_2 can be calculated.

Both simulations, comparing the horizontal TCAD (simple H_{fin} scaling) with the vertical TCAD, are shown in Fig. 3.29. The more realistic vertical TCAD simulation shows that when H_{fin} decreases, the It_2 performance is degrading less than what would be expected from simple H_{fin} scaling (horizontal TCAD). This improvement can be attributed to the fact that the vertical cooling by the top gate improves when the fin gets thinner because of reduced distance from the bottom of the fin (near the BOX) to the gate.

An important consideration needs to be made since this result is only valid for wide-fin devices, which is imposed by the 2D vertical TCAD. For narrow fin devices, the relative contribution from the top gate to the heat removal is much less because it is mostly governed by the side gates. 2D TCAD simulation for narrow fin devices requires a horizontal cross-section, which is contradicting the required vertical cross-section for H_{fin} scaling and hence such simulations require complex 3D TCAD. The expected dependency on H_{fin} for narrow fin devices lies somewhere in between both curves in Fig. 3.29. For H_{fin} scaling for narrow fin devices, the worst-case simple linear H_{fin} scaling according to

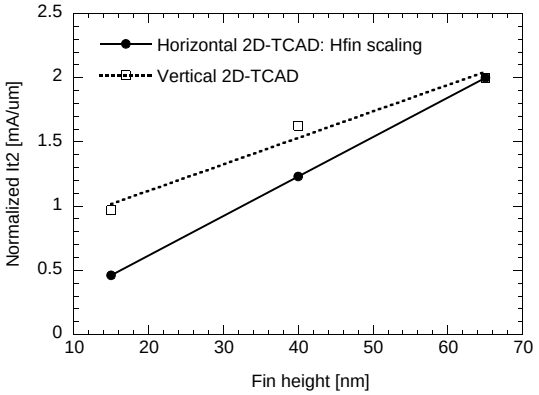

Figure 3.29: Comparison of horizontal and vertical 2D-TCAD It_2 simulation as function of H_{fin}. The more realistic vertical TCAD gives higher It_2 when H_{fin} decreases as compared to the horizontal TCAD, however it is only valid for wide fin devices.

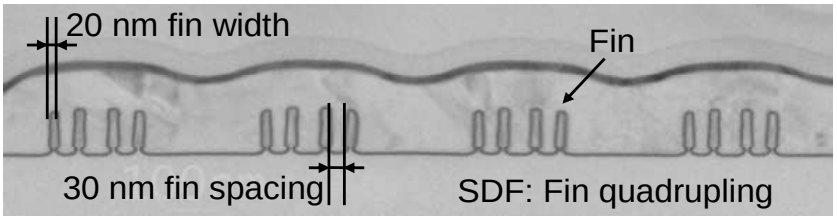

Figure 3.30: TEM image of fin quadrupling, obtained by Spacer Defined Fin methodology. The obtained fin width and fin spacing is 20 nm and 30 nm, respectively.

the horizontal cross-section is used when predicting the performance of the future IMEC processing targets in section 3.4.1.7.

3.4.1.5 Fin spacing dependence

With decreasing fin-to-fin spacing, the intrinsic robustness (W_{intr}, (3.1)) is expected to decrease because of increased fin-to-fin heating, while on the other hand the layout efficiency W_{layout} (3.2) might still be improved because of reduced area consumption. For example, the process feature of fin quadrupling, Fig. 3.30, using Spacer Defined Fins (SDF) can lead to a fin spacing even as narrow as 30 nm [Rooy 06]. Using the TCAD methodology of section 3.4.1.2, a prediction can be made for such future fin-to-fin spacing. The results are shown in Fig. 3.31. Despite that the intrinsic robustness is predicted to decrease with more than 60 % when going down to fin spacings of 30 nm, the layout efficiency is expected to increase with more than 30 %.

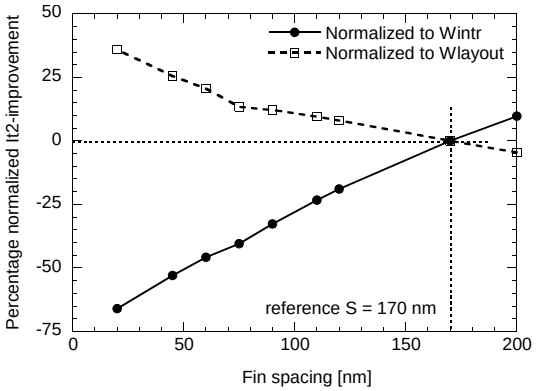

Figure 3.31: Percentage It_2 improvement normalized to W_{intr} and W_{layout} as function of fin spacing, as predicted by TCAD simulations for NMOS devices in bipolar mode with 75 nm L_g.

3.4.1.6 BOX thickness dependence

The impact of BOX scaling (T_{BOX}) and tradeoffs focusing on the short-channel characteristics have been experimentally verified in [Fuji 05] demonstrating improved V_T-rolloff and subthreshold slope characteristics for reduced T_{BOX}. On the other hand, increased junction capacitance resulting from BOX scaling reduces the inverter delay by 10 % for 5 nm T_{BOX}. Further, a decreased T_{BOX} is known to improve the heat dissipation [McDa 89] and therefore should be beneficial for ESD robustness.

As T_{BOX} is a vertical geometrical parameter, the cross-section as in Fig. 3.13 (bottom) is used, similarly as for the H_{fin} scaling and hence the results are only applicable for wide fin devices. The heating of a NMOS device with a ultra-thin BOX of 10 nm is compared to the reference 145 nm T_{BOX} by the TCAD simulation in Fig. 3.32 (right). The corresponding current pulses are shown on the left. Increasing the current density to 1.38 mA/μm for 10 nm T_{BOX}, yields the same maximum temperature after 100 ns as for 145 nm T_{BOX} during a 0.64 mA/μm TLP pulse resulting in a doubling of the expected It_2 level. The temperature profiles were captured during the 0.64 mA/μm TLP simulation after 80 ns for both 145 nm and 10 nm T_{BOX} and are shown in Fig. 3.33 on top and bottom respectively. The thicker T_{BOX} clearly prevents heat transfer to the substrate and hence causes increased heating of the silicon fins.

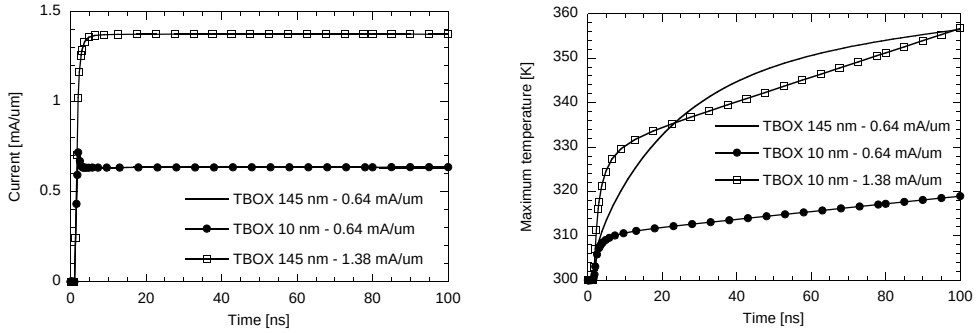

Figure 3.32: TCAD simulation of maximum temperature (right) as function of time during a 0.64 mA/μm and 1.38 mA/μm TLP current pulse for different T_{BOX}: 145 nm and 10 nm. The simulated current pulses are shown on the left. All NMOS devices work in bipolar mode and have 75 nm L_g.

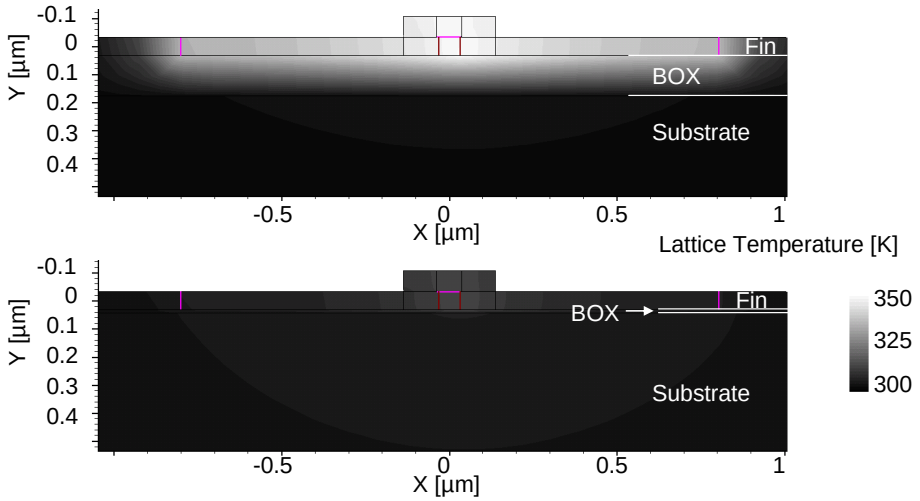

Figure 3.33: Temperature profiles captured at 80 ns during a 0.64 mA/μm TLP pulse for both 145 nm T_{BOX} (top) and 10 nm T_{BOX} (bottom).

3.4.1.7 32 nm and 22 nm technology node targets

The IMEC processing targets for the 32 nm technology node consist of 30 nm W_{fin}, 40 nm H_{fin} and 110 nm fin-to-fin spacing, compared to 30 nm, 65 nm and 145 nm for the current reference process, respectively. The reduced H_{fin} leads to a predicted decrease in ESD robustness by TCAD with a factor 0.62 (40/65) for these narrow fin devices as discussed in section 3.4.1.4. The reduced fin-to-fin spacing of 110 nm results in 23.3 % degradation in intrinsic performance (normalized to W_{intr}), but a layout efficiency improvement of 9.5 % (normalized to W_{layout}), according to Fig. 3.31 in section 3.4.1.5. Combining these results,

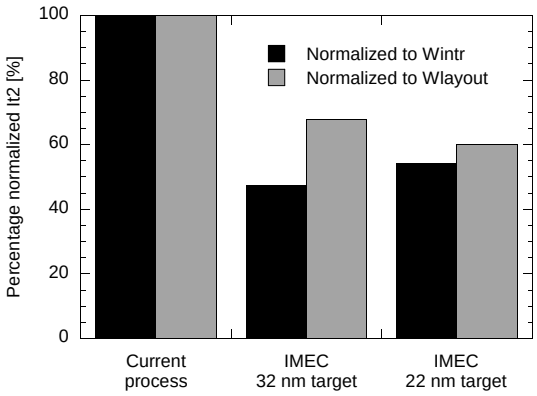

Figure 3.34: Prediction of It_2 performance for IMECs 32 nm and 22 nm processing targets.

the intrinsic performance for the 32 nm technology node is expected to decrease by 52.6 % and the layout efficiency by 32 % when compared to the current process.

The IMEC processing targets for the 22 nm technology node consist of 15 nm W_{fin}, 40 nm H_{fin} and 75 nm fin-to-fin spacing. This decreased fin width leads to a large intrinsic performance improvement of 48 % (Fig. 3.16). H_{fin} remains unchanged when going from the 32 nm to the 22 nm processing targets. The reduced fin-to-fin spacing of 75 nm results in 40.5 % degradation in intrinsic performance (normalized to W_{intr}), but a layout efficiency improvement of 13.4 % (normalized to W_{layout}), according to Fig. 3.31 in section 3.4.1.5. This results in an overall intrinsic performance degradation when compared to the current reference process of 45.8 % and layout efficiency degradation of 40 %.

These results are summarized in Fig. 3.34. When going from the 32 nm to the 22 nm prediction, the intrinsic performance is improved which is caused by the decreased fin width, however the layout efficiency is found to further decrease.

Fortunately, these future technology nodes will contain Selective Epitaxial Growth (SEG) by default, which will be shown in section 3.6.3 to almost double It_2 for NMOS devices with the shortest gate lengths hence restoring the degraded ESD performance in Fig. 3.34 to a certain extent.

3.4.2 MOS devices - active MOS-diode mode

When ESD stress is applied to gate and drain while the source is grounded, the device will operate in active MOS-diode mode. TLP measurements for narrow and wide N-type FinFET devices are shown in Fig. 3.35. These devices start to significantly conduct soon after their V_T is reached. The MOS-diode

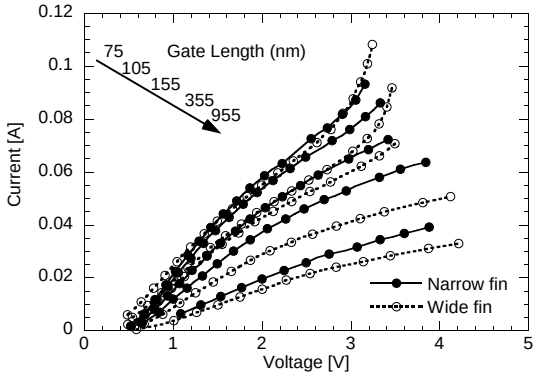

Figure 3.35: TLP-IV curves for different gate lengths of N-type FinFET in active MOS mode for both narrow (400 fins of 30 nm W_{fin}) and wide (single 40 μm) fin devices.

mode devices start to deviate from the linear behavior at high current levels which can be attributed to self-heating predominantly in the channel, while the voltage at the failure points are pushed higher compared to the bipolar mode. For the smallest gate lengths, some additional bipolar conduction is seen at high current levels when the slope of the IV-curve suddenly increases. In order to study active clamp MOSFETs, the TLP-IV curves of Fig. 3.35 could be limited up to the point of onset of self-heating where R_{on} starts to increase. In this section, we study the gate length and fin width dependence of the active MOS diode mode.

3.4.2.1 Gate length dependence

Different It_2 normalizations are shown in Fig. 3.36 as a function of L_g. It_2 decreases monotonically with increasing L_g, which is due to the increased R_{on} and hence power dissipation. Since the device operates in active MOS mode, also the normalization toward W_{eff} is included, which gives the same trends as toward W_{intr}. The MOS-diode mode provides higher It_2 for the smallest gate lengths than in bipolar operation, and lower It_2 for the larger gate lengths.

3.4.2.2 Fin width dependence

Narrow-fin devices are less area effective than wide fin devices as can be also seen in Fig. 3.37 where It_2/W_{layout} is shown as a function of fin width. This comes as no surprise, since the fin-to-fin spacing S is larger than the additional gate due to the sidewalls of the fin, $2{*}H_{fin}$. Similar as in bipolar mode,

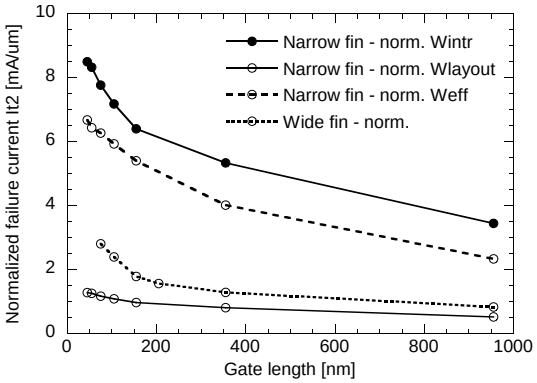

Figure 3.36: Normalized It_2 as a function of gate length for narrow and wide fin N-type FinFET devices in active MOS mode.

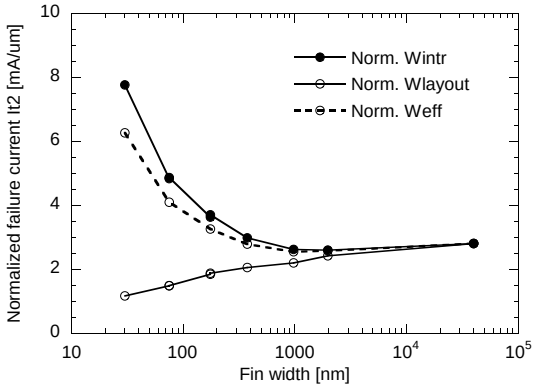

Figure 3.37: Normalized It_2 as a function of fin width for N-type FinFET devices with 75 nm gate length in active MOS mode.

narrow-fin devices in MOS diode mode have higher It_2 per intrinsic silicon width than wide fin devices due to better cooling of the fins.

3.4.3 Gated diodes

A cross-section of a gated diode is shown in Fig. 3.38 (left) and compared to the MOS-diode (right). The gated diode is sometimes also referred to as poly-diode. The gate of the gated diode is left floating to reduce gate leakage current and parasitic capacitance. The floating gate is also better with respect to the CDM threat [Putn 04].

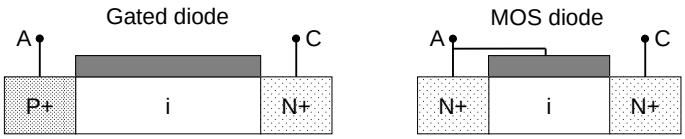

Figure 3.38: Cross-section of gated diode (left) compared to MOS diode (right).

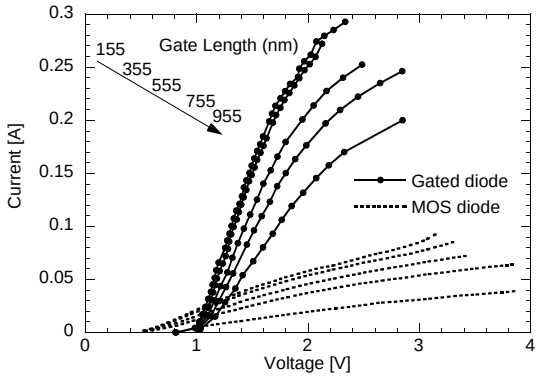

Figure 3.39: TLP-IV curves for different gate lengths of gated diodes in comparison with MOS diode mode. The devices have a fin width of 30 nm and 400 fins in parallel.

3.4.3.1 Gate length dependence

TLP-IV curves of gated diodes as a function of L_g are compared in Fig. 3.39 with the MOS diode mode. It is clear that gated diodes exhibit an improved It_2 and R_{on}, which is optimal for smallest L_g. Note that the gate lengths used for the gated diodes are larger than what can be used for the MOS devices (see Fig. 3.35) to accommodate for the N+ and P+ doping overlap on the gate due to mask misalignment.

3.4.3.2 Fin width dependence

When increasing W_{fin}, It_2 normalized per intrinsic silicon width decreases while it increases when considering layout Fig. 3.40, similarly as for the MOS diode mode. Since the leakage current is small for the gated diodes due the larger gate lengths needed, the optimum diode configuration in terms of ESD performance and area consumption is a wide fin diode with the smallest gate length possible.

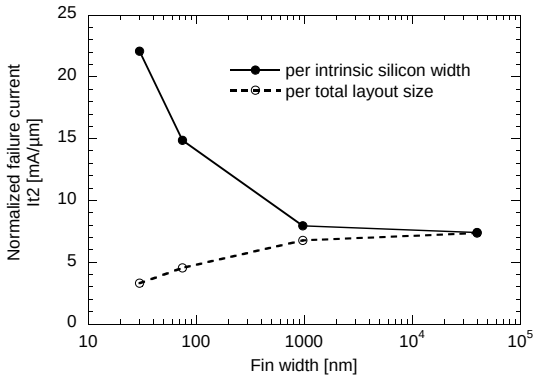

Figure 3.40: Normalized measured It_2 as a function of fin width for gated diodes with 555 nm gate length.

3.4.3.3 Diodes in series

In conventional bulk CMOS technologies, placing diodes in series requires the use of separate nwells for each diode. Therefore, the distance between two diodes is determined by minimum nwell to nwell spacing. However, in SOI technology, a single nwell can be drawn as the Shallow Trench Isolation (STI) cuts down till the BOX, thereby isolating each diode. This reduces the amount of required space. In FinFET SOI technology, the same layout technique can be used and no nwell is even present due to the usage of undoped bodies, see Fig. 3.41 (top). The anode is connected through the metal1 layer (M1) and several contacts (CT) down to the P+ active of the first diode. The cathode of the first diode is connected by CT-M1-CT to the anode of the second and so on.

Another technique which further reduces the required area is by merging the cathode active region with the anode active region of the next diode, see Fig. 3.41 (middle). The STI isolation is omitted. A good connection is formed through the silicidation process and the backend CT-M1-CT. For this technology, a reduced area of 25 % is obtained. Since the silicidation shorts the anode and cathode regions, further layout reduction is possible by omitting the intermediate CTs and M1 as in Fig. 3.41 (bottom). Since the anode and cathode regions don't need to accomodate any contacts, they can be made significantly smaller. However, omitting the intermediate CTs and M1 might have a drastic influence on It_2 as they are responsible for part of the cooling of the device during ESD stress. More investigation is required to determine the optimal layout strategy based on the layout technique as seen in Fig. 3.41 (bottom).

The ESD performance of the first two layout techniques (Fig. 3.41 (top and middle) is compared in Fig. 3.42. TLP measurements were done on three

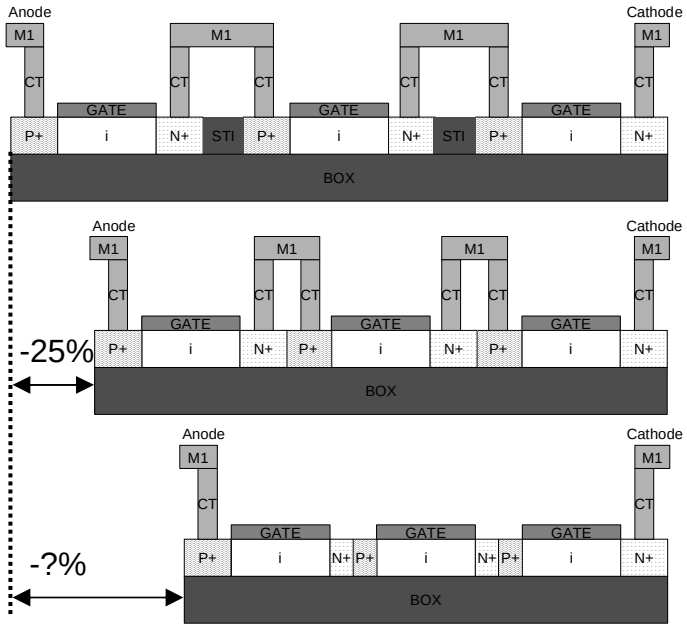

Figure 3.41: Cross-section of three gated diodes placed in series. The top figure shows separate devices, while in the middle the intermediate anodes and cathodes are merged into a single active area and are shorted by silicidation and the backend. By relying solely on the silicidation connection, the intermediate CTs and M1 can be removed resulting in a further layout reduction (bottom). Further investigation of this last technique is required.

diodes in series. Each diode has 80 nm L_g and consists of 400 fins of 20 nm W_{fin}. Selective Epitaxial Growth (section 3.6.3) was used to reduce the overall diode resistance. When omitting the STI isolation (Fig. 3.41 (middle)) a 16 % reduced on-resistance is measured for almost same It_2. This reduced resistance is due to the reduced interconnect resistance, caused by the parallel connection of the silicide and the CT-M1-CT chain. Note that this performance is obtained even with a 25 % area reduction. No devices were available without intermediate CTs and M1, according to Fig. 3.41 (bottom).

3.5 Benchmarking against Advanced CMOS Technology Nodes

The ESD results from our FinFET NMOS transistors and gated diodes have been benchmarked in [Russ 08] against the results obtained for advanced bulk and PDSOI CMOS technologies ranging from 130 nm down to 45 nm. Only thin oxide devices are considered in this section. The intrinsic ESD performance

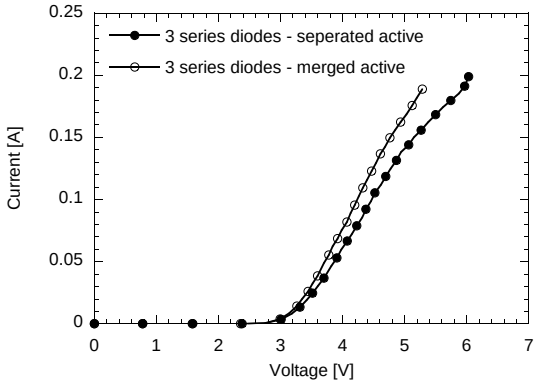

Figure 3.42: TLP-IV measurements for three diodes in series using different layout configurations. The diodes have 80 nm L_g and consist of 400 fins of 20 nm W_{fin}.

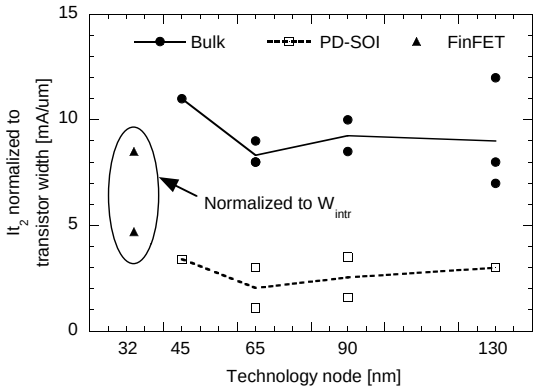

Figure 3.43: Intrinsic It_2 performance of NMOS transistors for different advanced CMOS technologies.

and the layout area efficiency is shown in Fig. 3.43-Fig. 3.44 for NMOS devices and Fig. 3.45-Fig. 3.46 for gated diodes respectively. For intrinsic performance, It_2 is normalized to the transistor width for bulk and PDSOI technologies, while a normalization to W_{intr} (see section 3.3) is used for FinFET devices.

The main conclusions from [Russ 08] are summarized below:

- For bulk technologies, the ESD performance of NMOS devices per transistor width stays relatively constant in the range of 7-12 mA/μm for silicide blocked devices. The ESD performance per area improves with technology scaling from 1.7 mA/μm^2 to 3.7 mA/μm^2 due to reduced size of silicide blocked regions.
- For bulk technologies, the ESD performance of gated diodes is decreasing with technology scaling, however not critical. An interesting boost in

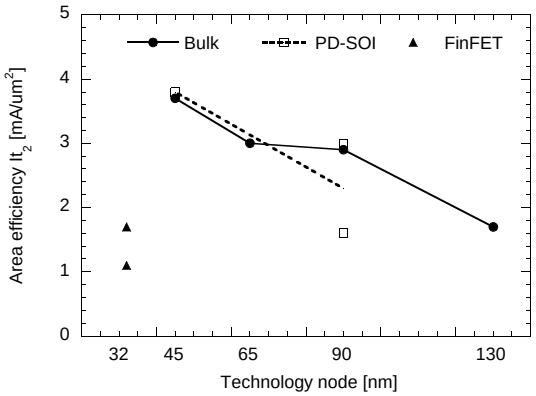

Figure 3.44: It_2 area efficiency of NMOS transistors for different advanced CMOS technologies.

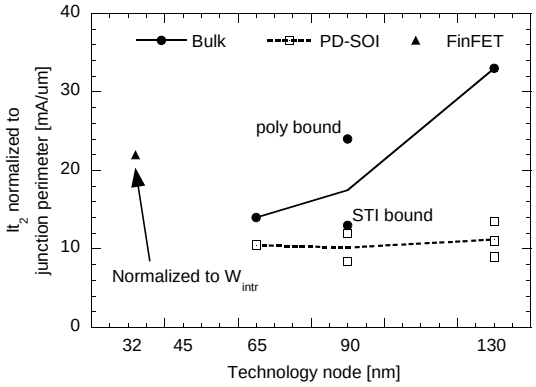

Figure 3.45: Intrinsic It_2 performance of gated diodes for different advanced CMOS technologies.

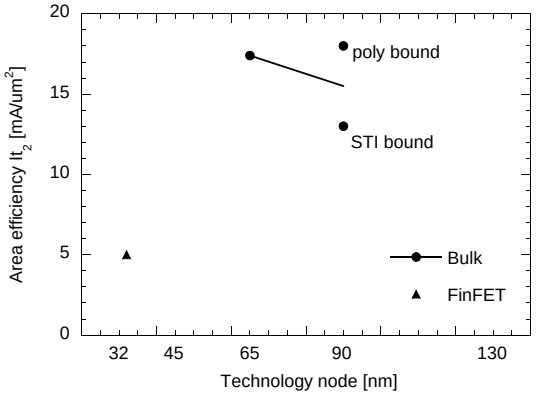

Figure 3.46: It_2 area efficiency of gated diodes for different advanced CMOS technologies.

performance is reported for poly bound (gated) diodes.

- For PDSOI technologies, the overall ESD performance of NMOS devices is by far weaker than in bulk and is clearly relatable to the poor heat conduction properties of the SOI material. Intrinsic performances up to 1.1-3.5 mA/μm are reported. Downscaling as such does not seem to pose a risk for the intrinsic ESD performance of SOI NFETs. The area-efficiency numbers for SOI (up to 3.8 mA/μm^2) can be as high as for bulk CMOS due to very area-efficient body-coupling method or the usage of really absolute minimum-dimension silicide blocked regions.
- For PDSOI technologies, the ESD performance of gated diodes per junction perimeter remains quite similar to that of bulk STI-bound diodes (13 mA/μm). A full benchmarking per area was not possible due to missing layout data but similar results are expected.
- For SOI FinFET technologies, processing improvements have been made demonstrating an area efficiency of 1.7 mA/μm^2 for NMOS transistors, reaching 50 % of those in bulk technologies.
- For SOI FinFET technologies, gated diodes show consistent performance and the per-area-values reach 30 % of those in bulk.

3.6 Process Technology Dependencies

The FinFET technology has to cope with some challenges such as a reduced mobility, high S/D access resistance, V_T variability, SCE control... Different process options are introduced to improve these parameters. These process options will also have an impact on the ESD robustness. Therefore, it is important to investigate their influence upfront. In this subsection, the impact of extension implants, fin doping on wide fin devices, Selective Epitaxial Growth (SEG), Silicide Blocking (SB) and strain is discussed.

3.6.1 Extension implants

In FinFET technology, extension regions are located next to the channel at the top and the sidewalls of the fin. Therefore an adapted integration scheme is needed to be effective in forming uniform extension regions in this 3-dimensional structure. Highly angled extension implants were demonstrated to yield higher performance devices [Kedz 03].

FinFET ESD robustness appears to be sensitive to extension-implant parameters as is shown on Fig. 3.47. The impact of two different implant conditions was analyzed: two-quadrant-implant with standard 45-degree tilt and two-quadrant-implant with 0-degree tilt implant, all with the same total dose. The 45-degree tilted implant provides the most uniform extension profile across

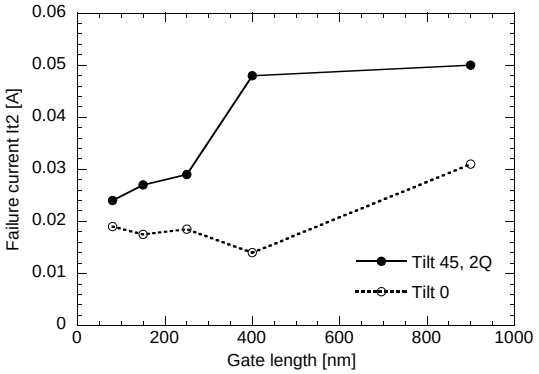

Figure 3.47: Maximum TLP current It_2 of N-type FinFET as a function of gate length for different extension implant parameters. The devices have a fin width of 25 nm, 320 nm fin spacing and 225 fins in parallel.

the fin and gives the best ESD results. In this case, the fin side walls still received a relatively high dopant dose. The perpendicular-to-the-fin tilt angle (0 degrees) leads to higher dopant concentration only in the top portion of the fin, while the sidewalls may be less doped. The latter implant condition led to less uniform extension profiles and to a significantly decreased ESD robustness, see Fig. 3.47.

3.6.2 Fin doping on wide fin devices

A very important ESD design constraint is the maximum allowed leakage current through the ESD clamp device. In section 3.4, wide fin devices were shown to have the best ESD performance per layout area. However, concluding from these results that the best ESD device would be a device with wide fins is not correct. This is because such a device needs also a longer gate to keep control on the SCE, which leads to an increased V_h and R_{on} (Fig. 3.9 and Fig. 3.11). Channel implants can be used to dope the fins and thereby reduce the leakage for wide fin devices. This makes them likely to be used for multiple-V_T devices, while the target for the standard core devices is without channel implants.

For narrow fin devices, V_T is determined by the workfunction of the metal gate since the full depletion makes tuning of V_T with implantation very difficult. Medium-V_T values are set by a mid-gap workfunction metal gate electrode. High-V_T targets can be achieved for wide fin devices by using fin doping [Coll 07]. Recently, a practical integration scheme has been shown by [Velo 08] to introduce a capping layer (LA_2O_3 or Dy_2O_3 for NMOS; Al_2O_3 for PMOS) between a high-κ host dielectric and the metal gate to successfully tune its workfunction towards band-edge and hence achieve low-V_T values.

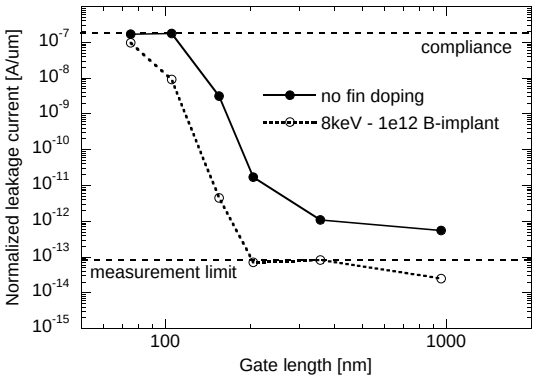

Figure 3.48: Normalized leakage current at 1 V drain bias as a function of gate length for 40 μm wide fin N-type FinFET devices and for different fin doping levels.

The impact of fin doping on the leakage current of 40 μm wide N-type and P-type FinFET devices is illustrated in Fig. 3.48 and Fig. 3.49 respectively. The leakage current was obtained at a drain bias of 1 V with source and gate grounded and was normalized toward W_{chan}. Fig. 3.48 shows that adding Boron in the NMOS fin body reduces the leakage current for a given gate length by increasing its V_T. As a consequence, such a wide fin device can meet leakage requirements with a smaller L_g which directly results in reduced V_h and R_{on}. More implant variations were available for PMOS devices, see Fig. 3.49. An increased Phosphorus dose results in decreased leakage current. When increasing the implant energy for the highest P-dose condition from 20 keV to 55 keV, the leakage increases again. Using these conditions, the dose is concentrated near the bottom of the fin and part of the dose is lost in the buried oxide.

The impact of channel implants on the ESD behavior of wide fin NMOS devices is studied in Fig. 3.50. This figure shows the TLP-IV curves of a wide fin NMOS device with 205 nm L_g, with and without fin doping. A leakage current decrease by three orders of magnitude was measured by changing the V_T by introducing doping, corresponding to Fig. 3.48, while the other ESD performance parameters remained unchanged.

If channel implants are available, they should preferably be used for the ESD protection devices. When not available, one might consider to introduce channel implants specifically optimized for ESD purposes. This would also open up the window for implementation of other types of ESD protection devices such as SCR devices.

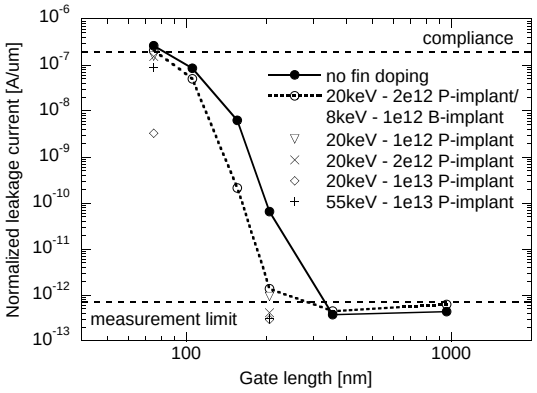

Figure 3.49: Normalized leakage current at 1 V drain bias as a function of gate length for 40 μm wide fin P-type FinFET devices and for different fin doping levels.

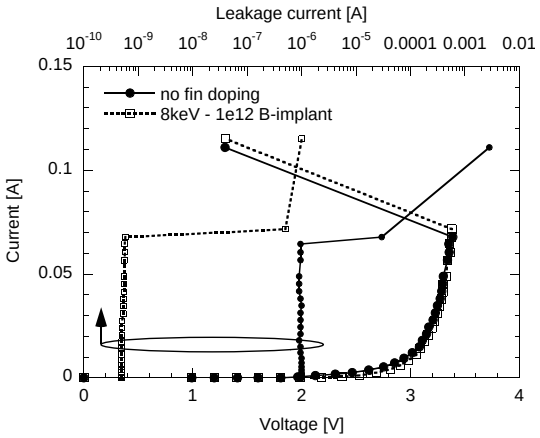

Figure 3.50: TLP-IV curves for wide fin N-type FinFET in bipolar mode for different fin doping levels. The devices have a gate length of 205 nm.

3.6.3 Selective Epitaxial Growth

For the technology nodes at and below 32 nm, fin widths smaller than 10 nm will be needed to maintain good short channel behavior [Coll 07]. For these narrow fin devices, the access resistance, which is the resistance from the source/drain landing pad to the region underneath the gate, is very high. SEG on source and drain areas is typically used to reduce the contact resistance [Kedz 03] by almost 50 %. Due to the increased silicon volume, also the problem of over-silicidation (particularly NMOS) is greatly reduced, because the SEG gets silicided instead of the fin. This leads to a decrease in leakage current by 4 orders of magnitude [Coll 07c].

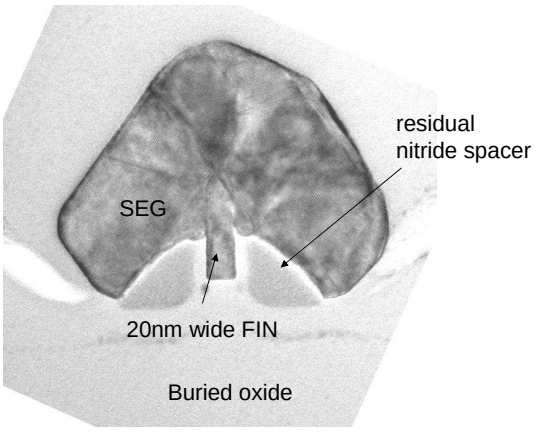

Figure 3.51: Selective Epitaxial Growth (SEG) over one fin.

As can be seen in Fig. 3.51, silicon is grown by SEG selectively on all exposed silicon surfaces, i.e. on top of the fins, at the sidewalls of the fin access regions, and on top of the S/D landing pad regions. Where the gate covers the fin (i.e. the channel region), obviously no growth of SEG takes place. Also, SEG does not grow on the gate electrode, since it is protected by a hard mask to avoid bridging between source and drain.

Fig. 3.52 and Fig. 3.53 show the influence on narrow fin N- and P-type FinFETs respectively for different L_g. For both NMOS and PMOS, SEG increases It_2 drastically and lowers R_{on}, while the dependency on L_g remains similar. The improved robustness can be mainly attributed to the better heat removal and storage from the drain-body junction of the fin due to the larger fin dimensions in the source and drain access region. The PMOS behavior is less improved by SEG because in general for PMOS FinFET devices the contact resistance is not the limiting factor but the lower carrier mobility.

Also the reduction of over-silicidation is a factor which increases It_2 for SEG devices due to improved current uniformity. The result is lower measurement variation for SEG devices and a decrease of V_h (Fig. 3.52). The Schottky contact created during over-silicidation is a source for recombination of the carriers generated by impact ionization during turn-on of the parasitic bipolar, lowering its β [Hoff 05]. As a consequence, the required voltage to sustain bipolar operation is lower than when over-silicidation would have occurred. Since the PMOS has less problems with over-silicidation due to the presence of Boron in the P+ S/D regions which slows down the silicidation process, the decrease in V_h is much less pronounced.

Fig. 3.54 shows intrinsic normalized It_2 for NMOS in bipolar mode from a recent 300 mm FinFET device lot with SEG included in the standard process flow. The devices have a gate length of 45 nm. With SEG, the improved

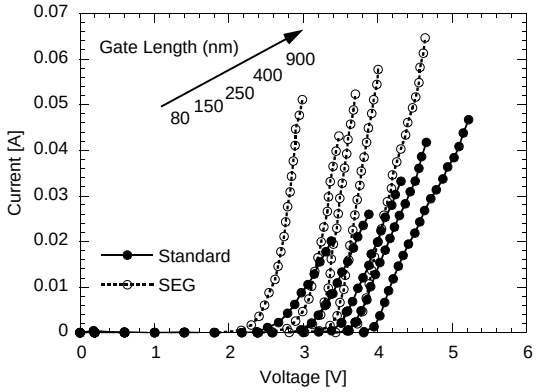

Figure 3.52: TLP-IV curves of N-type FinFET in bipolar mode as a function of gate length for wafers processed with and without SEG. The devices have a fin width of 25 nm and 225 fins in parallel.

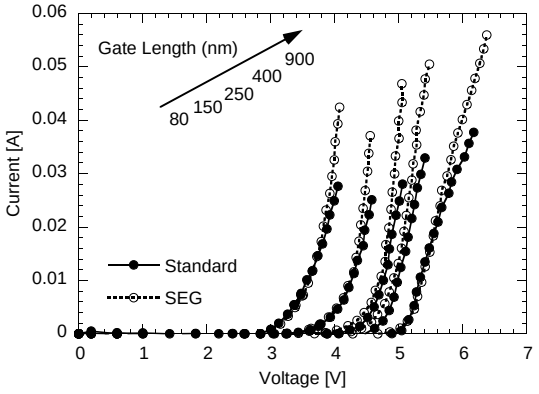

Figure 3.53: TLP-IV curves of P-type FinFET in bipolar mode as a function of gate length for wafers processed with and without SEG. The devices have a fin width of 25 nm and 225 fins in parallel.

intrinsic It_2 due to the 3D-cooling of the fins remains clearly visible as described in section 3.4.1.2.

However, for this last set of data, two additional process constraints make a direct evaluation of the impact of SEG very difficult. First, due to the testchip design rules, the fin spacing S depends on W_{fin}. For $W_{fin} \leq 40$ nm, the fin pitch is constant at 200 nm, giving a fin spacing of:

$$S = 200\ nm - W_{fin} \tag{3.15}$$

When $W_{fin} > 50$ nm, the fin spacing itself is constant instead of the fin pitch:

$$S = 300\ nm \tag{3.16}$$

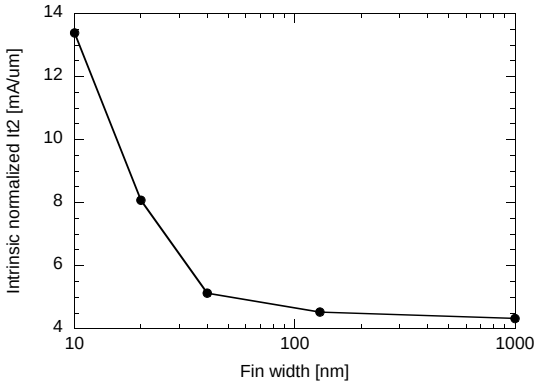

Figure 3.54: Failure current It_2 normalized to W_{intr} for NMOS with SEG in bipolar mode. The devices have 45 nm L_g. Narrow fins have intrinsic better It_2 performance.

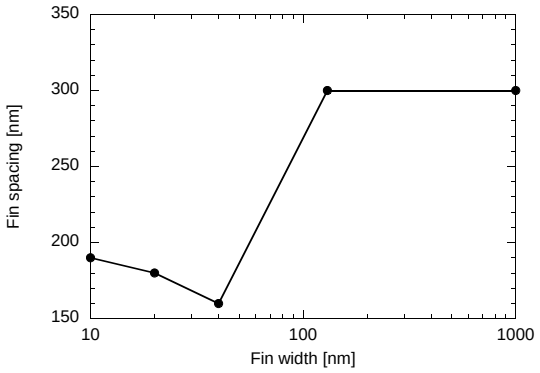

Figure 3.55: Dependence of fin spacing S on W_{fin}.

A graphical representation of the dependence of S on W_{fin} for the devices in Fig. 3.54 is shown in Fig. 3.55. For example, when W_{fin} is decreasing from 40 nm to 10 nm, the fin spacing increases from 160 nm to 190 nm respectively. According to section 3.4.1.5, this increased S leads to roughly 10 % increased intrinsic It_2. This means that the improved performance for narrow fin devices in Fig. 3.54 is not solely due to improved cooling of the fins, but also due to increased fin spacing.

Secondly, the amount of SEG growth depends on the fin width, since it is depending on crystal orientation [Coll 08]. In this case, the sidewalls have a {110} orientation with <110> current direction. The actual amount of Si grown on a narrow fin will be smaller than on a wide active area. All these combined elements have to be taken into account when studying the impact of SEG based on the data shown in Fig. 3.54.

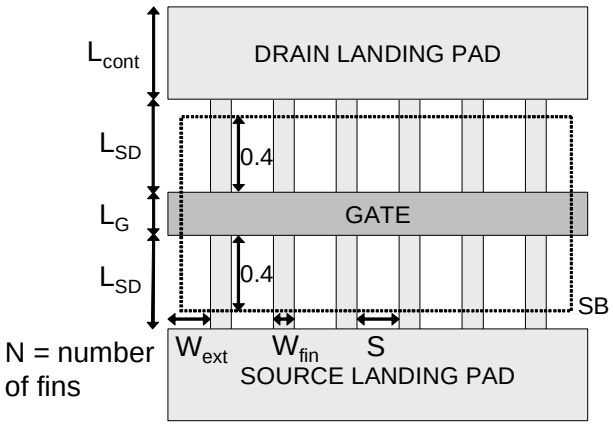

Figure 3.56: Top layout view of a FinFET device including silicide blocking (SB) mask.

Note that the introduction of SEG drastically increases the parasitic capacitances, as explained further in section 3.7.1.

3.6.4 Silicide Blocking

Silicide Blocking (SB) is known as a technique to improve ESD robustness [Amer 02]. A silicide blocking region is applied in the current work to FinFETs which extends 0.4 μm over the gate in both direction of source and drain (Fig. 3.56). L_{SD} was increased to accommodate the silicide blocking region. TLP-IV curves are shown in Fig. 3.57 for narrow (left) and wide (right) N-type FinFET devices with and without silicide blocking and in Fig. 3.58 for P-type devices. In the case of NMOS, It_2 increases for both narrow and wide devices. For narrow fin devices, the silicide blocking ensures more current uniformity at high current levels amongst the different fins. However, the leakage current increases progressively, making an accurate determination of It_2 difficult. This could be caused by an increasing number of failed fins. For wide fin NMOS devices, It_2 is increased due to the improved uniformity within the single fin, and both the fully silicided and silicide blocked devices fail abruptly. Further, the removal of over-silicidation due to silicide blocking can be seen by the measured decrease in V_h for silicide blocked devices, similar as for SEG, see section 3.6.3. Also some over-silicidation seems to be present for wide fin devices, based on their decrease in V_h. On the other hand, SB does not seem to improve It_2 for both narrow and wide PMOS devices as seen in Fig. 3.58. A possible explanation could be the occurrence of gate-oxide breakdown as described earlier in section 3.4.1.1.

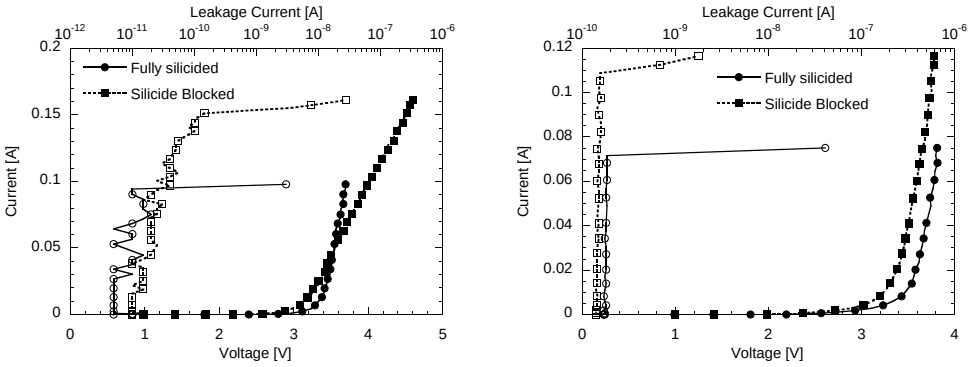

Figure 3.57: TLP-IV curves for narrow (left) and wide (right) fin N-type FinFET devices with and without silicide blocking in bipolar mode with 355 nm gate length. The narrow fin device consists of 400 fins of 30 nm width, while the wide fin device has a single 40 μm fin.

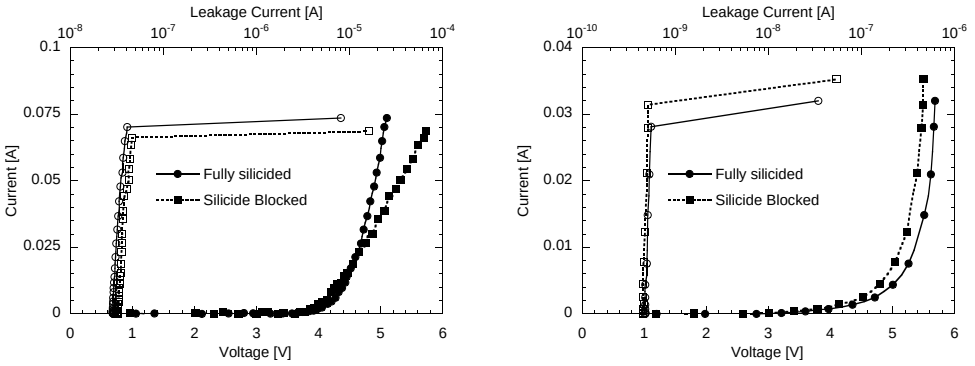

Figure 3.58: TLP-IV curves for narrow (left) and wide (right) fin P-type FinFET devices with and without silicide blocking in bipolar mode with 355 nm gate length. The narrow fin device consists of 400 fins of 30 nm width, while the wide fin device has a single 40 μm fin.

3.6.5 Strain

Both TLP and HBM measurements are used to provide new insights into the high-current behavior of strained FinFET devices during an ESD event in section 3.6.5.1 and section 3.6.5.2 respectively. Using TLP measurements, strain is found to improve the ESD robustness up to 20 % in NMOS FinFET devices, while HBM-IV measurements reveal a different failure mechanism for strained versus non-strained devices for MOS devices in parasitic-bipolar mode.

3.6.5.1 Based on TLP analysis

When starting from a {100} silicon wafer with [110] current direction, the electron mobility in narrow fin devices is degraded as the current flows mainly in the sidewalls of the device [Shen 91] [Yang 03]. These sidewalls have a less favorable crystal orientation compared to the top channel. In order to improve the performance, strain is introduced. For both nMOS and pMOS, a 100 nm thick tensile and compressively strained nitride layer with an intrinsic stress of 0.8 GPa were respectively deposited [Coll 08]. A NMOS drive current improvement up to 20 % was measured with tensile Contact Etch Stop Layer (tCESL). The improvement seen for pMOS due to compressive strain is lower, about 10 % [Coll 08] [Shin 05]. Since the PMOS improvement due to compressive strain is only moderate and almost no degradation of the PMOS due to tCESL is measured, a more simple process scheme with only tCESL can be used [Coll 05b].

The intrinsic normalized It_2 for narrow NMOS and PMOS devices with and without tCESL as a function of L_g is shown in Fig. 3.59. An improvement up to 20 % in It_2 is measured for NMOS devices with medium L_g. Only a slight reduction in It_2 is measured for PMOS due to the tCESL. While V_h is unchanged for PMOS, a decreased V_h is measured for NMOS devices with the smallest L_g as seen in Fig. 3.60. This improvement is due to improved electron mobility and is most pronounced for small to medium gate lenghts because they are more impacted by CESL. This improved mobility leads to reduced electric fields, which further improves the high field mobility. The explanation for the most improved It_2 for medium L_g for NMOS devices can be found in the extraction of the ESD on-resistance R_{on} normalized per W_{chan}, Fig. 3.61. A decrease in R_{on} is measured for NMOS devices with medium L_g, which can be attributed to the mobility improvement due to strain. Since the strain is transferred to the channel via the sides of the source and drain landing pads, for the largest L_g the impact of strain is minimal which results in an unchanged R_{on}. On the other hand, for smallest L_g, R_{on} is dominated by the access resistance and not by the channel resistance. No difference in heat conduction capability of the strain layer is expected due to the relative low strain level of 800 MPa. Note that SEG will reduce this mobility improvement, since the additional epitaxial grown silicon on the fin increases the distance of the SiN liner to the channel [Coll 05b] and hence reduces its impact. Yet the advantages of SEG have become very obvious in section 3.6.3.

3.6.5.2 Based on HBM analysis

HBM-IV measurements were used to investigate the impact of strain on different type of FinFET devices, namely FinFET NMOS devices in active MOS-diode

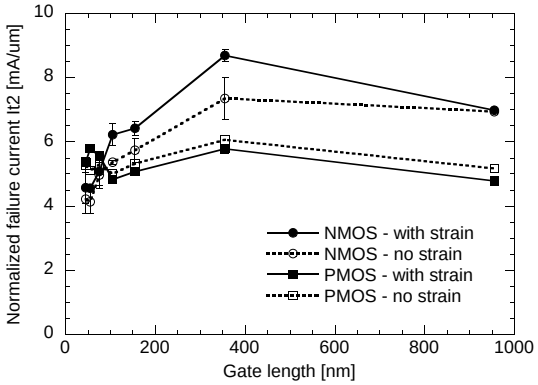

Figure 3.59: Normalized It_2 to intrinsic silicon width as a function of gate length for FinFET devices in bipolar mode for wafers with and without tCESL. The devices have a fin width of 30 nm and 400 fins in parallel.

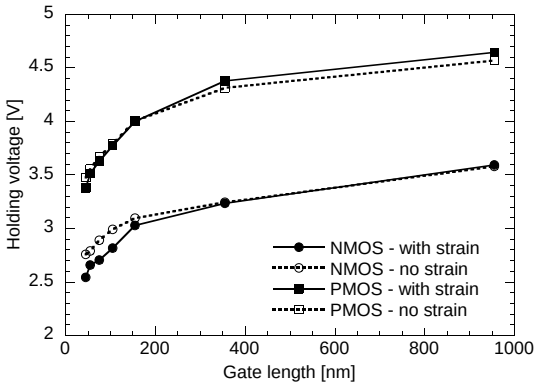

Figure 3.60: Holding voltage of FinFET in bipolar mode as a function of gate length for wafers processed with and without tCESL. The devices have a fin width of 30 nm and 400 fins in parallel.

mode and in parasitic-bipolar mode and gated FinFET diodes. A 10x increase in DC leakage current was considered as device failure.

FinFET NMOS devices in active MOS-diode mode

Fig. 3.62 shows the HBM-IV curves, just before failure, for NMOS FinFETs with and without strain stressed in MOS-diode mode, where the ESD stress is applied to gate and drain while the source is kept grounded. The devices start to conduct current soon after reaching their threshold voltage. Strained samples exhibit a larger mobility, which is seen in increased MOS drive current. They fail at a 15 % increased HBM failure level compared to non-strained devices as seen in Fig. 3.63. The ESD robustness decreases with increasing gate length (Fig. 3.63), which is due to increased self-heating. As confirmed

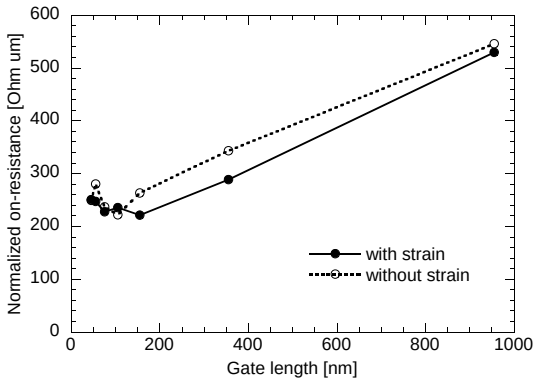

Figure 3.61: ESD on-resistance normalized to total channel width as a function of gate length for narrow N-type FinFET devices with and without tCESL in bipolar mode.

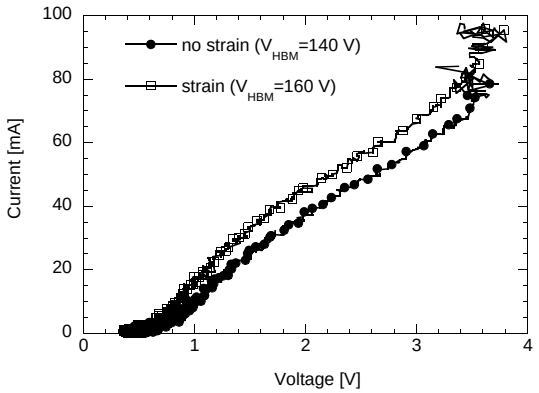

Figure 3.62: HBM-IV curves just before failure for strained and non-strained NMOS FinFETs stressed in active MOS-diode mode. The gate is tied to the drain while the source is kept grounded. The devices have a gate length of 155 nm. Strain improves the mobility and hence the MOS-drive current. Also the HBM robustness is increased.

by TCAD simulations (Fig. 3.64), the increased ESD performance for strain is due to lower temperature (right) in the fins owing to higher electron mobility (left).

On the contrary to the lower heating in strained devices, the thermal properties of the SiN strain layer were found not to improve the cooling of the fins (Table 3.2). Indeed, the thermal conductivity of the 100-nm SiN strain layer is about four times lower than the one of the 50-nm SiC layer, which is used instead for the non-strained devices between the active device area and the low- layer. On the contrary, the specific heat capacitance is about the same in

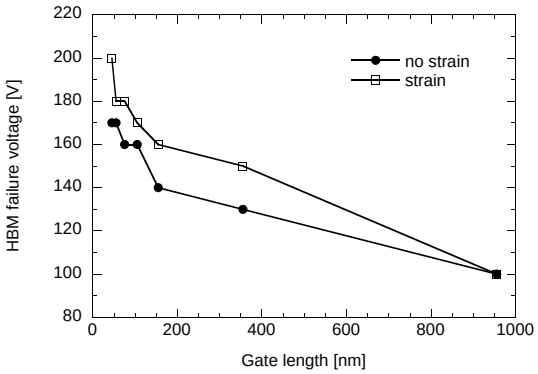

Figure 3.63: HBM failure voltage as a function of gate length for N-type FinFETs in MOS-diode mode. Strain improves the ESD robustness up to 15 % for short and medium gate lengths.

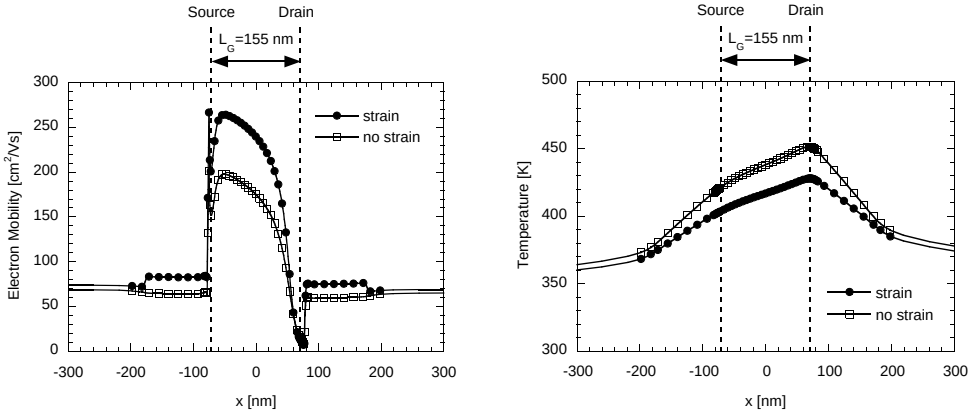

Figure 3.64: TCAD-simulated mobility (left) and temperature profile (right) along the fin length during a 140 V HBM pulse in MOS-diode mode. Mobility and temperature were captured during the maximum HBM current at 10 ns. Strain increases the mobility and results in a decreased temperature. The temperature profile exhibits a smooth peak, located at the drain junction.

both the cases.

FinFET NMOS devices in parasitic-bipolar mode

Fig. 3.65 shows the HBM-IV curves, just before failure, for NMOS FinFETs with and without strain stressed in parasitic-bipolar mode. Strained devices exhibit a lower holding voltage because of a higher common-emitter current gain (β) of the parasitic Bipolar Junction Transistor (BJT) due to larger electron mobility. Moreover, strain improves the ESD robustness up to 30 % (Fig. 3.66), which cannot be attributed only to lower power dissipation as for the MOS-diode mode. In [Goss 06] it was shown by failure analysis that

Table 3.2: Thermal parameters of the materials used for the manufacturing of strained and non-strained FinFET devices.

Material	**Thermal conductivity [W/cmK]**	**Specific heat capacitance [J/gK]**	**Melting point [K]**
Si	1.5	0.7	1687
SiN	-	-	1023
Si_3N_4 (like the strain layer)	0.28	0.73	2173
SiC	1.14	0.75	3003
SiO_2	0.014	1	1923
low-κ (silica based)	$\sim$ same SiO_2	$\sim$ same SiO_2	-

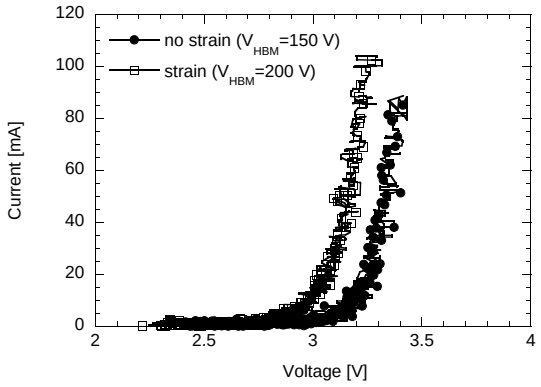

Figure 3.65: HBM-IV curves just before failure for strained and non-strained NMOS FinFETs, where the ESD current is discharged through the parasitic bipolar of the device. The devices have a gate length of 155 nm.

FinFETs in bipolar mode can show non-uniformity at high current levels. This non-uniform failure is typical for ESD protection devices based on avalanche breakdown and is due to current instability at high current levels [Vash 08]. The different gate-length dependency in FinFET devices with strain (with a maximum sensitivity at medium L_g) compared to no-strain gives a first indication for a change in failure current uniformity. Another indirect proof can be found in the increased spread in It_2 from the TLP measurements as seen by the larger error bars in Fig. 3.59 for NMOS devices without strain as compared to with strain.

Further, a different failure signature is also observed in the voltage versus time waveforms between strained and non-strained devices (Fig. 3.67 and Fig. 3.68). When a non-strained FinFET fails in bipolar mode, an unusual ringing of the

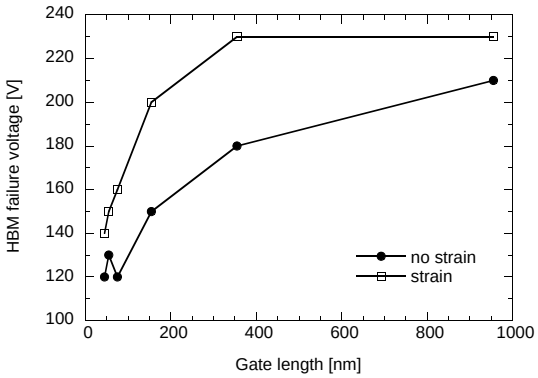

Figure 3.66: HBM-failure voltage as a function of gate length for N-type FinFETs in parasitic-bipolar mode. Strain improves the ESD robustness up to 30 % for medium gate length.

HBM voltage waveform is observed at the beginning of the pulse (Fig. 3.67 (left)). Such ringing can be caused by a set of failing fins which become shorted, causing a voltage drop. Subsequently, these fins will take all the current and fuse to an open, leading to a voltage increase. The next set of fins will then fail to a short, repeating the sequence. This ringing indicates a large failure non-uniformity amongst the different fins. A modest increase in DC leakage current (∼100 nA) is seen (Fig. 3.69 (left)), indicating the occurrence of only a few damaged fins (i.e. filamentation between source and drain). During the next higher ESD stress level, these (pre-)damaged fins may take a large amount of the current and hence are burnt open. Consequently, a few other fins take over, until finally all fins are fused. This unstable mechanism is noticed in the voltage waveform where an increase in the amplitude of the ringing is seen, followed by transition to a high-resistive 'open' condition (Fig. 3.67 (right)). However, when a strained FinFET fails, the voltage drops down during the stress (Fig. 3.68). The post-stress electrical measurements (Fig. 3.69 (right)) suggest filaments between source and drain by the abrupt leakage increase (∼mA). The ringing behavior and subsequent 'open' condition are not observed anymore. This indicates a more uniform failure-current distribution for strained devices, meaning the different fins fail more simultaneously, i.e. more simulateneous filamentation, preventing fusing of single fins.

Moreover, the same experiments were performed for non-strained and strained FinFETs with single 'fin' devices of 40 μm (like planar SOI MOSFETs) in parasitic-bipolar mode. Such devices have much less problems with current uniformity at high current levels, since now the current is located within one single wide fin, see section 3.4.1.1. Here, strain improves the ESD robustness up to 14 %, however all devices fail to a short condition irrespective of strain. This again indicates that the ringing and subsequent 'open' are due to the

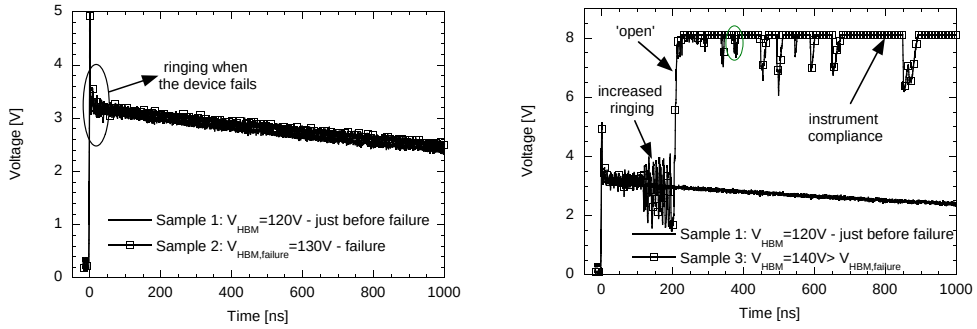

Figure 3.67: HBM-voltage waveforms for a device without strain in bipolar mode with 75 nm gate length. Left: when the device fails, a small amount of ringing in the waveform is observed. Right: when the stress level is increased on a fresh sample (V_{HBM}=140 V>$V_{HBM,failure}$=130 V), the amplitude of such ringing increases until it diverges to a high-resistive 'open' condition.

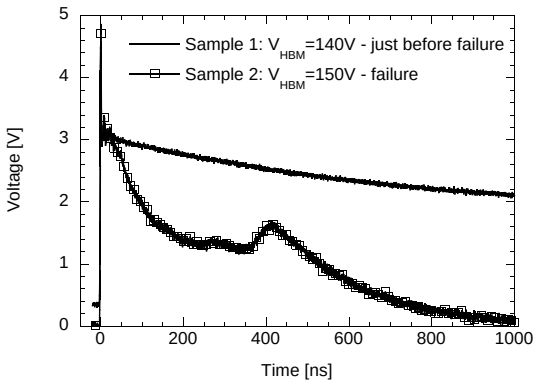

Figure 3.68: HBM-voltage waveform before and during failure of strained FinFET in bipolar mode with 75 nm gate length. When the sample fails, the voltage drops to a 'short'.

non-uniform failure between separate fins in multi-fin FinFETs.

The improved failure current uniformity for multi-fin strained FinFET devices can be attributed to a different temperature profile at the drain junction compared to devices without strain, as simulated by TCAD (Fig. 3.70). Besides the lower maximum temperature for strained devices, also the temperature profile is less peaked. This most likely makes the devices less vulnerable to thermal runaway of individual fins, which improves the failure current uniformity. In MOS-diode mode, the ringing behavior was not observed in both no-strain and strain cases, suggesting uniform failure over the entire fin array. Moreover, similar trends and voltage failure signatures are observed for gated FinFET diodes, which were shown to fail uniformly in [Russ 07]. Failure

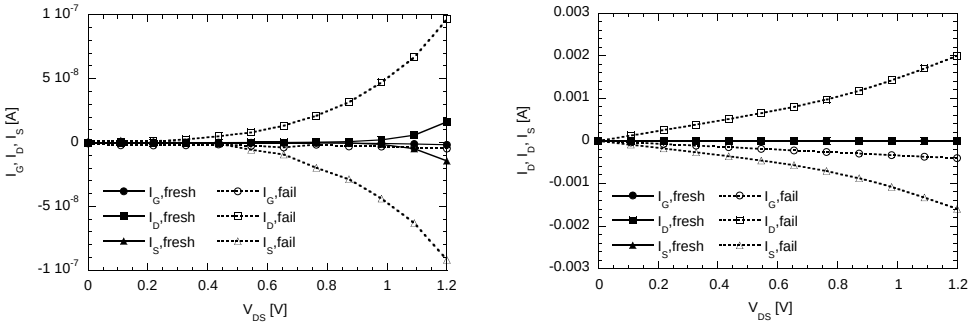

Figure 3.69: I_{DS}-V_{DS} (at V_{GS}=0 V) curves before and after failure for FinFETs without (left) and with strain (right). In the case of no strain, the drain current after failure is in the order of hundreds of nA's, indicating filamentation between source and drain of a few fins. In the case of strain, the current flowing from source to drain shows a large increase up to several mA's, indicating the formation of filaments in almost all fins.

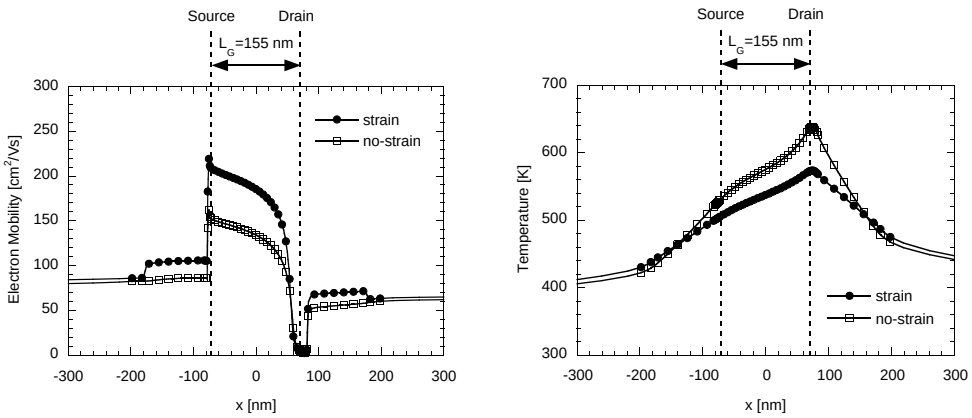

Figure 3.70: TCAD-simulated mobility (left) and temperature profile (right) along the fin length during a 140 V HBM pulse in bipolar mode. Mobility and temperature were captured during the maximum HBM current at 10 ns. Strain increases the mobility and results in a decreased temperature, which also is less peaked. The temperature profile is maximal at the drain where the impact ionization is highest and a sharper peak and higher temperature are seen contrary to the diode mode (Fig. 3.64).

analysis could be performed to support this hypothesis.

To further substantiate the finding of failure current non-uniformity between different fins, other ESD techniques, which are well known to improve the current uniformity at high current levels [Amer 02], were investigated. For non-strained FinFETs, an improvement of the ESD robustness can be obtained by providing finger ballasting as shown in Fig. 3.71, obtained by increasing

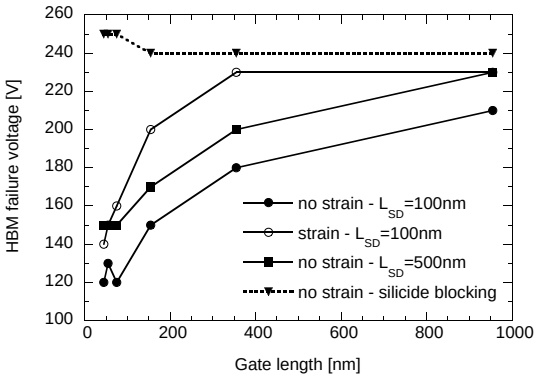

Figure 3.71: HBM-failure voltage as a function of gate length for N-type FinFETs in parasitic-bipolar mode. Silicide blocking and increased L_{SD} improve the ESD robustness.

L_{SD} (=500 nm) and/or employing silicide blocking. In both cases, no ringing is observed anymore and the devices fail to a short as was the case for the strained devices. Silicide blocking ensures the failure current uniformity over the entire device array regardless of L_g, while still some degree of non-uniformity exists in case of increased L_{SD} and in case of strain, seen by the dependence on L_g.

Gated FinFET diodes

Fig. 3.72 shows the HBM failure level as a function of L_g for strained and non-strained gated FinFET diodes, in which the ESD stress is applied to gate and anode while the cathode is kept grounded. Strain improves the HBM robustness up to 13 % and the trend is similar to the one observed for FinFETs stressed in active MOS-diode mode (Fig. 3.63). Similar to the latter, the increased ESD performance for strain is due to lower power dissipation because of higher electron mobility.

3.7 Gated Diodes - RF Considerations, Transient Analysis and Modeling

This section focusses deeper on various aspects of gated diodes. First, in section 3.7.1, gated diodes are discussed from an RF point of view as they commonly are used for protecting high speed digital IO's and RF circuits. Next, in section 3.7.2, voltage overshoots due to diode forward recovery are carefully characterized and included in an ESD diode compact model.

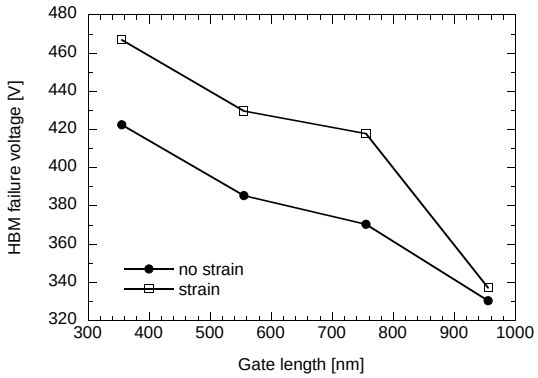

Figure 3.72: HBM-failure voltage as a function of gate length for gated FinFET diodes. Strain improves the ESD robustness up to 13% for short and medium gate lengths.

3.7.1 RF considerations

When the gated diode is used in high-speed or RF applications, also the parasitic capacitance is an important parameter. For these applications, area might be less of a concern and the question is whether the 2-3 times improved intrinsic ESD performance observed for narrow fin devices compared to wide fin devices (Fig. 3.40) results in an improved FOM for RF when considering capacitance as well. The FOM to be considered is It_2 per capacitance [mA/fF]. RF S-parameter measurements were performed on two available gated diodes in RF configuration. The first one consisted of 400 fins with a width of 20 nm and gate length of 80 nm, while the second one was a single wide (planar) fin device of same gate length and 80 μm width. The devices were processed with SEG (section 3.6.3) in IMECs 300 mm fab. The measured capacitances were 20 fF and 32.5 fF respectively after de-embedding of the metal interconnects resulting in a FOM of 11.5 mA/fF for the narrow fin device and 33.4 mA/fF for the wide fin (i.e. planar) diode. This means that when considering parasitic capacitance as an optimization goal, again the wide fin (planar) gated diode is the preferred option. The gate was left floating, yielding a lower capacitance than when connected to anode or cathode. To understand these results, formula (3.17) was derived:

$$C_{tot} = C_j N_{fin} W_{fin} H_{fin} + C_{oh} N_{fin} (W_{fin} + 2H_{fin}) \tag{3.17}$$

The total device capacitance C_{tot} is divided into two parts. One part equals the junction capacitance C_j from anode to cathode which is proportional to the junction cross-section $N_{fin} W_{fin} H_{fin}$. This part of the total capacitance is therefore directly proportional to the intrinsic ESD robustness of the diode. The second part C_{oh} represents the overhead capacitance proportional to the

total gate width $N_{fin}(W_{fin} + 2H_{fin})$ and consists of gate overlap and fringing capacitances between the fins and the (floating) gate [Wu 07].

(3.17) consists of two unknowns, namely C_j and C_{oh}, and they can be found by solving a set of equations for both the narrow and wide fin devices. The parasitic capacitance C_{narrow} was measured for a narrow fin device ($N_{fin} = N_{narrow}$ and $W_{fin} = W_{narrow}$). Similarly, the parasitic capacitance C_{pla} was measured on a single planar fin device $N_{fin} = 1$ and $W_{fin} = W_{pla}$). A solution for C_j and C_{oh} can be analytically derived as a function of the narrow and wide fin devices and is given in (3.18) and (3.19) respectively.

$$C_j[fF/\mu\mathrm{m}^2] = \frac{N_{narrow}(W_{narrow} + 2H_{fin})\frac{C_{pla}}{W_{pla}} - C_{narrow}}{2N_{narrow}H_{fin}^2} \tag{3.18}$$

$$C_{oh}[fF/\mu\mathrm{m}] = \frac{2H_{fin}C_{narrow} - (N_{narrow}(W_{narrow} + 2H_{fin})\frac{C_{pla}}{W_{pla}} - C_{narrow})W_{narrow}}{2N_{narrow}H_{fin}(W_{narrow} + 2H_{fin})} \tag{3.19}$$

For the narrow fin device, C_{oh} contributes almost 97 % of the total device capacitance due to the large fringing capacitances between the fins and gate sidewalls, while the 'useful' capacitance C_j is only 3 %. This ratio changes to 79 % of C_{oh} and 21 % of C_j for wide fin devices. The relative contribution of C_{oh} and C_j is illustrated in Fig. 3.73 as a function of W_{fin}.

It_2 and C_{tot}, both normalized towards intrinsic silicon width are shown in Fig. 3.74 as a function of fin width together with the derived FOM (It_2/C_{tot}). Symbols indicate measurement results while for intermediate fin width, the parasitic capacitance is calculated using (3.17). The large overhead capacitance of the narrow fin devices degrades the FOM with respect to the wide fin devices, making wide fin devices the preferred choice. Note that almost 20 % of C_{oh} can be attributed to the usage of SEG as described in [Parv 07]. When considering parasitic capacitance instead of minimal area consumption, again the optimal solution is a wide-fin diode and no trade-offs are currently present.

3.7.2 Transient analysis and compact modeling

As technology keeps scaling down, the core transistors become more and more vulnerable towards ESD stress. As a result, ESD researchers need to focus besides the quasi-static behavior also more and more on the dynamic response

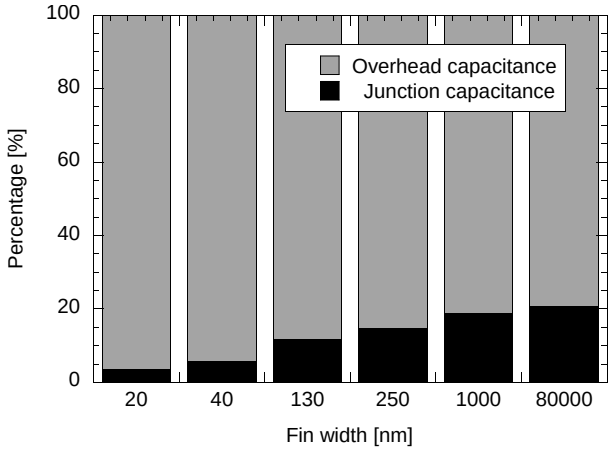

Figure 3.73: Contribution percentage of both overhead and junction capacitance as function of fin width, according to (3.17). Narrow fins have relative more overhead capacitance.

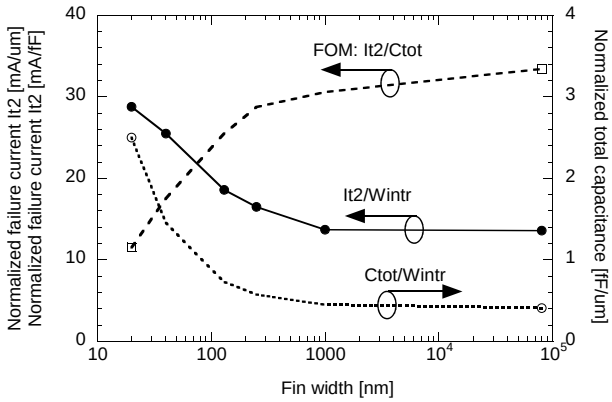

Figure 3.74: Normalized It_2 and parasitic capacitance per intrinsic silicon width as a function of fin width. The derived FOM (It_2/C_{tot}) is improving with increasing fin width. The symbols indicate measurement data points.

of the ESD protection device under ESD conditions as voltage overshoots can cause serious damage. For the presented gated FinFET diodes, 100 ns TLP measurements do not provide quasi-static device information anymore. In general, understanding the dynamic response requires the use of more extensive TLP investigations (such as longer pulse widths) or the use of on-wafer HBM measurements [Scho 07] [Scho 07b] as presented in this section. Together with voltage and current waveform capturing during the ESD stress, these measurements can provide the dynamic IV response of the protection device under real ESD stress.

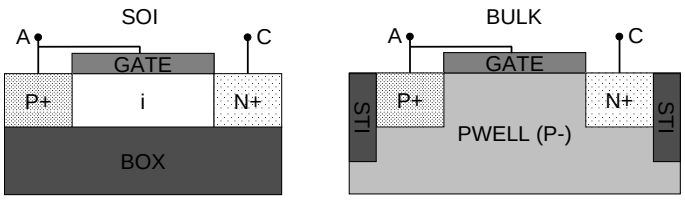

Figure 3.75: Cross-section of a gated-diode in (left) a FinFET CMOS technology, and (right) in a bulk CMOS technology.

During MM and CDM stress events, the voltage overshoots due to forward recovery (the time it takes the diode to conduct when switched from reverse to forward bias) will be much higher due to the faster rise times than during HBM. During these ESD stress types, also reverse recovery of the diode can be observed, e.g. in a dual-diode ESD solution with a power clamp. Reverse recovery occurs when a forward conducting diode is turned off rapidly and the internally stored charges in the intrinsic-region ('i' in Fig. 3.75) cause transient reverse current to flow at a high reverse voltage.

ESD diode compact models, available in the literature [Stoc 06] [Li 06], model only the TLP quasi-static IV curves. Until now, no transient ESD stress effects are considered in these models. This enhances the necessity of accurate transient ESD component models. In this subsection, gated diodes are characterized and modeled under real HBM ESD conditions. The presented model is a first step in accurate modeling transient effects (forward recovery in this work) during ESD stress events. The used knowledge/methodology can be extended towards a more complete diode model or towards modeling of other, more complex ESD protection devices.

Device Characterization

The gated-diodes are drawn as 'planar' like diodes with one very wide fin. This layout is compatible with bulk and FinFET technology. In bulk, it results in a gated-diode with STI at its anode and cathode sides, and a pwell doping below its gate, Fig. 3.75 (right), creating a P+/P-/N+ structure, while in FinFET technology, it results in a P+/i/N+ structure, see Fig. 3.75 (left).

On-wafer TLP and HBM measurements are performed on a 35 μm wide diode with a gate length of 110 nm, processed in both bulk and FinFET CMOS technology. The It_2 values are 1.2 A and 0.3 A during TLP and 1.5 kV and 500 V during HBM, respectively. This clearly illustrates the lower ESD robustness of FinFET diodes due to the limited thermal dissipation in the buried oxide.

TLP-IV with 2 ns rise time and HBM-IV of the bulk and FinFET diodes are overlapped in Fig. 3.76 and Fig. 3.77. The HBM-IV curve is realized by plotting

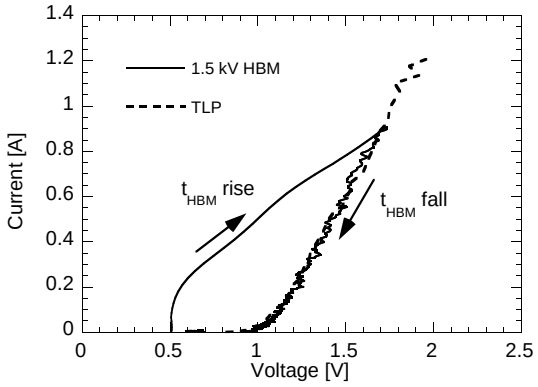

Figure 3.76: Measured TLP and 1.5 kV HBM-IV of a 35 μm wide bulk gated-diode, 110 nm gate length. The rising and falling part of the HBM-IV curve aree indicated.

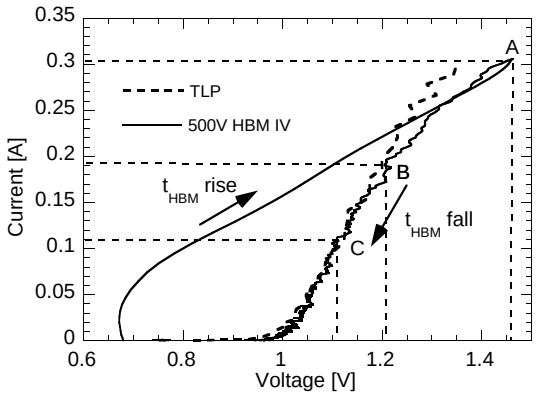

Figure 3.77: Measured TLP and 500 V HBM-IV of a 35 μm wide FinFET gated-diode, 110 nm gate length.

the aligned current in time over voltage in time according to section 2.5.3. From these IV curves, the same parameters as from TLP can be extracted (R_{on}, V_h).

For bulk diodes (Fig. 3.76) the 1.5 kV HBM-IV curve rises within 10 ns during the diode turn-on up to the peak HBM current, and then falls down overlapping the TLP-IV curve. The rising part is highly dependent on the filter in the calibration of the HBM system [Scho 07b] and is limited by the bandwidth of the voltage probe. This fast rising part of the HBM pulse is not considered in this work. The falling part, which is relatively slow in comparison to the rising part, is studied (Fig. 3.78).

The 500 V HBM-IV curves of the FinFET diode do not follow the TLP-IV in the initial falling part of the HBM IV curve (Fig. 3.77). The HBM-IV rises up

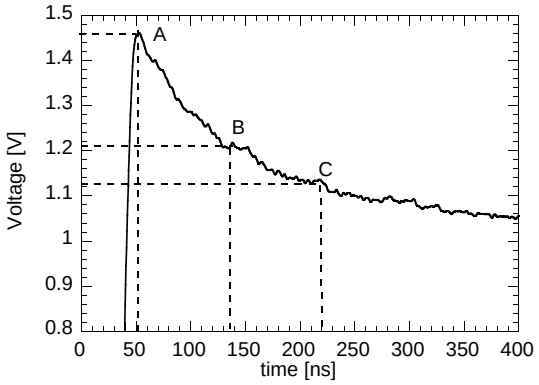

Figure 3.78: Measured voltage across a 35 μm wide FinFET gated-diode during a 500 V HBM stress event.

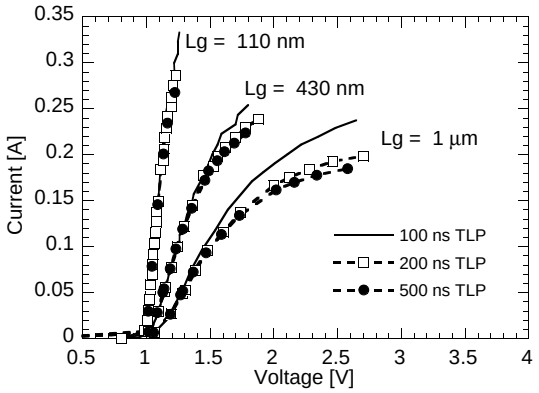

Figure 3.79: 100/200/500 ns TLP measurements of 35 μm wide FinFET gated-diodes with 110 nm, 430 nm and 1 μm gate length.

to the point of maximum ESD current and voltage (A) and falls down to the TLP-IV at point (B), from where the TLP-IV curve is followed for the rest of the HBM event.

Fig. 3.78 shows the measured 500 V HBM voltage across the diode. Points A, B and C from Fig. 3.77 are indicated. A voltage drop of 250 mV between (A) and (B) occurs over a time period of 80 ns. Another 70 ns later, point C in Fig. 3.77 and Fig. 3.78, only a voltage drop of 100 mV is seen.

This deviation from the linear regime at the top of the HBM-IV curve can be easily mistaken for self heating, as often observed in TLP-IV curves. However, the FinFET diode does not show self heating for small channel lengths during TLP, only at larger channel lengths. This is proven in Fig. 3.79, where 100, 200 and 500 ns TLP IV curves are plotted for diodes with a channel length of 110, 430 nm and 1 μm respectively.

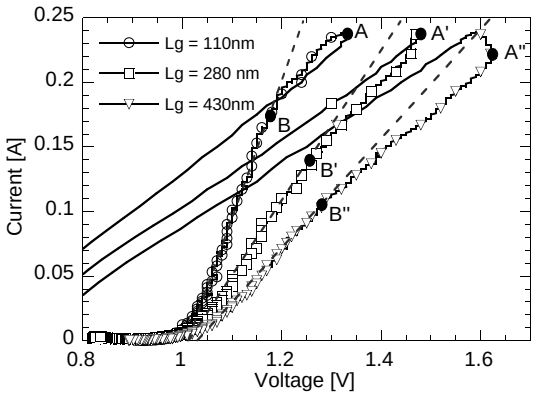

Figure 3.80: 400 V HBM-IV measurements on 35 μm wide FinFET gated-diodes with 110, 280 and 430 nm gate length: corresponding forward recovery times t_{fr} are 70, 120, and 167 ns respectively.

The bending during HBM (Fig. 3.77) is only present at the initial part of the voltage waveform of the diode. This relates to a transient effect, namely forward recovery of the FinFET gated-diodes during the HBM event. When the FinFET PIN diode switches rapidly from off-state to on-state, the carrier concentration in the base region (i-region in Fig. 3.75 (left)) will only increase gradually. This conductivity-modulation effect in the base-region will produce a large forward voltage V_m (point A in Fig. 3.77) [Howa 65] [Clif 93]. When the conductivity-modulation effect is over, after forward recovery time t_{fr} (80 ns in Fig. 3.77), V_m is returned to the normal diode forward voltage (point B in Fig. 3.77).

The amount of forward recovery is closely linked to the initial bulk resistance of the diode R_{mo}, and the rate of the current change (di/dt). The forward recovery time is linked mainly to the carrier lifetime and the thickness of the i-region (under the gate of the FinFET diode) [Yama 04]. Increased doping of the i-region will result in a lower R_{mo} and thus in a lower V_m. This explains why no forward recovery effect is observed in Fig. 3.76 for the bulk gated-diode. When increasing the gate length, also a higher R_{mo} and therefore a higher V_m, is obtained (Fig. 3.80). Also t_{fr} is increased with the gate length as it increases the transit time of the carriers [Yama 04]. In conclusion, for the gate diodes a minimal gate length is preferred. Besides the It_2 and R_{on} advantage, they also have the smallest forward recovery effect.

Fig. 3.81 plots the HBM-IV curve for 300 and 500 V HBM stress levels. The increased di/dt of the 500 V pulse results in a higher amplitude and longer duration of the overshoot. T_{fr} increases from 67 ns to 119 ns.

Forward recovery is actually also observed during TLP measurements with 2 ns rise time but in a less significant way than for HBM-IV measurement.

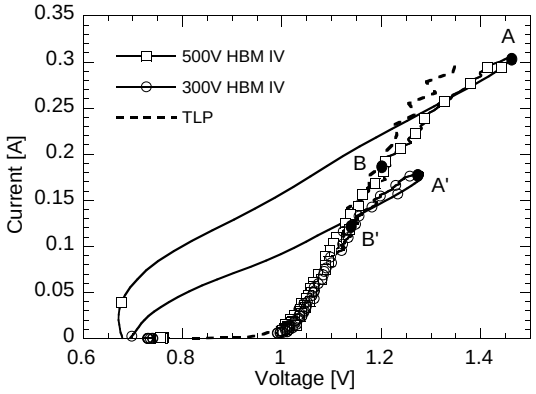

Figure 3.81: 300 and 500 V HBM-IV and TLP measurements on a 35 μm wide FinFET gated-diode, 110 nm gate length.

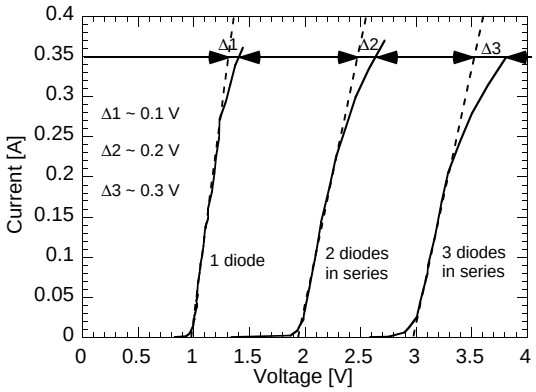

Figure 3.82: 100 ns TLP measurements on 2 and 3 35 μm wide FinFET gated-diodes with 110 nm gate length in series.

The TLP-IV curve for the 35 μm wide FinFET gated-diode with 110 nm gate length shows a slight bending at the top part of the curve (Fig. 3.82). This deviation is around 0.1 V (Δ1) at 0.35 A TLP current. It is not attributed to self-heating, as demonstrated in Fig. 3.79, but to forward recovery. In order to clearly visualize this bending in the TLP-IV curve, TLP measurements are performed on 2 and 3 diodes in series (Fig. 3.82). For 3 diodes in series, a total deviation of 0.3 V is measured at 0.35 A TLP (Δ3). This corresponds to three times Δ1. As forward recovery generates a voltage overshoot during a period of tens of nanoseconds (80 ns for this diode), it increases the averaged TLP voltage value taken between the 70 ns and 90 ns timeframe of the TLP pulse. The deviation Δ increases with increased TLP levels and this is consistent with the di/dt impact on the forward recovery behavior discussed during HBM stress.

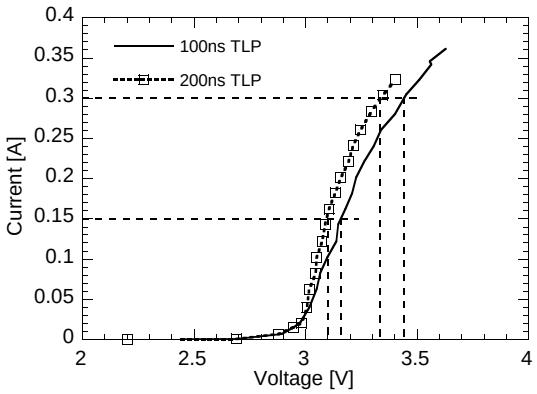

Figure 3.83: Comparison of 100 and 200 ns TLP-IV curve for 3 diodes in series. The diodes are 35 μm wide and have a gate length of 110 nm.

When comparing 100 ns and 200 ns TLP-IV for the 3 diodes in series (Fig. 3.83), it becomes clear that in the 100 ns TLP-IV curve, forward recovery is the cause for an increased voltage, starting even at very low current levels. Forward recovery causes thus in Fig. 3.82 not only a bending away from the straight line as indicated, but in fact a deviation over the full TLP IV curve. For Fig. 3.83, a measurement window of 70-90 % of the TLP pulse width is used.

To further substantiate this finding, voltage waveforms are compared for the 100 ns and 200 ns TLP measurements at two TLP current levels, namely 0.15 A and 0.3 A, as indicated in Fig. 3.83. The original voltage waveforms are shown in Fig. 3.84, where the left figure shows the full TLP voltage waveform and the right a zoomed view. As expected, the 100 ns and 200 ns waveforms are exactly the same for the beginning part, but as can be seen in the right figure, the voltage for both current levels keeps on decreasing further in the 200 ns waveforms. This proves that also for low current levels, forward recovery of the diode is not completed during 100 ns TLP pulses, and therefore 100 ns TLP measurements are not giving quasi-static measurements for such FinFET gated-diodes.

Note that the difference between self-heating and forward recovery causing the bending in IV curves, can easily be seen in Fig. 3.83 and Fig. 3.84. In Fig. 3.83, in case of self-heating, the 200 ns TLP curve would lie to the right of the 100 ns TLP curve, where here it lies to the left. In Fig. 3.84, due to forward recovery the voltage decreases over time, whereas for self-heating it would increase.

Compact modeling

In order to simulate the ESD performance of on-chip protection networks based on such diodes, the diodes need to be modeled in the high current ESD regime

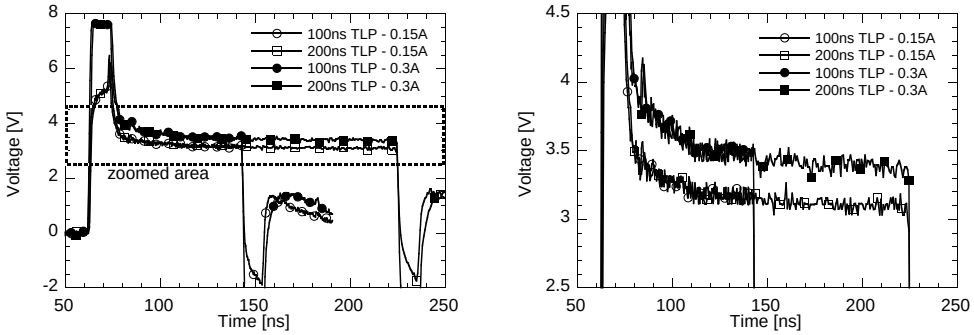

Figure 3.84: Transient voltage waveforms taken from 0.15 A and 0.3 A TLP pulses for both 100 ns and 200 ns TLP measurements. Full voltage waveforms are shown on the left and the indicated rectangle is zoomed to in the right figure. It is clear that the forward recovery effect is not completed after 100 ns, as the voltage keeps on decreasing during the 200 ns TLP waveforms.

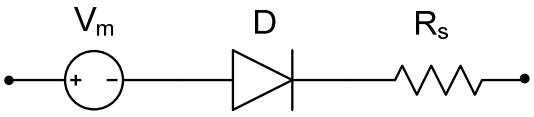

Figure 3.85: Proposed diode model valid in HBM ESD time domain.

and need to take transient effects such as forward recovery into account. In order to facilitate the portability between different simulators [Li 06], Verilog-A is used to implement a behavioral model.

An extension of an existing ESD diode model [Stoc 06] is proposed, were a voltage source V_m is added in series with a diode current model D and the high current on-resistance R_s (Fig. 3.85).

Components D and R_s describe the standard TLP-IV curves and can be implemented as in [Stoc 06] [Li 06]. V_m is depending on the dynamics of the applied ESD current. Therefore, the recombination current I_m and charge in the base region (I-region) q_m, are modeled as a function of time by solving the diffusion current equations:

$$I_m(t) = \frac{q_e(t) - q_m(t)}{T_m} = \frac{\delta q_m(t)}{\delta t} + \frac{q_m(t)}{\tau}, \tag{3.20}$$

$$q_e(t) = \tau I_s(e^{\frac{V_j(t)}{2V_t}} - 1), \tag{3.21}$$

where τ represents the carrier lifetime, T_m the transit time, I_s the diffusion leakage current, V_t the thermal voltage, V_j the junction voltage and q_e the

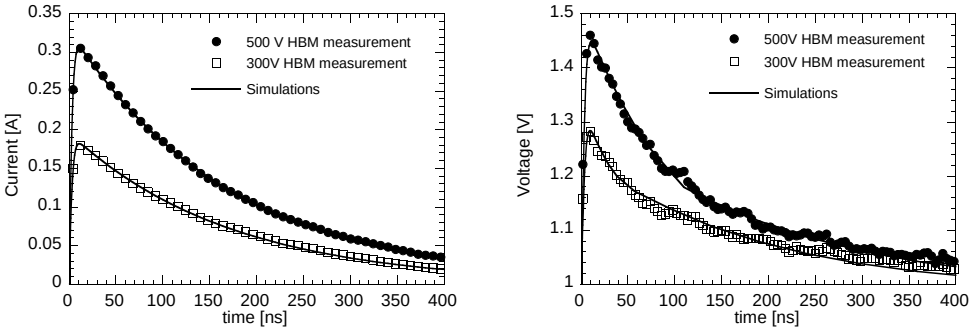

Figure 3.86: Measured and simulated current (left) and voltage (right) across a 35 μm wide FinFET gated-diode, 110 nm gate length, during a 300 V and 500 V on-wafer HBM stress (τ=68.6 ns, R_{mo}=49 Ω, T_m=5 ns, β=1e-4 Vs and R_s=0.89 Ω).

injected charge due to diffusion current from the P+-i junction. For forward recovery ($dq_m/dt >= 0$) the voltage V_m is calculated as [Bata 94]:

$$V_m(t) = \frac{R_{mo}\beta I_d^2(t)}{\tau R_{mo} I_m^2(t) + \beta I_d(t)} - \frac{R_{mo}\beta I_d(t)}{R_{mo}\tau(1+\frac{T_m}{\tau})^2 I_d(t) + \beta}, \tag{3.22}$$

where R_{mo} is the initial resistance in the mid-region, β a geometrical and physical dependent parameter of the diode, and I_d the sum of I_m and the displacement current in the diode.

In order to enable model parameter extraction and model validation for HBM transients, a fourth-order lumped element model [Verh 93] is extracted for the on-wafer HBM tester, which is valid for different HBM pre-charge voltages (Fig. 3.86, left). This HBM model is used in the extraction of the diode model parameters.

A least-square optimization routine is used for parameter extraction. A cost function K:

$$K = \sum_{k}^{precharges} [V_{HBM,k}^{meas} - V_{HBM,k}^{sim}(\tau, T_m, R_{mo}, \beta)]^2 \Big|_{I_{HBM,k}^{meas}=I_{HBM,k}^{sim}} \tag{3.23}$$

is minimized for the parameters τ, T_m, R_{mo}, and β where $V_{HBM,k}^{meas}$, $I_{HBM,k}^{meas}$, $V_{HBM,k}^{sim}$, $I_{HBM,k}^{sim}$ are the measured and simulated HBM current and voltage waveforms for precharge number k.

Fig. 3.86 shows the simulated and measured HBM voltages and currents for a 300 and 500 V HBM stress. Fig. 3.87 shows the resulting measured and

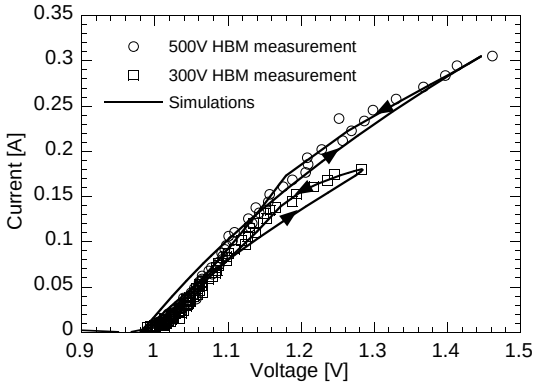

Figure 3.87: Measured and simulated 300 V and 500 V HBM-IV on a 35 μm wide FinFET gated-diode, 110 nm gate length.

simulated HBM-IV curve of the FinFET diodes. An excellent agreement is observed. The same model can be used for HBM transient modeling of bulk diodes. The model can be extended towards a compact scalable diode model.

3.8 Design Methodology

In section 3.4 and section 3.6, the different ESD-device parameters (failure current It_2, holding voltage V_h, on-resistance R_{on}, leakage current and area consumption) of a grounded gate NMOS FinFET device were investigated as a function of device geometry and process parameters respectively. For N-type FinFETs a comparison was presented between standard grounded-gate configuration and MOS-diode mode where the gate is tied to the drain.

Some process features such as strain, SEG, etc. are imposed by the technology, while some process options can be chosen specifically for the ESD protection devices such as silicide blocking, channel implants, etc. Besides such process options, the ESD design engineer can choose the layout parameters to find an optimal ESD layout and design.

A design methodology is needed because the more complex geometry of FinFET devices introduces a higher degree of complexity that makes optimization absolutely not obvious as compared to planar devices.

Such design methodology for FinFET devices is presented in this section. It takes into account all complex dependencies on both layout and process parameters of the electrical ESD device parameters of NMOS FinFET devices in both parasitic bipolar and active MOS operation mode in section 3.8.1 and section 3.8.2 respectively. In general, this methodology allows optimization towards a given ESD target (ESD level, area consumption, leakage current,

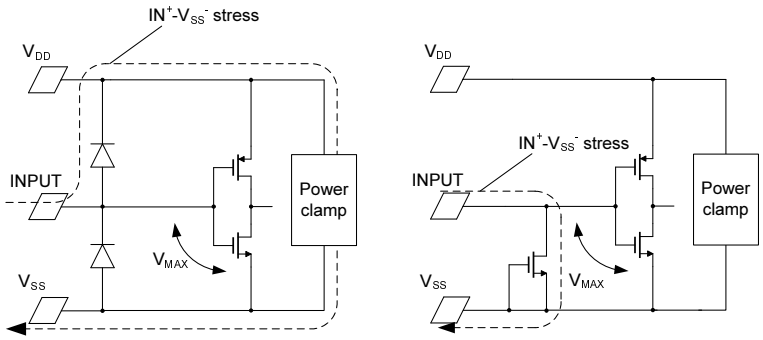

Figure 3.88: Dual diode ESD protection (left) versus local clamping (right). The arrows indicate the current flow during positive ESD stress between input and ground.

parasitic capacitance,) while fulfilling several imposed design constraints. A specific example applying the design methodology is used to find the minimum-area solution of a MOS clamp operating either in bipolar or in active MOS mode. In both cases it is required to sustain a certain HBM ESD stress V_{HBM}, while meeting a given leakage specification and without exceeding a certain maximum voltage V_{max}.

ESD current capability is not the limiting factor for FinFET ESD design as It_2 scaling with silicon width was demonstrated in section 3.4.1.3 leading to an HBM robustness up to 3.5 kV and more. On the other hand, voltage clamping capability seems more of a concern due to the reduced oxide breakdown voltage as illustrated in Fig. 1.8. This makes traditional dual-diode solutions obsolete due to too large voltage drops as illustrated in Fig. 3.88 (left) and as predicted by [Bose 05]. Other concepts, such as local clamping improve the ESD design window. Since grounded gate NMOS FinFET devices have their Vt_1 equal to V_h, they are a suitable candidate for such local clamping as shown in Fig. 3.88 (right). In this case, the maximum allowed V_{max} in the design methodology can be set to the gate oxide breakdown voltage BV_{ox}.

In the third subsection, a trajectory is created in the L_g-W_{fin} design space when the optimization constraint V_{max} is varied. Interpretation of these results enables a deeper insight into the different design and device trade-offs.

Finally, a new type of active MOS clamp is presented in section 3.8.4 which can operate in both polarities.

3.8.1 MOS devices - parasitic bipolar mode

The impact of W_{fin} and L_g on the different ESD device parameters for the NMOS devices in bipolar mode are summarized in Table 3.3. A "+" indicates

Table 3.3: Summary of different device parameters as a function of layout parameters L_g and W_{fin} for grounded gate NMOS devices in bipolar mode."+" is beneficial for ESD protection design, whereas "-" is detrimental.

	Short gate length	**Long gate length**
Narrow fin	+ low V_h + low R_{on} + low leakage + high It_2/W_{intr} - low It_2/W_{layout}	medium V_h medium R_{on} + low leakage + high It_2/W_{intr} - low It_2/W_{layout}
Wide fin	+ low V_h medium R_{on} - high leakage medium It_2/W_{intr} medium It_2/W_{layout}	- high V_h - high R_{on} + low leakage medium It_2/W_{intr} medium It_2/W_{layout}

behavior beneficial for ESD protection design, whereas "-" indicates a detrimental effect. Two different normalizations are used for It_2 as in section 3.3. The intrinsic silicon width W_{intr} does not include the fin-to-fin spacing (parameter S in Fig. 3.3), whereas the total layout width W_{layout} does.

A schematic block diagram of the methodology is shown in Fig. 3.89 where the different steps are summarized and explained in the following.

Design methodology - step 1

As a first step, based on available measurement data (L_g and W_{fin} variations) It_2, V_h and R_{on} are calculated over the full L_g-W_{fin} design space using a triangle-based interpolation method. The extraction of these parameters is illustrated for the bipolar mode already presented in Fig. 3.4. This allows estimating It_2, V_h and R_{on} values for any given virtual L_g-W_{fin} point. Fig. 3.90 shows a contour plot of It_2, normalized per intrinsic silicon width, over the L_g-W_{fin} design space. At large W_{fin}, It_2 saturates around 2 mA/μm. Contour plots of V_h and R_{on} normalized per intrinsic silicon width W_{intr} are shown in Fig. 3.91 and Fig. 3.92 based on the data in section 3.4.1.

Design methodology - step 2

Secondly, a set of devices is selected (specific W_{fin}-L_g combinations) which meets the leakage specification. Leakage qualification is done based on an empirical formula used within IMEC for Short Channel Control (SCC):

$$SCC = \frac{L_g}{min(W_{fin}, 2H_{fin}) + 6EOT} \tag{3.24}$$

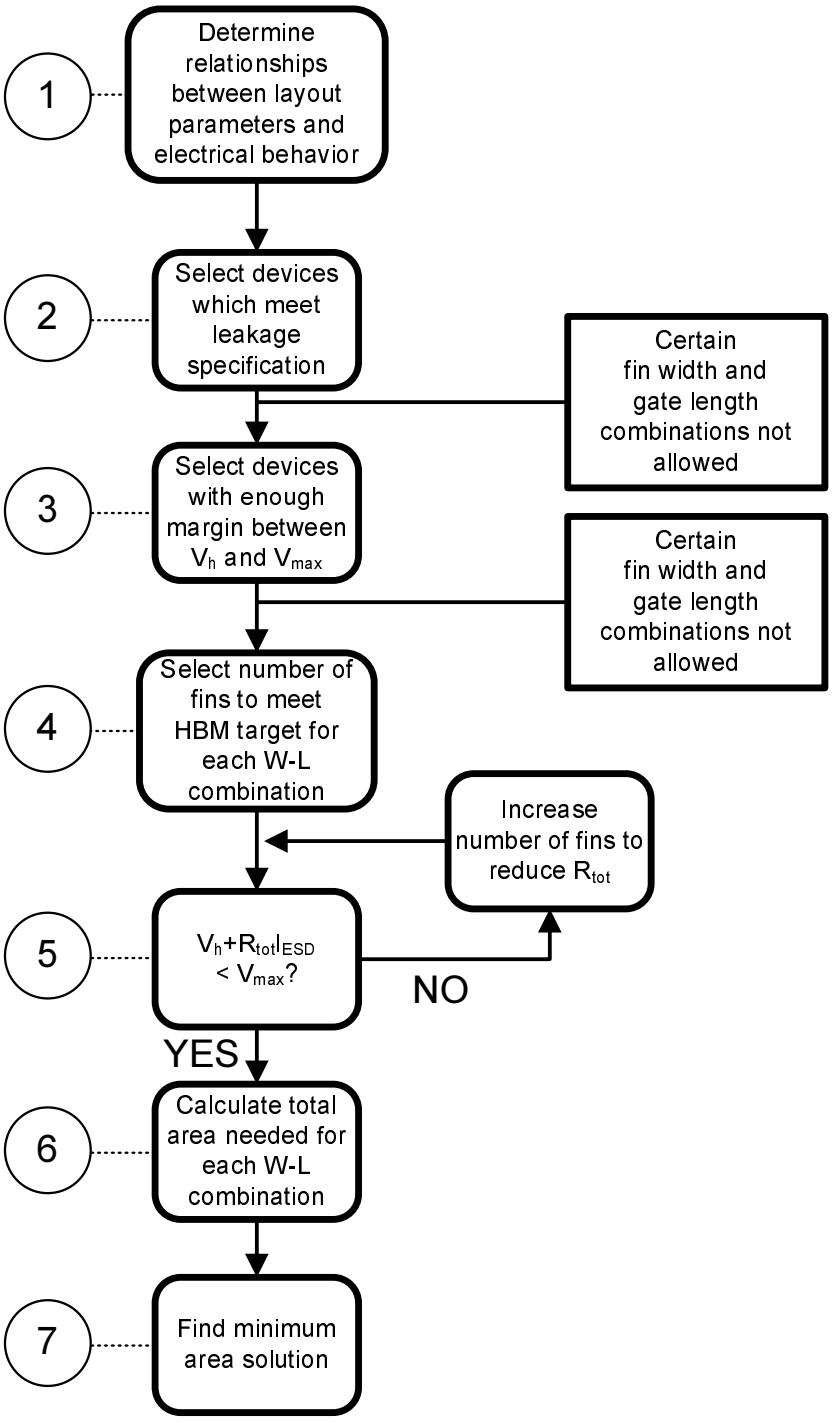

Figure 3.89: Block diagram showing the different steps of the design methodology for the specific example used.

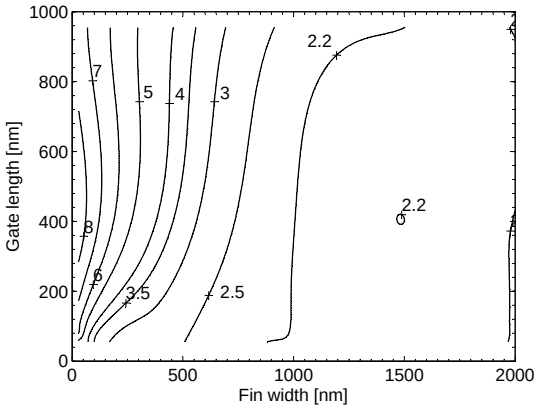

Figure 3.90: Contour plot of normalized failure current It_2 in bipolar mode per intrinsic silicon width [mA/μm] as a function of gate length and fin width.

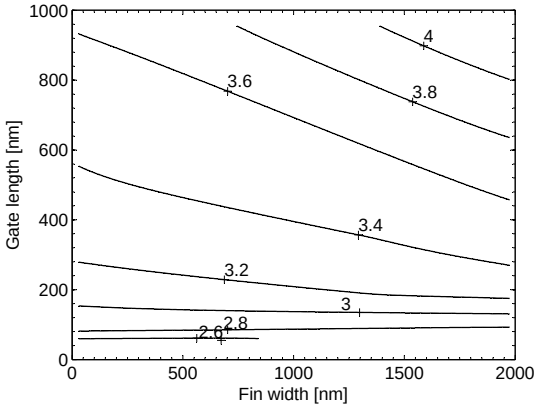

Figure 3.91: Holding voltage V_h [V] contours in bipolar mode as a function of gate length and fin width.

where SCC is calculated as a function of L_g, W_{fin} and Equivalent Oxide Thickness (EOT). SCC>1.4 is considered as a safe device, 1.4≥SCC≥1 has still good short channel control, while devices with SCC<1 suffer from strong SCE. This formula provides an easy way to take into account the leakage behavior of a device with certain L_g and W_{fin}. This formula was preferred over actual measurement data because a lot of variation in leakage current was measured due to the presence of parasitic Schottky contacts [Hoff 05]. These Schottky contacts are a result of over-silicidation of the drain to body junction and are present because the process was still under development. Devices with too high initial leakage would consequently have a low ESD robustness, and hence are not considered. By adding SEG, the problem of over-silicidation is greatly reduced [Coll 08] and less spread on the results was measured. The results of formula (3.24) are overlaid with the logarithmic of the leakage current [A/μm]

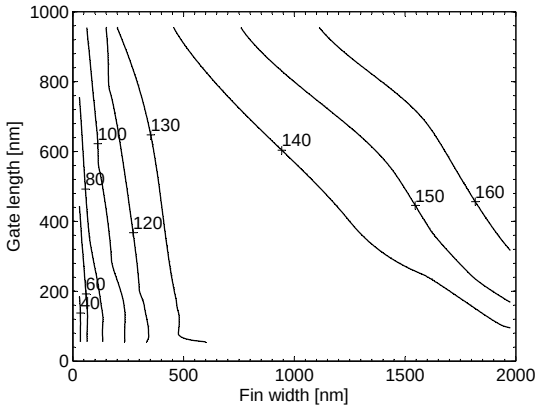

Figure 3.92: Normalized on-resistance R_{on} contours in bipolar operation mode per intrinsic silicon width [$\Omega\mu$m] as a function of gate length and fin width

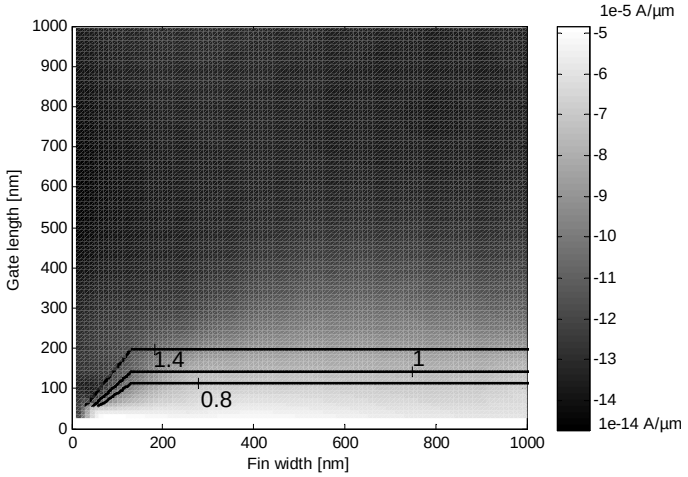

Figure 3.93: Logarithmic of measured leakage current [A/μm] normalized towards total channel width W_{chan} for the Short Channel Control (SCC) and overlaid with formula (3.24) (solid lines) to show its validity.

measured on a wafer with SEG, normalized to total channel width W_{chan} in Fig. 3.93. A clear correlation can be observed, demonstrating the validity of the formula.

Design methodology - step 3

For pratical reasons, only devices with enough margin between V_h and V_{max} are selected, otherwise way too large device size would be obtained due to the too limited R_{on} margin.

Design methodology - step 4

Next, for each L_g-W_{fin} point, the number of fins N needed to meet a given ESD robustness specification is calculated using the normalized It_2 graph, Fig. 3.90.

Design methodology - step 5

In a fifth step, the voltage drop V_{drop} over the device during maximum ESD current is calculated using:

$$V_{drop} = V_h + I_{ESD} R_{tot} < V_{max} \tag{3.25}$$

$$R_{tot} = \frac{R_{on}}{NW_{fin}} \tag{3.26}$$

where R_{tot} represents the total resistance of the device. V_{drop} has to remain below the maximum allowed voltage in the application V_{max} and the number of fins N can be increased to reduce R_{tot} when necessary. In a similar fashion, the trigger speed of the protection device can be included in the optimization as well, by imposing a second limit for the maximum transient voltage overshoot.

Design methodology - step 6

In a sixth step, the total necessary device area is then calculated as:

$$area = (NW_{fin} + (N-1)S + 2W_{ext})(L_g + 2L_{SD} + 2L_{cont}) \tag{3.27}$$

Design methodology - step 7

Finally, the lowest-area device in the design space is selected as the optimum solution for the given constraints.

As an example, this design methodology can be used to determine the minimum area solution for a grounded gate NMOS device used as local clamping as in Fig. 3.88 (right). The ggNMOS needs to have an ESD capability of 1 kV HBM, V_{max} of 4 V during ESD which is the oxide breakdown voltage and low leakage current (i.e. SCC>1.4). The required area is calculated using (3.27) for each point in the L_g-W_{fin} design space taking into account the correlation factor of 1.5 kV/A between HBM and TLP. The optimal solution is the point in the L_g-W_{fin} design space with the smallest required area.

Fig. 3.94 shows the optimal solution point at 395 nm L_g and 200 nm W_{fin} (dot) corresponding to a consumed area of 296 μm^2. It also shows the percentage of area increase for the full L_g-W_{fin} design space compared to this optimal solution. It is clear that any L_g or W_{fin} deviation from the optimum leads to a certain increase in the required area. No solutions exist for small L_g because of

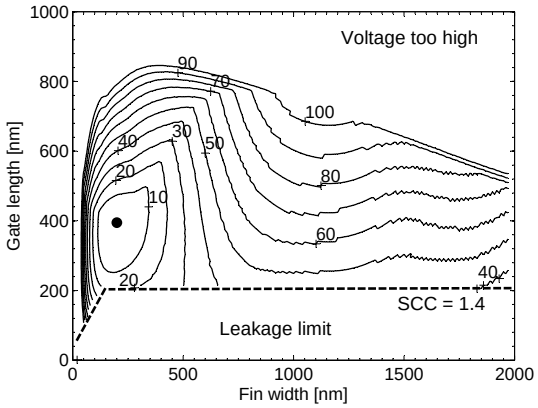

Figure 3.94: Percentage of increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 4 V V_{max} and excellent short-channel control (SCC>1.4) in bipolar mode.

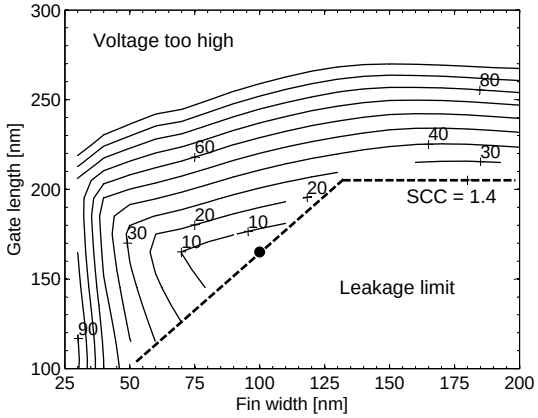

Figure 3.95: Percentage of increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 3.4 V V_{max} and excellent short-channel control (SCC>1.4) in bipolar mode.

the leakage current limitation and for large L_g because of too high maximum voltage drop.

When the maximum allowed voltage for example is decreased from 4 V to 3.4 V, the optimum solution shifts to lower L_g (165 nm) because of a lower required V_h. As a consequence, also W_{fin} (100 nm) has to be reduced for SCC, as can be seen in Fig. 3.95. This solution is limited by the leakage current limit and results in an increased area consumption of 40 %, namely 417 μm^2.

Also, folding of the transistor by sharing source and drain areas could be implemented to reduce the overall area. Even though the required area for

Table 3.4: Summary of different device parameters as a function of layout parameters L_g and W_{fin} for grounded gate NMOS devices in MOS diode mode."+" is beneficial for ESD protection design, whereas "-" is detrimental.

	Short gate length	**Long gate length**
Narrow fin	medium R_{on} + low leakage + high It_2/W_{intr} - low It_2/W_{layout}	- high R_{on} + low leakage medium It_2/W_{intr} - low It_2/W_{layout}
Wide fin	medium R_{on} - high leakage medium It_2/W_{intr} medium It_2/W_{layout}	- high R_{on} + low leakage - low It_2/W_{intr} - low It_2/W_{layout}

a given intrinsic silicon width is reduced by folding, It_2 and R_{on} may be impacted by constraints in the metal wiring and/or accumulative heating of folded structures. As such, the folding factor would become an additional layout parameter which can be easily included in the design methodology.

3.8.2 MOS devices - active MOS diode mode

The different dependencies of It_2 on L_g and W_{fin} in MOS diode mode were described in section 3.4.2. Table 3.4 summarizes the different dependencies. Based on these measurement results, the contour plot of It_2 normalized per intrinsic silicon width W_{intr} can be created as shown in Fig. 3.96. Some strange bumps can be introduced due to the linear interpolation routine and the limited set of data points and are an artifact of the method. MOS current starts to flow at about 0.5 V for narrow-fin devices and this threshold voltage is largely independent of L_g as seen from Fig. 3.35. This value can be considered as an equivalent TLP-V_T. On the contrary, for wide fin devices this V_T decreases with short gate lengths, thus these devices have poor control of SCE and hence cannot be used. R_{on}-extraction in diode mode is more difficult than in bipolar mode due to the non-linear current behavior as described in section 3.4.2. For the presented methodology, a non-physical linear R_{on} was extracted between the TLP-V_T and Vt_2 to obtain correct Vt_2-values at It_2 current level, as illustrated in Fig. 3.97 on the left. A more complex function may be implemented as well.

In order to study active clamp MOSFETs, the TLP IV-curves of Fig. 3.35 could be limited up to the point of onset of self-heating, where R_{on} starts to increase. This then yields a new It_2-value and corresponding linear extracted

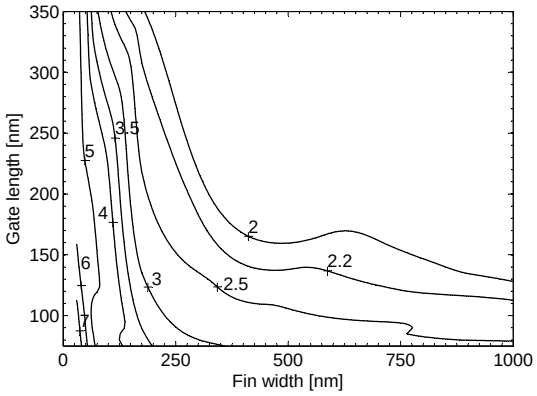

Figure 3.96: Contour plot of normalized failure current It_2 in MOS diode mode per intrinsic silicon width [mA/μm] as a function of gate length and fin width.

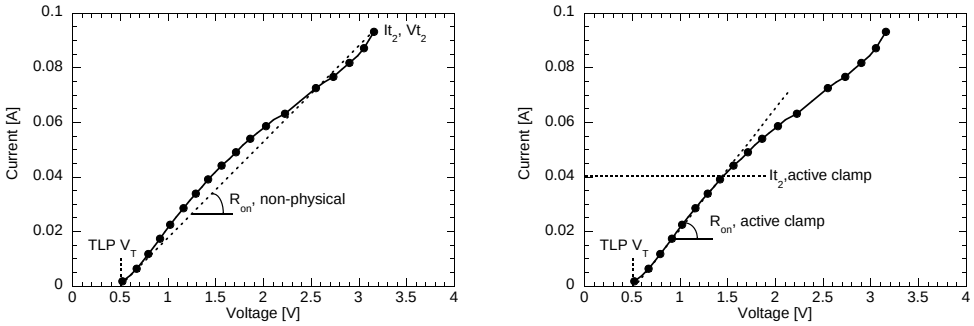

Figure 3.97: Definition of linear extracted R_{on} in case of devices in active MOS diode mode (left) and for active clamp devices (right).

R_{on} to be used in the methodology, as shown in Fig. 3.97 on the right.

Using the non-physical R_{on} as described in Fig. 3.97 (left), the design methodology can be used to optimize towards area in a similar fashion as for the bipolar mode. From these results, one might intuitively but wrongly think, based on Fig. 3.36 and Fig. 3.37, that the best device in MOS diode mode is a wide fin transistor with a minimum gate length which just fulfills the leakage requirements of (3.24). Using constraints of 1 kV HBM, 4 V V_{max} and SCC>1.4, it can be calculated that this device would have 200 nm L_g and would use 578 μm^2. However, when applying the methodology, the optimal solution turns out to be a device with N=1582 fins of 90 nm W_{fin} and 145 nm L_g as can be seen in Fig. 3.98. It uses an area of only 470 μm^2, which is roughly a 20% reduction compared to the intuitive solution. This 20% reduction can be explained by the fact that because of the increased gate length needed for SCC on wide fin devices, It_2 drops down rapidly (Fig. 3.36) and hence devices with narrower fins and consequently smaller gate length can become more area

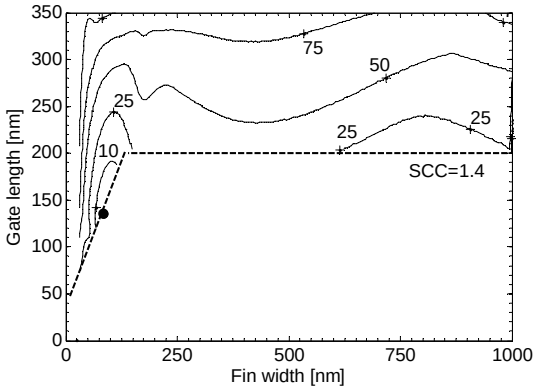

Figure 3.98: Percentage of increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 4 V V_{max} and excellent short-channel control (SCC>1.4) in MOS-diode mode.

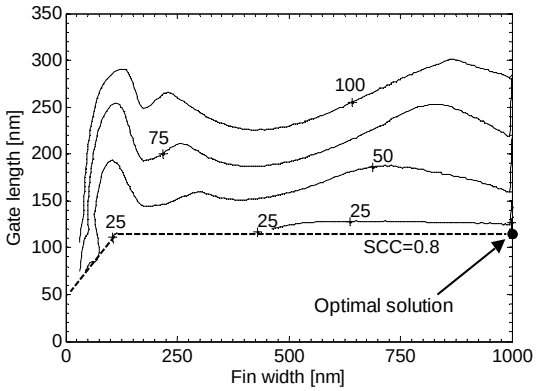

Figure 3.99: Percentage of increased area over optimal solution (dot) which meets imposed design constraints of 1 kV HBM, 4 V V_{max} and excellent short-channel control (SCC=0.8) in MOS-diode mode.

efficient. When this leakage constraint is removed (e.g. SCC=0.8) the optimal solution found is indeed as was first predicted, Fig. 3.99. Even though the solution found in Fig. 3.98 might appear numerically unstable as any deviation in process and device parameters might lead to specifications not being met by the proposed optimal solution, the impact of such deviations should be taken into account by including an appropriate safety margins, such as for V_{max}.

When comparing the results of the MOS diode with the bipolar operation mode, the MOS diode seems to be less sensitive to a deviation from the optimal W_{fin} and L_g. However, the overall performance of the MOS diode is not superior to the bipolar mode, which is generally the case in bulk technology. This can be attributed to the relatively high R_{on} as seen in Fig. 3.35, which can be

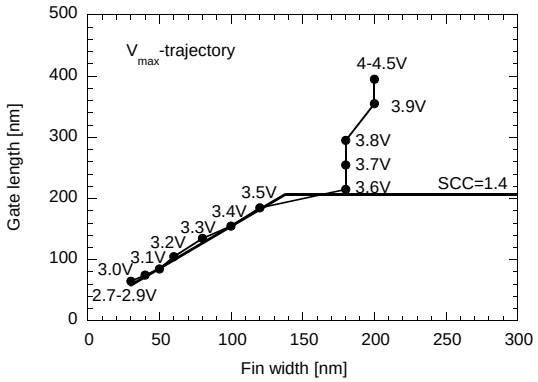

Figure 3.100: V_{max}-trajectory for the optimal solution in W_{fin}-L_g design space for V_{max} ranging from 4.5 V down to 2.7 V.

explained by the absence of a P+-body contact in SOI technologies. As such, a connection to the bulk-drain diode is absent and only MOS current conduction is present. In fact, when considering the example used above, the MOS diode mode requires an area increase of 58% over the bipolar mode to reach the same ESD target specifications. This has an important consequence, namely that in some cases the MOS diode mode would become the limiting factor (negative polarity ESD stress) when compared to the bipolar mode (positive polarity ESD stress). In practice, this would mean that in a full ESD protection circuit a separate reverse gated diode, section 3.4.3, would be preferred in conjunction with the MOS in bipolar mode.

3.8.3 Optimization constraint trajectory

In this section, the impact of the maximum allowed voltage V_{max} on the optimal values for L_g and W_{fin} is studied in greater detail. On one hand, such exercise allows to investigate the sensitivity of correct V_{max} determination (based on the ESD design window) on the optimal layout parameters, and secondly it enables deeper understanding of the different effects which come into play when V_{max} decreases.

In section 3.8.1, the minimum area solution was found for a ggnMOS device operating in bipolar mode, with an HBM target of 1 kV and low leakage requirements (SCC>1.4) for two V_{max} values, namely 4 V and 3.4 V. This exercise extends the V_{max} range from 4.5 V down to 2.7 V. In the W_{fin}-L_g design space, a V_{max}-trajectory for the optimal solution can be created as shown in Fig. 3.100.

Deeper understanding is obtained based on five different graphs as function of V_{max}.

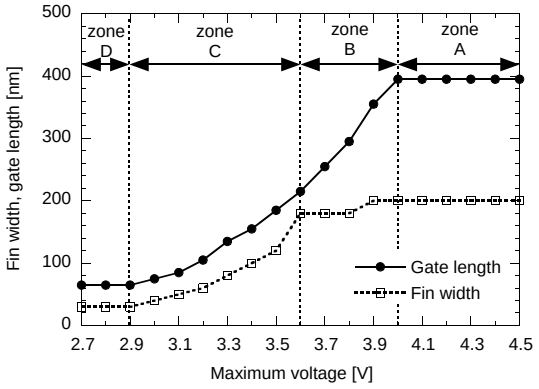

Figure 3.101: Dependence of optimal L_g and W_{fin} as function of V_{max}.

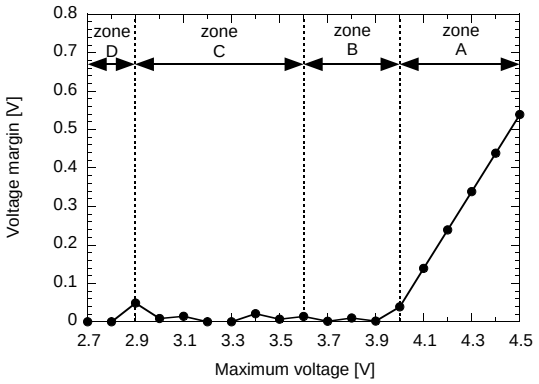

Figure 3.102: Remaining voltage margin between voltage drop over optimal solution and V_{max} as function of V_{max}.

1. Dependence of optimal L_g and W_{fin} as function of V_{max} (Fig. 3.101)
2. Remaining voltage margin between voltage drop for optimal solution and V_{max} as function of V_{max} (Fig. 3.102)
3. Maximum current capability of optimal solution as function of V_{max} (Fig. 3.103)
4. Area consumption of optimal solution as function of V_{max} (Fig. 3.104)
5. Short Channel Control (SCC) of optimal solution as function of V_{max} (Fig. 3.105)

According to Fig. 3.101-Fig. 3.105, four different zones can be distinguished (Zone A-Zone D). Each zone is discussed in detail below based on these corresponding five graphs.

Zone A (4 V< V_{max} <4.5 V)

1. When decreasing V_{max} from 4.5 V to 4 V, no change in L_g and W_{fin} is needed. This optimal L_g-W_{fin} point was found using the design

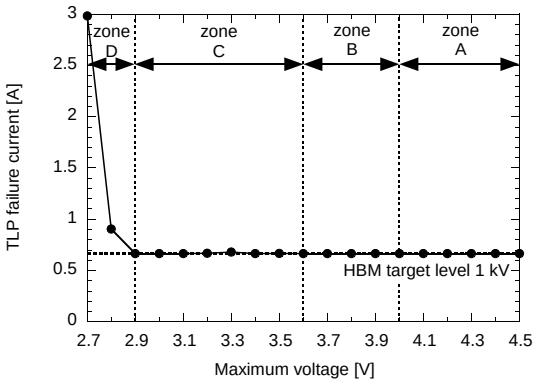

Figure 3.103: Maximum current capability of optimal solution as function of V_{max}.

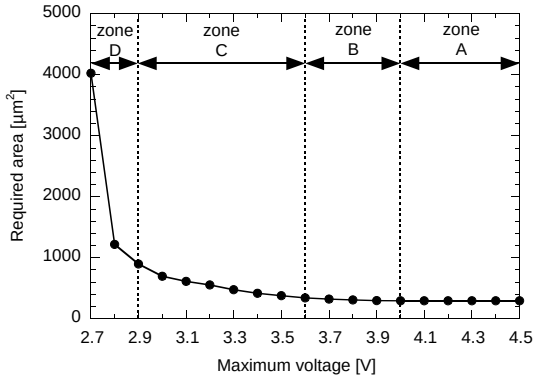

Figure 3.104: Area consumption of optimal solution as function of V_{max}.

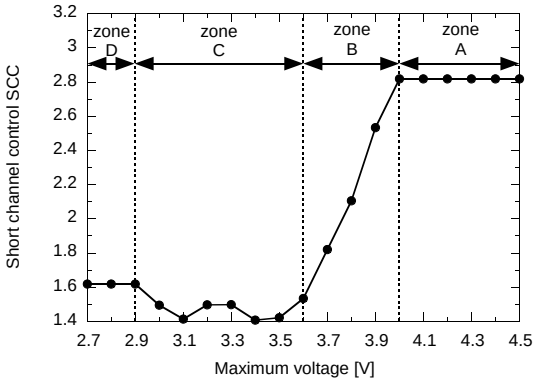

Figure 3.105: Short Channel Control (SCC) as function of V_{max}.

methodology as shown in Fig. 3.94 and takes all the different dependencies into account.
2. This can be attributed to the fact that there is still margin left between the voltage drop over the optimal solution during ESD and V_{max}.
3. This optimal solution is limited by the minimum required ESD current (using correlation factor of 1.5 between TLP and HBM).
4. Since L_g and W_{fin} are not changing, the required area is independent of V_{max}.
5. The solution is not limited by SCE, as SCC>1.4.

Zone B (3.6 V< V_{max} <4 V)

1. When decreasing V_{max} from 4 V to 3.6 V, W_{fin} stays constant, while L_g needs to decrease.
2. There is no voltage margin anymore, indicating that this solution is limited by maximum voltage. This means that with reducing V_{max}, also L_g needs to be reduced to lower V_h, see Fig. 3.91.
3. The solution is limited by minimum required ESD current.
4. The slight increase in area can be attributed to the decreasing L_g, which causes a reduction of It_2 and therefore a larger number of fins is needed, see Fig. 3.90.
5. The solution is not limited by SCE, meaning that for decreasing L_g, W_{fin} can remain constant.

Zone C (2.9 V< V_{max} <3.6 V)

1. Both W_{fin} and L_g need to decrease when V_{max} decreases from 3.6 V to 2.9 V.
2. The solution is limited by maximum voltage requiring reduced L_g for decreasing V_{max} as in Zone B.
3. The solution is limited by minimum required ESD current.
4. Area consumption increases more and more since W_{fin} is decreasing also, next to L_g as in Zone B. This leads to less area efficiency by increased overhead due to fin-to-fin spacing.
5. Additionaly over Zone B, as SCC=1.4, this solution is limited by SCE, as can also be seen from Fig. 3.100. This requires a decrease in W_{fin} for decreasing L_g. (The deviation of SCC=1.4 is due to quantized values for L_g and W_{fin}, with a 5 nm resolution.)

Zone D (2.7 V< V_{max} <2.9 V)

1. L_g and W_{fin} stay constant when V_{max} decreases from 2.9 V to 2.7 V since the minimum fin width of 30 nm is reached.
2. The solution is limited by maximum voltage.

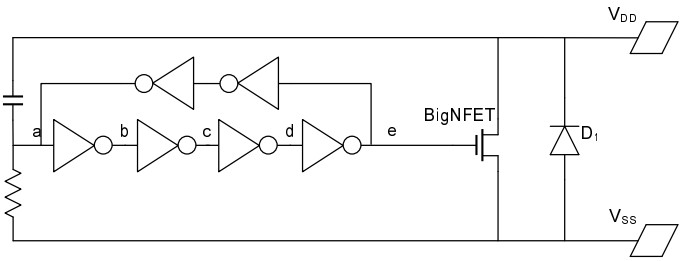

Figure 3.106: Schematic of RC-triggered power clamp. The addition of inverters and feedback relaxes the constraint on the RC-network.

3. As the maximum voltage specification comes too close to the minimum possible V_h, the number of fins needs to be increased to reduce R_{tot}. To meet the 2.7 V V_{max} criterium, the optimal solution could take 3 A TLP, which means that the device was upscaled five times due to the extremely tight voltage specification.
4. The increased number of fins leads to an exponentially increased area consumption.
5. SCC is slightly larger than 1.4 due to quantized values for L_g and W_{fin}.

In summary, in Zone A, both L_g and W_{fin} can remain constant when V_{max} is decreasing since the solution is not limited by V_{max}. In Zone B, V_{max} becomes limiting, pushing L_g down to reduce V_h. W_{fin} does not need to be reduced since the solution is not limited by SCE. Going to Zone C, when L_g decreases further, also W_{fin} needs to be reduced due to leakage restrictions. Finally, in Zone D, the voltage specification becomes so hard that L_g cannot be reduced further because the minimum fin width is reached and hence leakage requirements determine L_g. The only way V_{max} can be met is by reducing R_{tot}, instead of V_h, by increasing the number of fins.

No solution obviously exists for voltage clamping below 2.7 V using a grounded gate NMOS device.

3.8.4 Bidirectional power clamp

An RC-triggered power clamp [Ker 99] is shown in Fig. 3.106, where during positive ESD stress between V_{DD} and V_{SS}, the RC-circuit detects the transient ESD signal and turns on the gate of the BigNFET transistor via an inverter chain with feedback. Hence, the BigNFET discharges the ESD current while operating in active MOS mode. For negative stress between V_{DD} and V_{SS}, the current is flowing through the diode D_1 placed parallel to the BigNFET. The addition of the dedicated diode for the negative stress polarity requires additional silicon area.

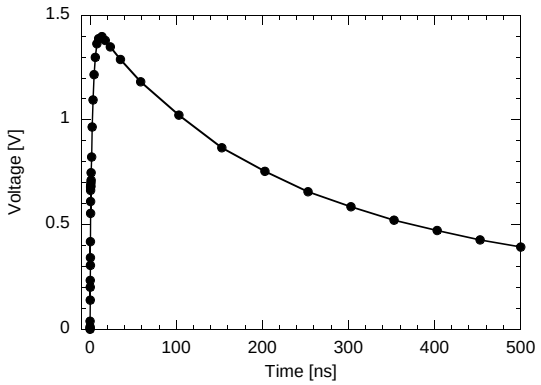

Figure 3.107: 1 kV HBM simulations of the circuit in Fig. 3.106. HBM stress was applied positive between V_{DD} and V_{SS}.

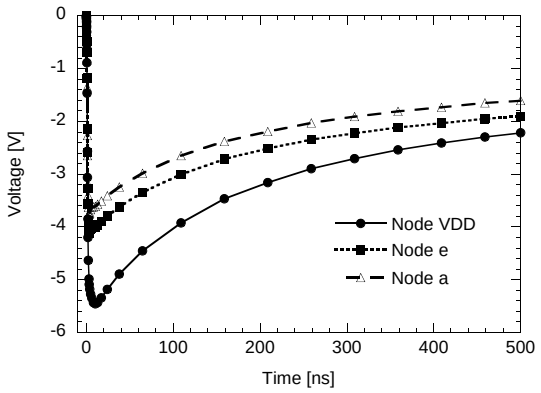

Figure 3.108: 1 kV HBM simulations of the circuit in Fig. 3.106 without reverse diode D_1. HBM stress was applied negative between V_{DD} and V_{SS}.

However, since a FinFET transistor has no body contact, it is a fully symmetric device, meaning that source and drain can be interchanged. We can exploit this symmetry by making the BigNFET operate in active mode during both positive and negative stress polarities, thereby avoiding the need for an additional reverse diode, D_1 in Fig. 3.106. 1 kV HBM simulations have been performed on the circuit shown in Fig. 3.106 for both polarities. In Fig. 3.107, the active clamp is operating as expected, clamping the voltage to 1.4 V. However, during negative stress events, simulated in absence of diode D_1, the inverters are not inverting anymore, but are acting as buffers, meaning that their output follows their input, but the signal is degraded. As V_{DD} goes negative, this signal is coupled onto node a, and all other nodes (b-e) follow this signal. As a result, V_{GS} of the BigNFET is zero, and hence the BigNFET remains off. Simulations show in Fig. 3.108 that since node e does not follow node a exactly, at some moment the BigNFET will switch on, but at too high voltage (-5.5 V).

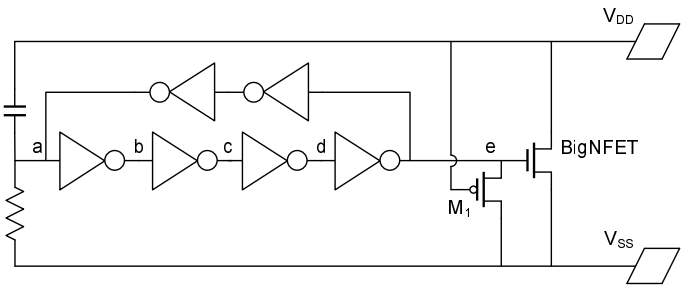

Figure 3.109: Schematic of symmetric RC-triggered FinFET power clamp. The addition of M_1 enables the BigNFET to operate in active mode also during negative stress events.

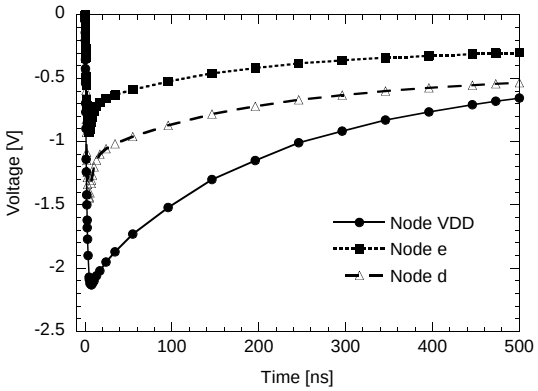

Figure 3.110: 1 kV HBM simulations of the circuit in Fig. 3.109. HBM stress was applied negative between V_{DD} and V_{SS}.

Node e should not be allowed to go negative, to be able to open the BigNFET. Therefore, an additional PMOS is added (M_1), Fig. 3.109, to pull node e to V_{SS} during negative ESD stress. Since node e is now controlled to be low during negative ESD stress, the BigNFET turns on at a much lower voltage. The maximum (absolute) voltage of node V_{DD} is -2.1 V according to the simulations in Fig. 3.110. As can be seen from Fig. 3.109, node e is not well controlled. Since the PMOS M_1 is not in an inverter configuration, the output voltage at node e, depends on the load of the PMOS. The load consists of the output of the inverter between node d and e. The voltage at node d is also seen in Fig. 3.110, and in this configuration, the PMOS of that inverter is in a conducting mode, limiting the pull-down of node e.

This solution can further be improved by controlling node d as well during negative ESD stress, trying to keep the output impedance of the inverter between node d and e as high as possible. Ideally, node d should be pulled to V_{SS}. To achieve this, additionally the NMOS transistor M_2 is placed as shown

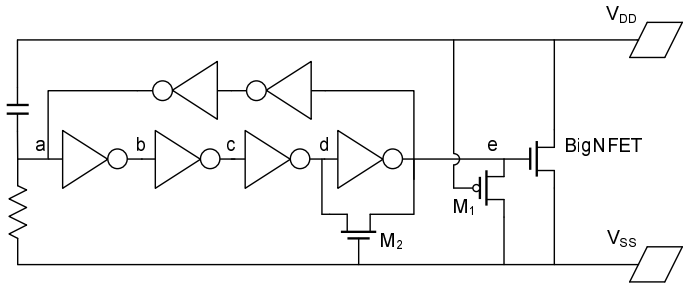

Figure 3.111: Schematic of symmetric RC-triggered FinFET power clamp based on Fig. 3.109. The addition of M_2 further improves the turn-on voltage during negative stress events.

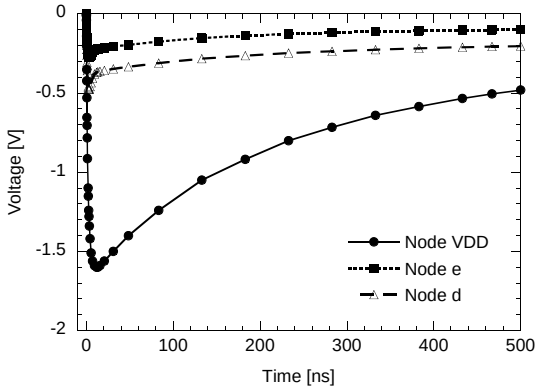

Figure 3.112: 1 kV HBM simulations of the circuit in Fig. 3.111. HBM stress was applied negative between V_{DD} and V_{SS}.

in Fig. 3.111.

During negative ESD stress, M_2 pulls node d as low as possible. This voltage is limited by the V_T of M_2 and therefore, node d is not fully zero. As a result, the output impedance of the inverter between node d and e is not infinite, and hence node e cannot be pulled fully to zero as well. However, the maximum (absolute) voltage at the V_{DD} is now limited to -1.6 V. This value is slightly higher than the maximum voltage during positive stress (1.4 V) due to the reasons explained above.

TLP measurements were performed on a bidirectional power clamp where a PMOS was used as BigFET transistor. The operation principle of such PMOS implementation is analog to the NMOS version. The TLP results are shown in Fig. 3.113, and almost no difference is seen in the IV-curves proving the concept of the fully bidirectional power clamp. During negative stress events, It_2 is a bit higher than during positive stress which can be attributed to an additional current path through transistor M_1 in combination with the last

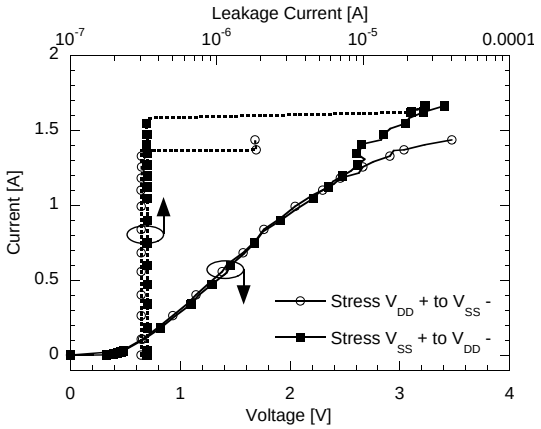

Figure 3.113: TLP measurements of the bidirectional FinFET power clamp, using a PMOS as BigFET.

driver stage.

3.9 Conclusions

This work provides fundamental insights into the behavior of FinFET devices under ESD conditions for various layout and process conditions.

Special care has to be taken when normalizing the ESD performance parameters. For physical understanding of ESD behavior in FinFETs, intrinsic silicon width W_{intr} (3.1) should be used. Layout efficiency can be studied using W_{layout} (3.2). ESD robustness of drivers is evaluated using W_{chan} (3.3). For comparison with other technologies, the effective width W_{eff} (3.4) is preferred.

Uniform current conduction is guaranteed in grounded gate MOS devices due to their floating base (no snapback), yielding kV HBM levels for multi-finger multi-fin devices. Some degree of non-uniform failure exists at high current levels which can be improved by increasing gate length and various ballasting techniques. MOS devices in active MOS diode mode have better ESD performance for narrow gate lengths compared to bipolar, but opposite for larger gate lengths. Gated diodes should be drawn as planar-like structures instead of using narrow fins because they have the best performance in terms of It_2 per layout due to absence of fin-to-fin spacing overhead and It_2 per capacitance because of reduced parasitic capacitances. In general, narrow fin devices have improved cooling properties but suffer from reduced area efficiency.

Well doping reduces leakage current for wide fin devices without impacting

ESD performance. SEG drastically improves It_2 and R_{on} and removes any oversilicidation problems. Also Silicide Blocking removes the oversilicidation effect. It further improves It_2 due to improved failure current uniformity at the expense of increased R_{on}. Strain also increases It_2 by improving the carrier mobility and by improving failure uniformity. FinFET technology development is still facing a lot of process challenges which have a direct impact on the ESD performance of the devices.

A FinFET design methodology is required to find the solution for a multi-dimensional optimization problem depending on functional and ESD limitations. The developed methodology yields the optimal design solution, which was found to be sensitive to layout and process deviations. The absence of a body contact for the MOS device in diode mode can make it less efficient than in bipolar mode for a given set of constraints.

All the results demonstrate that the possible extreme sensitivity of FinFET devices would not be a showstopper for the advanced nanotechnologies if ESD is considered during the technology development. However, even with this knowledge, the design of ESD protection for FinFET technology appears to be a challenging task in the future.

Chapter 4

ESD Protection for Narrowband RF CMOS Circuits

The traditional low-capacitance RF-ESD protection approach is not feasible anymore for narrowband RF circuits operating at frequencies >5 GHz. Inductive based ESD protection is an excellent alternative solution which improves with increasing frequency in terms of RF performance, ESD performance (both HBM and CDM) and area consumption. This technique has been validated on a number of case studies, including Low Noise Amplifier (LNA) and Power Amplifier (PA) designs implemented in 90 nm, 45 nm planar and 45 nm FinFET CMOS technologies for operating frequencies ranging from 5 GHz to 60 GHz.

4.1 Introduction

Emergence of extensive applications for portable electronics has fueled the rapid deployment of CMOS based integrated RF front-ends. These technologies demonstrated transit frequencies well above 150 GHz, e.g. in a 90 nm CMOS technology, and are commercially available for manufacturing. This chapter focusses on ESD protection for narrowband RF circuits. Chapter 5 discusses in a similar way wideband RF circuits.

In an RF front-end, the LNA is one of the critical building blocks. The LNA, being connected to the outside world through its antenna can therefore easily be exposed to ESD stress events. Incorporating sufficient and suitable ESD protection on the LNA requires that the added ESD protection does not degrade the designed functional performance parameters of the LNA. The most important performance figures for the LNA along with a typical target

Table 4.1: Typical performance figures for a LNA.

Performance figure	**Target value (@f_C)**
f_C	5.5 GHz
S_{11}	<-10 dB
S_{22}	<-10 dB
S_{21}	>15 dB
S_{12}	<-30 dB
NF	<3 dB
IIP3	As high as possible
P_{tot}	As low as possible
Area	As small as possible
ESD protection level	>2 kV HBM

specification of each parameter are listed in Table 4.1. Throughout this thesis, the LNA is used as a test-vehicle for the different narrow- and wideband ESD protection strategies. Also, one example is given in this chapter where ESD protection is provided for a PA at the output of a transceiver.

Next generation wireless license-free communication will use a 7 GHz band between 57 and 64 GHz. Various benefits exist of operating in this 60 GHz frequency band such as two-way wireless communications at data rates similar to fiber optic cable, excellent immunity to interference, high security due to short transmission distances and hence also frequency re-use. Downscaled CMOS recently has been shown to be a valid technology for such applications [Sche 08] [Tano 08].

The analog and RF performance of FinFET devices have been extensively studied in [PhDSubramanian], while [PhDBorremans] focusses on the impact on circuit design and performance. Scaling opportunities from an analog point of view can be interpreted from Fig. 4.1 for planar and FinFET technologies. The unity current gain cutoff frequency, f_T, is plotted versus the achievable transconductance efficiency (g_m/I_{ds}). It can be seen that, to realize a certain g_m when a certain current is available, the planar 40 nm devices are faster. Alternatively, when a specific speed (f_T) is required, the planar 40 nm devices consume less current for similar g_m. Design freedom is thus captured in these curves: speed can be traded off for power. It can be interpreted from Fig. 4.1 that with the current status of the technology, better performance and design freedom is expected from the planar 40 nm transistors, as compared to the FinFETs, who perform similar to the 90 nm devices. The reduced f_T for the FinFET devices can be attributed due to increased parasitic resistances, which impact the transconductance, and increased parasitic capacitance, as

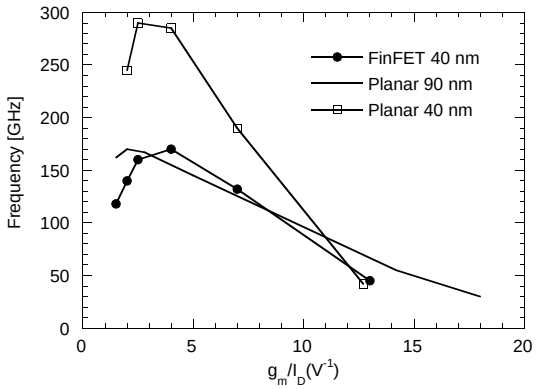

Figure 4.1: f_T versus g_m/I_{ds}, for a 90 nm and 40 nm planar and 40 nm FinFET technology.

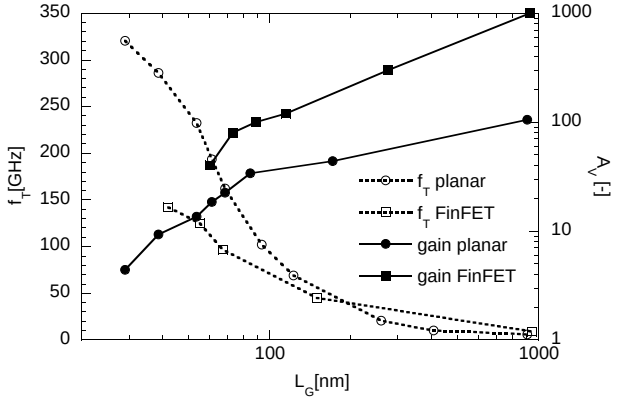

Figure 4.2: For planar and FinFET devices, f_T and the intrinsic gain g_m/g_{ds} at 0.2 V overdrive versus the channel length L_g.

also measured in section 3.7.1. Device optimization should bring the FinFET curve in Fig. 4.1 closer to the planar one. Fig. 4.2 plots the intrinsic gain (g_m/g_{ds}) and f_T versus channel length L_g. While FinFETs show higher gain for short channel lengths, planar devices can attain similar gain at similar f_T by increasing the channel length. Observe from Fig. 4.1-Fig. 4.2 that a high f_T can be exclusively achieved with planar devices. On the other hand, extremely high gain can exclusively be achieved with FinFETs. The excellent control of SCE results in high output resistance (low g_{ds}). Moderate f_T and gain lie in both devices range.

A generic on-chip ESD protection implementation can be represented as shown in Fig. 4.3, for input, output, and power supply pins of a LNA. The elements ESDx are ESD protection devices, which can be diodes, MOS devices, passives, etc. The ESD protection strategy wherein diodes divert the ESD stress current

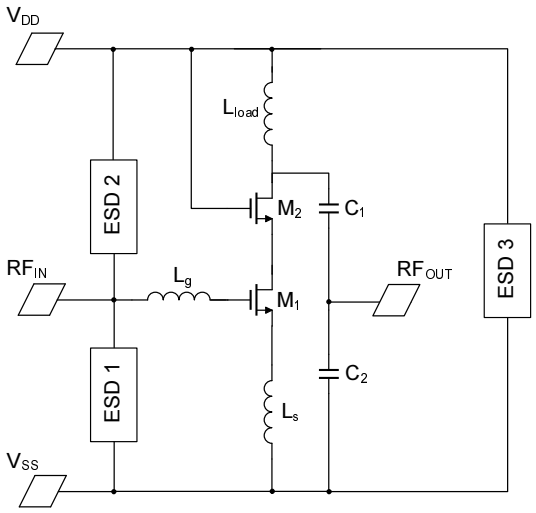

Figure 4.3: Basics of on-chip ESD protection. The core circuit represents the LNA topology used in this work. ESD1-3 are the ESD protection devices.

from the input/output pins to the power clamp is one of the most commonly used in designs [Rich 00] [Velg 01]. Diodes of appropriate size and/or type are implemented such that the added parasitic capacitance at the RF pins does not alter any RF circuit parameter. Implementing the full chip protection can be rather straightforward once the RF pin is protected with respect to the power supply/ground, since there are no loading constraints (therefore no critical size constraints) on the power/ground pin ESD protection.

However, using the conventional diode ESD protection will become more and more difficult when technology further scales and when RF operating frequencies keep on increasing. This is because the magnitude of the parasitic impedance of the dual diodes, shown in Fig. 4.4 (left), which is parallel to the RF signal line, decreases with increasing frequency, according to

$$|Z_{ESD}| = \left| R_{s,ESD} + \frac{1}{j\omega_{RF} C_{ESD}} \right| = \sqrt{R_{s,ESD}^2 + \frac{1}{\omega_{RF}^2 C_{ESD}^2}} \tag{4.1}$$

In order to minimally impact the RF performance, this impedance should be as high as possible. Therefore, an upper limit is posed on the maximum allowed parasitic capacitance, and hence maximum diode size. When the RF frequency increases, the allowed diode size decreases and $R_{s,ESD}$ increases, resulting in a degradation of the ESD performance. These limitations will be demonstrated in the first section of this chapter. Therefore, in the remaining of the chapter, new narrowband RF-ESD protection concepts are introduced which can provide adequate ESD protection for RF applications in future CMOS technologies.

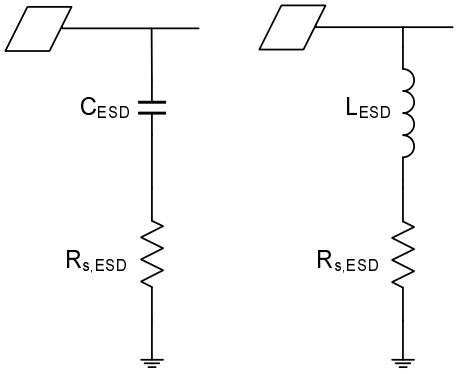

Figure 4.4: Equivalent schematic of capacitive (left) ESD protection devices, such as diodes or grounded gate NMOS, and inductive (right) ESD protection devices.

A novel technique is codesign where the ESD protection is incorporated in the impedance matching networks [Vass 04] as will be demonstrated in section 4.3. Further, a number of previous reports highlighted the use of inductors to shunt the ESD current from the core circuit, without disturbing the RF signal propagation [Lero 04] [Hyvo 03] [Ker 03] [Hyvo 03b] [Issa 08]. These involve an on-chip inductor implemented either as a tuned resonator or filter, or as an off-chip component, mostly realized in relatively older technologies ($> 0.13\ \mu$m). The application of an ESD protection inductor for RF circuits with increasing operating frequencies looks promising, because contrary to the dual diode approach, the magnitude of the parasitic impedance of the ESD inductor, as shown in Fig. 4.4 (right), increases with increasing frequency, according to

$$|Z_{ESD}| = |R_{s,ESD} + j\omega_{RF} L_{ESD}| = \sqrt{R_{s,ESD}^2 + \omega_{RF}^2 L_{ESD}^2} \tag{4.2}$$

Therefore, smaller L_{ESD} values can be used which have also smaller $R_{s,ESD}$. However, its implementation is not trivial and requires extensive simulations and custom design of suitable inductors, or adaptation of the functional core to fit the available inductor values. In our work, the ESD inductor is added either as "plug-and-play", i.e. without altering anything to the original design, or in a codesign approach, where any remaining parasitic capacitance (such as the bondpad capacitance) is tuned out. Soldner et al [Sold 05] compared the low-capacitance approach with codesign and come to the same conclusion that <5 GHz the low-C approach is preferable despite their intrinsic RF performance degradation since they are still the most simple and most rapidly realizable. Above >5 GHz, novel solutions are required.

Another major concern for RF-ESD protection is the CDM-type of ESD stress, as was described in section 2.2.3. Compared to HBM, CDM is characterized by much higher current levels (6-10 A), much shorter (∼1 ns) current pulses and

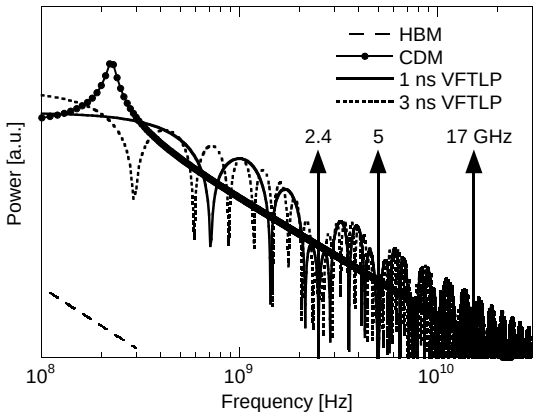

Figure 4.5: Frequency spectrum of HBM, CDM, 1 ns and 3 ns VFTLP. Different WLAN frequencies are indicated.

much faster rise times, typically 400 ps or less. As can be seen in Fig. 4.5, the frequency spectrum of CDM and VFTLP extends well into the GHz range and hence they will be coupled much more inside the RF circuit than HBM. At higher RF operating frequencies, this coupling is reduced, as will be shown by several examples in this chapter. Such fast current pulses give rise to voltage overshoots, which can potentially damage the core circuit.

VFTLP measurements, described in section 2.4.2, are used to characterize protection-devices and strategies in the time and current domain of CDM. VFTLP typically has a rise time of 200 ps and pulse widths of 1 to 10 ns. Since CDM is a single pin bipolar stress event, no one-to-one correlation exists with the unipolar VFTLP measurements due to different current paths for both types of ESD stress. Therefore, VFTLP was performed in this thesis on-wafer with two independent needles connected by a short ground loop instead of using (expensive and fragile) RF probes. As such, VFTLP measurements can be performed between all possible pin-to-pin stress combinations to find weak spots, which would not be possible otherwise due to the fixed RF probe pitch. The downside is that voltage overshoots will be measured due to the parasitic needle inductance, however they can be removed by proper calibration, as was described in section 2.5.2. The VFTLP pulses used have 3 ns pulse width and 400 ps rise time arriving at the bondpads, which meets the CDM pulse specification given in the JEDEC standard [CDM 08]. According to the JEDEC specification, a rough correlation between CDM and VFTLP can be estimated to 90 V/A for small packages and 45 V/A for large packages. A similar correlation factor has been found in recent work [Wata 08].

The outline of this chapter is as follows. First the standard dual-diode and the codesign technique are benchmarked using a 5 GHz narrowband LNA, implemented in a 90 nm CMOS technology, in section 4.2 and section 4.3

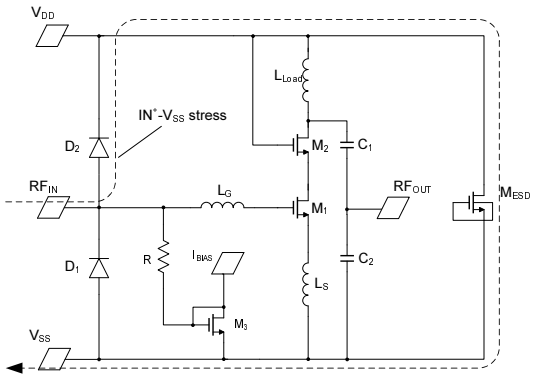

Figure 4.6: General dual-diode based ESD protection concept.

respectively. Their RF and ESD results are compared to the newly developed "plug-and-play" inductor to ground technique in section 4.4 using the same demonstrator circuit. In section 4.5, it is shown that when the RF operating frequency increases, the inductor to ground technique becomes better in terms of area consumption and efficient ESD protection level. This makes a 5 GHz LNA the worst-case demonstrator for such ESD design concept. The applicability of the inductor to ground is demonstrated by several examples for 45 nm planar and FinFET technologies up to frequencies of 60 GHz. Next, another technique combining the benefits of the inductor and a codesign approach is discussed in section 4.6, where a transformer-based ESD protection is evaluated. For the inductor based approaches, special emphasis is paid to CDM robustness using on-wafer VFTLP measurements. Finally, in section 4.7, our results are benchmarked against the state-of-the-art publications.

4.2 Dual Diode Methodology

The dual-diode strategy is by far the most widely used ESD protection in integrated circuits, for digital as well as for analog or mixed signal applications. This is also a perfect example of the plug-and-play ESD protection strategy, where ESD protection structures are placed after complete design of the RF circuit such that the ESD and RF designs are not coupled to each other. This plug-and-play technique is used for digital circuits as well. Diodes are used for both ESD1 and ESD2 elements in Fig. 4.3, resulting in the basic schematic as shown in Fig. 4.6.

The LNA operates at 5 GHz and is implemented in a 90 nm CMOS technology. The LNA circuit employs a common source topology (transistor M_1), which is matched to 50 Ω at both input and output. By using a single amplification stage, power consumption is reduced and degradation of linearity is prevented.

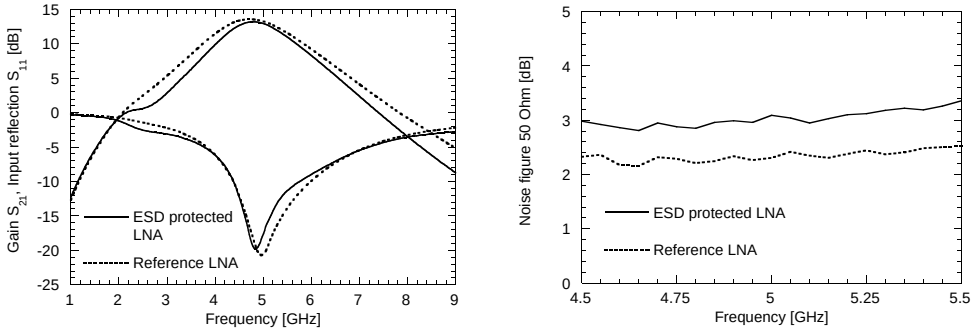

Figure 4.7: Gain and S_{11} (left), and Noise Figure (right) of the 90 nm CMOS 5 GHz LNA without ESD protection and with ESD protection using inductors and additional diodes at the input nMOS gate.

The cascode transistor M_2 reduces the Miller effect, significantly lowering the input capacitance seen at the gate of input transistor M_1. It also improves reverse isolation, increasing the stability, and the decoupling of the input and output impedance matching design.

The input impedance matching (S_{11}) is achieved using a 0.4 nH source degeneration inductor, L_S [Shae 97]. Inductor L_G, 4 nH, is used to tune-out the remaining capacitive impedance at the gate of M_1. The output matching (S_{22}) is achieved by a capacitive impedance divider consisting of Metal Insulator Metal (MIM) capacitors C_1 and C_2. It adds the exact amount of capacitance to resonate with the load inductor L_{load} at 5.5 GHz and to transform the impedance level at the drain of M_2 to 50 Ω.

The sizes of the diodes used are 65 μm^2. Between the power supply and ground rails, a 400 μm wide ggNMOS device is used as power clamp. The diodes were selected based on their stand-alone ESD capability to handle more than 2 kV HBM stress. The power clamp sizing was not considered as it poses no constraint on the RF functionality. The diodes have their own noise contribution increasing the NF of the LNA. In fact, by adding the ESD protection, only the linearity is improved resulting from the reduced S_{21}. Fig. 4.7 shows the S-parameters and noise figure measurement results from the LNA on the left and right, respectively.

To ensure ESD robustness, all possible ESD current paths need to be carefully evaluated. When input is stressed positive towards ground, the ESD current should flow only through the predefined current path, i.e. through the ESD diode between input and V_{DD}, and then through the power clamp to ground (dotted line in Fig. 4.6). The HBM measurement showed that in this worst case stress combination, the LNA passes only 500 V, much less than the expected 2 kV, which can be attributed to the 1.5 nm thick gate-oxide failure of transistor M_1. During this stress combination, the total voltage build up

across the ESD protection elements is fully transferred to the gate of M_1 due to the absence of an on-chip coupling capacitor in this design. Therefore, it is very beneficial to add such on-chip decoupling capacitor between the ESD diodes and the core LNA. However, this capacitor, being non-ideal, will also have its impact on the RF behavior of the circuit and hence has to be taken into account in the simulations for circuit optimization.

4.3 Codesign Methodology

The same 90 nm CMOS 5 GHz LNA from Fig. 4.3 has been protected using a so-called codesign approach [Vass 04]. In such codesign strategy, the ESD protection is integrated into the matching circuit of the corresponding RF block whereby the ESD and RF circuit functionalities are merged into the same physical devices. This means that there is more designer freedom since the boundaries between the RF and ESD design have been removed, and the complete circuit including the ESD protection and the RF core is being simultaneously optimized as one single design.

Fig. 4.8 shows the principle schematic of the input stage of the chosen common source topology. In a 'classical' RF design, the input of the circuit is defined at the reference plane *A*. R_s denotes the source impedance, C_{par} is a parasitic capacitance, which includes the gate-drain and the gate-bulk capacitances. Well known from RF design theory [Lee 98], L_s is used to set the real part of the input impedance equal to R_s at the desired frequency, while L_g is used to adjust the series resonance. L_1 and C_1, together with L_g and C_{par} can be used to construct a π-type RF matching circuit that allows, in the presence of large C_{par}, for more freedom to setup the resonant (operating) frequency, bandwidth and impedance transforming ratio. The latter is determined by the design considerations of the amplifying stage (M_1-M_2). The π-type matching circuit shifts the circuit input to the reference plane *A'* and makes it possible to incorporate a robust ESD protection when replacing C_1 and C_{par} with ESD protection components, as shown in Fig. 4.8.

In this way, the ESD and the RF properties of the LNA are designed essentially together. Consequently, the constraints on the ESD device capacitance (proportional to the ESD performance) are reduced, thus increasing the failure threshold of the circuit by using larger ESD devices. Depending on the RF design strategy, other circuit topologies, such as common gate and differential amplifier can be implemented.

The wire bonding and packaging introduce another constraint to account for in the codesign. The package LC parasitic at the RF pin can be, to a first order, approximated with an equivalent LC-circuit. It can be merged easily in the existing ESD design and can even help to provide better matching based on the

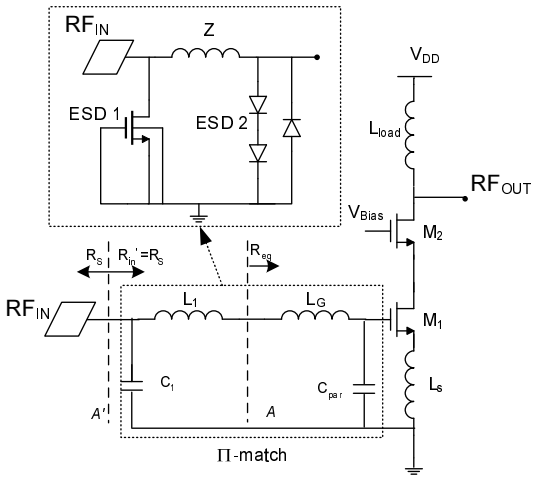

Figure 4.8: Implementation of additional impedance transformer ($L_1 - C_1$) in the input matching of the LNA and the dashed line box indicates the RF equivalence of a two stage ESD protection as indicated by the arrow.

additional degree of freedom. The adjustable package bond-wire inductance and the possible implementation of a separate variable capacitance device in parallel to the ESD devices in the π-type matching circuit can be used to fine tune the resonance match, providing further flexibility for compensation of the unforeseen parasitic.

The ESD protection devices used for this design consist of a 120 μm wide ggNMOS [Vass 03] and small diodes of 12 μm^2, see Fig. 4.8. This LNA is also processed in the 90 nm RF CMOS technology. All the RF parameters degrade by adding the large ggNMOS, but they are still within the target specifications. The degradation in the input matching indeed resulted in the higher gain for the co-designed LNA (Fig. 4.9).

HBM ESD testing was performed on the codesigned LNA. When the input was stressed positive with respect to ground, the LNA passed 2.5 kV but failed at 2.6 kV. This shows that the ESD protection strategy did work even with a large ggNMOS. The input, when stressed positive with respect to V_{DD}, passed 1.9 kV but failed at 2 kV. In this stress combination, the ESD current path is still through the ggNMOS to the ground and from there through the power clamp to V_{DD}, since there is no dedicated ESD protection between input and V_{DD}. The observed failure is thus due to the higher voltage drop at the input gate which is a sum of voltage drops across the ggNMOS, interconnect parasitic resistances and the power clamp. The power pads survived a stress level of 4 kV.

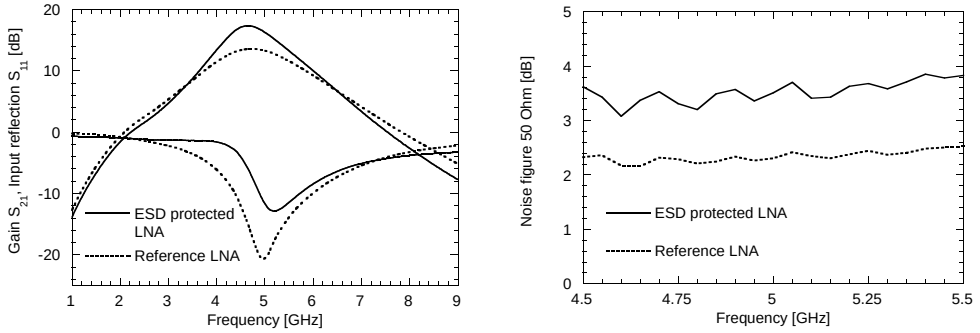

Figure 4.9: Gain and input matching (left) and the noise figure (right) of the codesigned LNA compared with the LNA without any ESD protection.

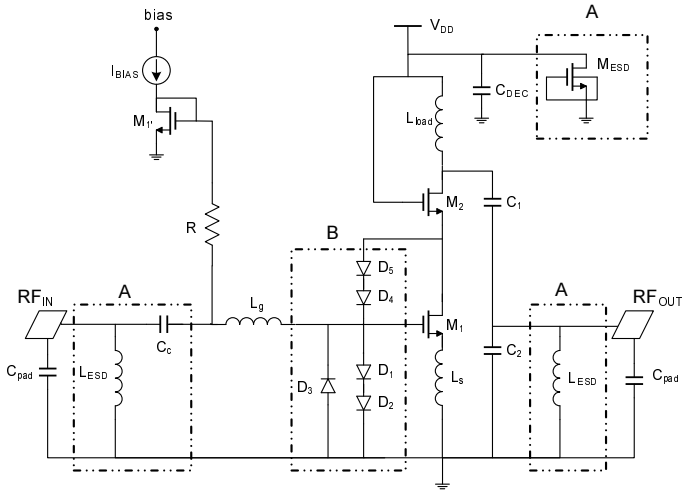

Figure 4.10: The schematic of the Low Noise Amplifier with shunt inductor protection. Dashed line rectangles A represents standard ESD protection, and B corresponds to additional ESD protection.

4.4 Inductor to Ground Methodology

When placing an inductor between the RF pad and ground, the inductor acts as a low pass filter for the ESD signal, diverting the ESD current to ground, and allows the RF signal to pass to the LNA core (high pass for the RF signal). More accurately, with the parasitic capacitance of the circuit, it is essentially an LC band pass filter. The ESD inductor is added as "plug-and-play" as in the case of the dual-diode strategy. Since the inductor is a bi-directional element, no inductor is needed to V_{DD}. Fig. 4.10, shows the schematic of the LNA with the inductors (L_{ESD}), boxes A, placed at both input and output and realized in a 90 nm RF CMOS technology.

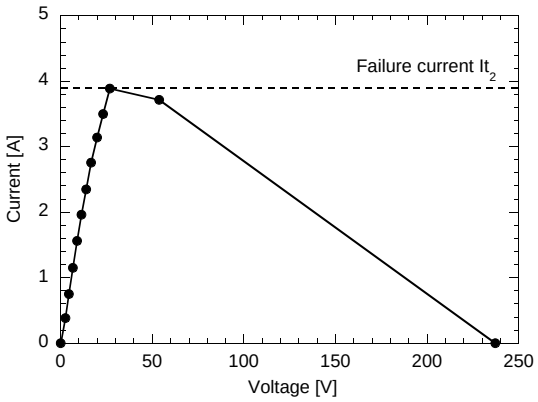

Figure 4.11: Typical TLP-IV measurement of an inductor. The inductor fails at the vias at the underpass, resulting in an open condition.

4.4.1 Back-end of line (BEOL) inductor

Backend inductors used in this section could conduct well up to 4 A of TLP current without any RF or DC degradation. A typical TLP-IV measurement is shown in Fig. 4.11. At an It_2 level of $\sim$ 4 A, the vias at the underpass of the inductor fail, resulting in an open condition.

A grounded gate NMOS device, M_{ESD}, is used as power clamp at the power supply node V_{DD}. The ggNMOS can be sized as large as required because no RF signal is present at the power supply. Further, since all the ESD protection devices work bi-directionally, all possible pin-to-pin combinations are protected against ESD stress.

The inductor selection was based on a trade-off between RF and ESD requirements. It can be treated as a series connection of an inductance L_{ESD} and a resistance $R_{s,ESD}$:

$$Z_{ESD} = \omega_{RF} L_{ESD} + R_{s,ESD}. \tag{4.3}$$

According to [Lint 05], the impact on the noise factor due to addition of L_{ESD} is:

$$F_{ESD} \approx \frac{R_s R_{s,ESD}}{(\omega_{RF} L_{ESD})^2}, \tag{4.4}$$

with R_s the source impedance which is typically 50 Ω. For minimal impact on the noise figure, preferably a large L_{ESD} is chosen. On the other hand, when an ESD event occurs across the inductor, the fast rising edge of the ESD current will cause a voltage overshoot across the inductor (node RF_{IN}), as the current through the inductor cannot change instantaneously:

$$V_{RFIN} = L_{ESD} \frac{dI_{ESD}}{dt} + R_{s,ESD} I_{ESD} \tag{4.5}$$

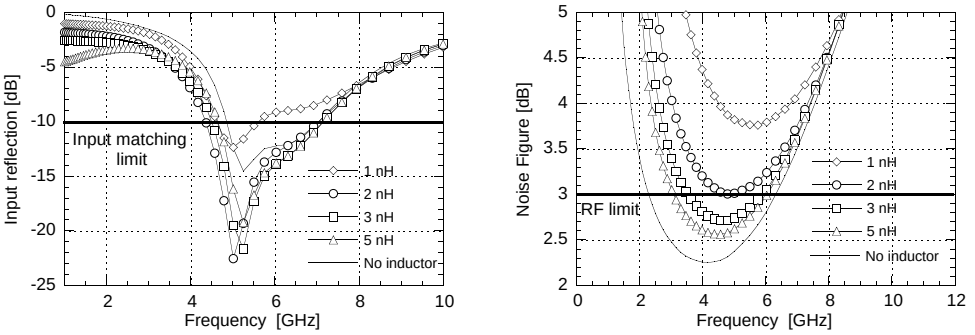

Figure 4.12: Simulated input matching (left) and noise figure (right) for different values of ESD inductors. All inductors fulfill the requirement of S_{11}<-10 dB and larger inductors give rise to higher voltages across transistor M_1.

The decoupling MIM capacitor (C_C) couples this transient voltage onto the node V_{gate} of transistor M_1, as a capacitive divider:

$$V_{gate} = V_{RFIN} \frac{C_C}{C_C + C_{M1}} \tag{4.6}$$

This means that an inductor with low inductance and low on-resistance is preferred to reduce the voltage drop across its terminals as much as possible since this voltage could possibly damage the thin gate oxide of transistor M_1. A clear trade-off between RF and ESD is visible. The optimal solution only just meets the RF requirements and hence results in the highest possible ESD protection level for the given application.

Since only a limited set of inductors (1 nH to 5 nH) were available from the design library, RF and ESD simulations are used with dedicated inductor models to determine the optimal solution. The simulation results on input matching, Fig. 4.12 (left), shows that using any of these inductors will fulfill the criteria S_{11}<-10 dB. Simulations of the power gain (S_{21}) did not reveal any significant dependence on the value of the ESD inductor. On the other hand, since the noise of the LNA is mostly determined by the elements at its inputs, an impact on noise figure is seen when adding L_{ESD}. The NF increases with decreasing value of L_{ESD}, Fig. 4.12 (right). Its requirement of NF<3 dB prevents the 1 nH inductor from being a valid candidate.

HBM transient simulations were performed to determine which inductor provides the best ESD protection. This simulation with the input stressed with respect to ground, showed in Fig. 4.13 that all inductors except 1 nH yielded almost 4 V across the gate of M_1 which is very close to the oxide breakdown voltage in this technology. Since this is only a simulation result, the real voltage at the gate could differ and be even a bit higher. Moreover, taking statistics

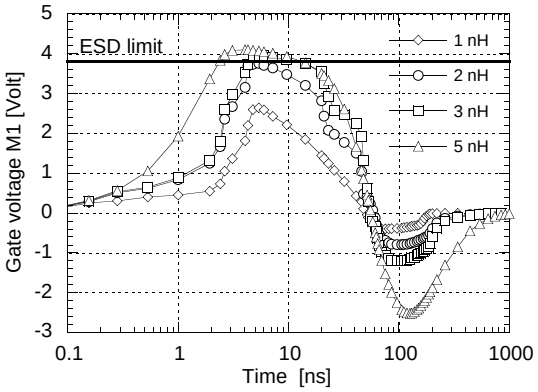

Figure 4.13: Voltage at the gate of the input transistor during 2 kV HBM simulations for different values of ESD inductors.

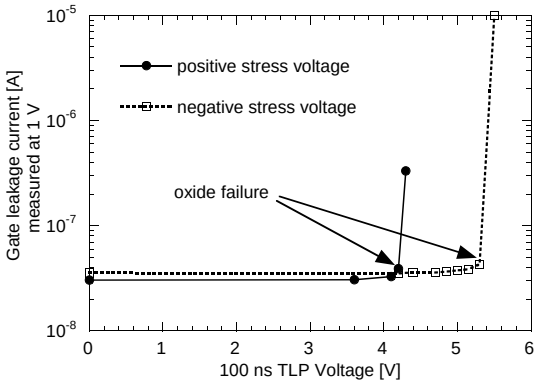

Figure 4.14: Measured absolute value of leakage currents of the gate oxide of the RF transistor for positive and negative voltage stress conditions using 100 ns TLP. The gate was stressed versus source, drain and bulk.

into account, and to make sure that 99.9% of all oxides are not degraded, the maximum allowed voltage should be lowered to 3.8 V (according to Weibull statistics). This voltage was calculated based on [OCon 03] with a Weibull slope β of 1.5 and a voltage acceleration factor γ of 6 dec/V.

Fig. 4.14 shows that the gate oxide of transistor M_1 can withstand +4.2 V and -5.4 V. This means that stressing the input positive with respect to ground is worst-case compared to a negative stress at the input with respect to ground. During negative stress, M_1 will be operated in accumulation regime, where the negative voltage spreads over both the oxide and the accumulation region. Therefore, a higher voltage can be built-up prior to damaging the gate-oxide during the negative stress. In the case of positive stress, the transistor is driven into depletion or into inversion and the gate-oxide fails thus at a lower voltage.

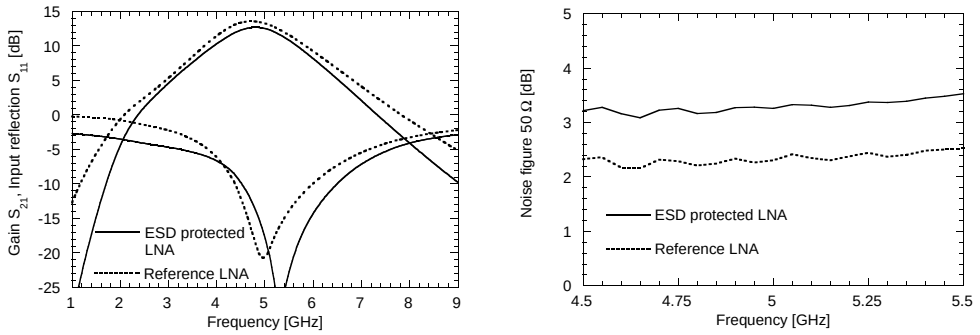

Figure 4.15: Measured input matching S_{11} (left) and measured noise figure (right) for the LNAs with and without ESD inductors. The difference in S_{11} at low frequencies is due to the series resistance of the ESD inductor.

Based on this RF and ESD analysis and based on the emphasis on RF functionality, a 3 nH inductor was chosen as ESD protection inductor at both input and output because of its lower NF. RF measurements were performed on both LNAs. Although S_{11} was shifted marginally to higher frequencies, Fig. 4.15 (left), for both LNAs due to an inaccurate source inductor model, the results were still on target (proven by re-simulations with updated model extracted from silicon). Fig. 4.15 (right) shows the measured NF for both LNAs. A 1 dB increase in NF is observed due to the contribution of the inductor. In case this increase in NF is not acceptable from RF point of view, a larger value of L_{ESD} should be chosen, which would result in a decreased ESD performance.

The LNA without ESD protection already fails at 9 V HBM stress, because of its unprotected sensitive gate oxide. The LNA with only the inductor as RF ESD protection has an ESD robustness of 2.2 A TLP, and 2.5 kV HBM at all pins, which is in agreement with what was observed during the transient HBM simulation.

A full RF measurement should be performed after any ESD stress pulse to make sure no RF degradation has occurred. For example, any change in input matching S_{11} would indicate failure at the RF_{IN} pin. However, during ESD testing, a quick method is needed to detect failure, without the need for any additional equipment such as a network analyser. Since the inductor only has a few ohms of resistance to ground, leakage at the input node cannot be used as criterion. Therefore, another criterion is needed. If during monitoring of the leakage at the bias node (if this node is present in the design) the bias resistor R is measured, most likely the gate oxide of M_1 has failed. Without failure, an open circuit should be seen here. Another possible criterion to detect failures due to ESD stress at the input pin, invariably at M_1, is to use the leakage at the V_{DD} node. During positive bias at this node, transistor M_2 goes into strong inversion, such that any damage at transistor M_1 can be monitored.

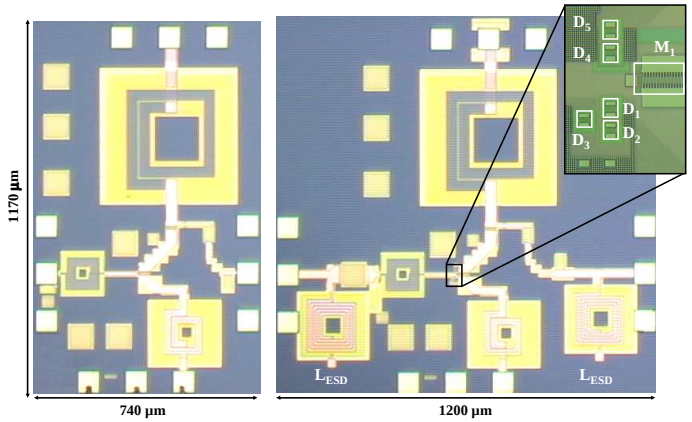

Figure 4.16: Micrographs of the reference LNA (left) and ESD-protected LNA using 5 LM back-end of line (BEOL) inductors with diodes (right). The inset on the micrograph on the right side shows the additional clamping diodes.

This is much more sensitive than monitoring at the bias node, because now there is no big (kΩ) resistor in series in the leakage path. In this work, results of both quick DC leakage measurement described above correlated perfectly with the RF measurements performed.

If higher ESD robustness is required, additional optimization can be achieved by limiting the voltage, positive and negative, at the gate oxide to a safe value to prevent any degradation. A simple method is to implement very small diodes close to the gate of the core transistor, as shown in box B in Fig. 4.10. The only purpose of these diodes is to clamp the voltage at the gate, which is in the order of a Volt and it is not required that they carry a large current (a few mA). Thus these diodes can be very small and their capacitance negligible. Fig. 4.16 shows the corresponding micrographs of the 'LNA' and 'ESD-LNA with diodes'. The inset on the micrograph on the right side shows the added diodes.

In this LNA, the gate of M_1 was biased at 0.6 V, so two diodes in series from gate to ground are needed in parallel with a diode from ground to gate. A worst-case scenario has been simulated with the compact model of a diode of 4x2 μm^2 capable of conducting more than 160 mA during 100 ns. Plugging this into the simulator, almost no RF degradation could be noticed. From practical implementation point of view, due to the small footprint, these diodes can be easily placed right in front of the transistor gate. By adding the extra clamping diodes, the ESD robustness of the circuit is dramatically improved yielding 4 A of TLP and 5.5 kV of HBM. These diodes also improve the MM performance from 225 V up to 350 V. A summary of these measurement results is shown in Table 4.2.

Table 4.2: Summary of ESD measurement results, stressed input to ground.

Input to ground	**LNA**	**ESD-LNA w/o diodes**	**ESD-LNA with diodes**
HBM [kV]	0.009	2.5	5.5
MM [V]	-	225	350

When applying positive stress on the V_{DD} pin with respect to ground, both the drain and gate of transistor M_2 (Fig. 4.10) are pulled high. The transistor goes into strong inversion, a channel is formed between drain and source, and this raises the source potential. Therefore, the gate oxide of transistor M_2 remains unstressed. One must make sure however, that the drain-bulk junction of M_2 does not start to avalanche, since the transistor was not designed to operate in this region, and hence it should be avoided. However, a more severe problem arises during this positive stress on V_{DD}. When transistor M_2 starts conducting as explained earlier, stress is seen across the gate oxide of transistor M_1 between its drain and gate terminal. Therefore, additional circuitry is needed to protect M_1 during this type of ESD stress. As before, adding simple diodes can solve the problem. Two diodes are added in series between the drain and gate of M_1 as shown in box B in Fig. 4.10. These small diodes have a capacitance of 11 fF each, thus the total added capacitance between drain and gate of M_1 is 5.5 fF. Since this value is very small, and because of the presence of the cascode transistor M_2, there is no significant Miller effect increasing the capacitive load at V_{gate}. RF simulation with a RF diode compact model did not show significant change in RF performance of the LNA circuit. By adding these diodes, a protection level of 5 A TLP is measured between V_{DD} and ground, which corresponds to the failure level of the power clamp. Fig. 4.17 shows the gain and S_{11} (left) and the noise figure (right) of the LNA with ESD inductor with and without added diodes. This figure clearly shows that the added diodes only result in a minor degradation in the noise figure.

4.4.2 Above-IC inductor

The inductive ESD protection strategy requires the lowest possible on-resistance in order to lower the potential drop across the inductor which will eventually result in a voltage build-up across the ultra-thin gate oxide (capacitively coupled across MIM capacitor). Although these inductors could, by itself, show very high ESD robustness, in the state-of-the-art CMOS processes the Q-factor is limited by resistive losses in the inductor metal layer(s) and by coupling to the lossy semiconductor substrate. Because of this relatively high series resistance additional precautions have to be taken to secure the gate

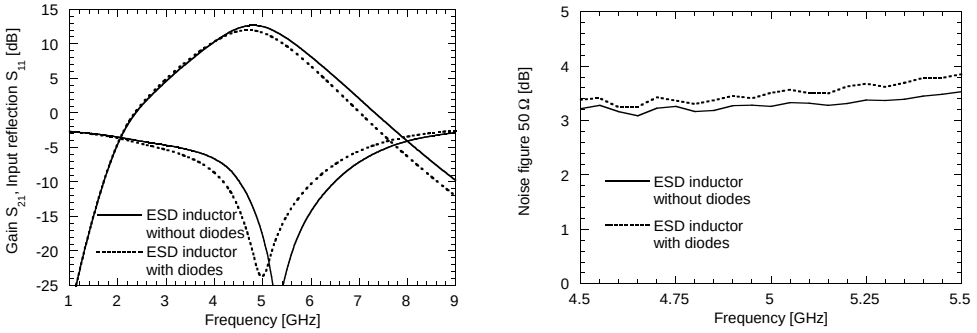

Figure 4.17: Gain and S_{11} (left), and noise figure (right) of the 90 nm CMOS 5 GHz LNA with ESD inductor with and without additional clamping diodes at the input nMOS gate. The impact on the RF performance of the diodes is marginal.

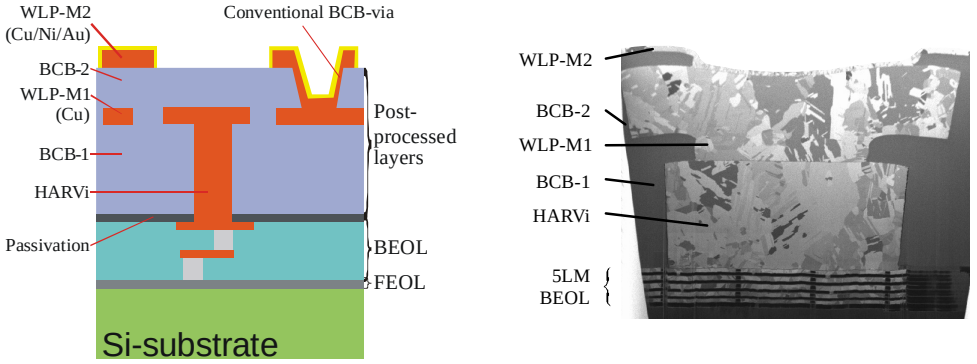

Figure 4.18: Left: schematic cross-section of the "above passivation"-layers. Right: a SEM cross-section of WLP-M1 and WLP-M2 on top of M1-M5 metal levels: conventional via (through BCB-2) and High Aspect Ratio Via or HARVi (through BCB-1).

oxide, such as adding clamping diodes as described earlier.

An attractive and cost effective alternative solution is to realize the inductors using thin-film wafer level packaging (WLP) techniques [Carch 04]. In this case, multiple BCB (benzo-cyclobutene dielectric, K=2.65) and thick electroplated Cu layers (WLP-metal 1 and WLP-metal 2) are deposited on top of the IC passivation, hence high-quality interconnects and inductors are created. Connection to the normal back-end of line (BEOL) layers is made with High Aspect Ratio Vias (HARVi). Fig. 4.18 shows an example schematic cross-section and SEM cross-section of such scheme.

Thin-film technology offers the advantage of high precision, low temperature, and low cost. As metal layers are added above passivation, one may also reduce the number of BEOL metals, thereby reducing costs. Further, the

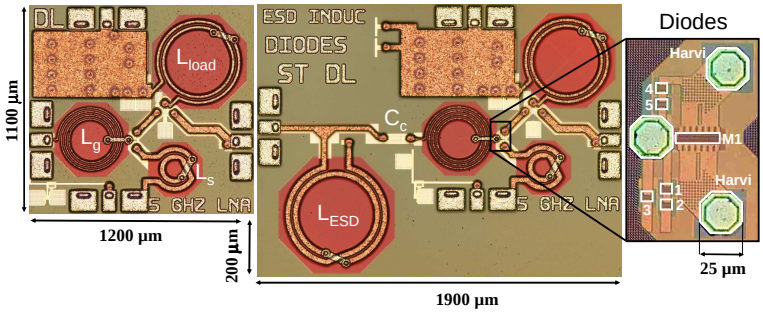

Figure 4.19: Micrograph of the reference LNA (left), ESD-protected LNA using Above-IC inductors with diodes (middle) and zoom on the additional clamping diodes (right).

process is compatible both with an Al BEOL and with a copper one. In [Carch 05], measured single-ended Q-factors above 40 are demonstrated for inductors realized on top of a five-levels-of-metal (5LM) Cu-oxide BEOL.

The same circuit as in Fig. 4.10 is used to evaluate the impact of the Above-IC inductors. Three versions of the LNA have been designed and implemented to evaluate both the RF and ESD performance. These are (a) LNA without ESD protection (LNA), (b) LNA with Above-IC inductor as ESD protection (ESD-LNA w/o diodes), and (c) LNA with both Above-IC inductor and clamping diodes as ESD protection (ESD-LNA with diodes). Fig. 4.19 shows the micrographs of the 'LNA' and 'ESD-LNA with diodes' using Above-IC. The layout of the 'ESD-LNA w/o diodes' is exactly the same as the 'ESD-LNA with diodes' except for the diodes shown at the right side of Fig. 4.19.

The LNAs are biased at a current of only 2 mA flowing through the LNA from a V_{DD} of 1.2 V. The power gains and input matching of the three LNAs are shown in Fig. 4.20, and the noise figure (NF) in Fig. 4.21. It can be seen that adding the "plug-and-play" ESD inductor only induces minor RF degradation, consisting of a decrease in S_{21} of 0.5 dB and a NF increase of 0.5 dB when compared to the LNA without ESD protection. Adding the additional clamping diodes adds another 0.2 dB to NF, and a gain decrease of 0.8 dB. Compared to normal BEOL, Above-IC inductors and interconnects yield a 4 dB improvement in gain, up to 0.7 dB decrease in NF, and a decrease in power consumption from 9 mW to 2.4 mW. Thus from RF circuit functionality point of view, the Above-IC inductors are advantageous compared to the BEOL inductors.

A summary of the ESD measurement results, stressing input to ground positively, is shown in Table 4.3. This shows that the Above-IC LNA with ESD inductor with clamping diodes has an ESD robustness of more than 8 kV of HBM and 1 kV MM at the RF input, which is a large improvement compared to normal BEOL, Table 4.2. For the BEOL ESD-LNA, the higher resistance

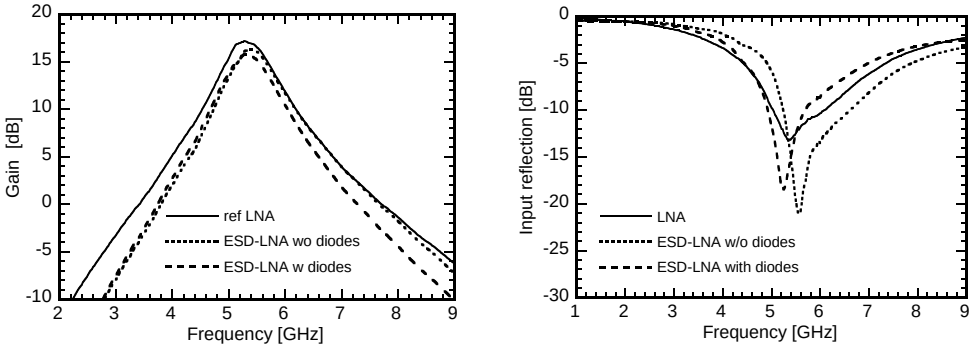

Figure 4.20: Measured gain (left) and input matching (right) of the reference LNA, ESD protected LNAs with and without clamping diodes, using Above-IC inductors.

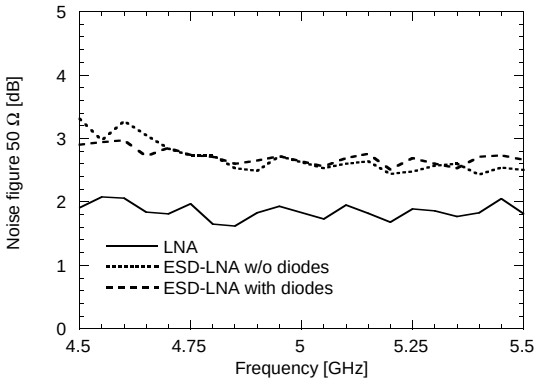

Figure 4.21: Measured 50 Ω noise figure (NF) of the reference LNA, ESD protected LNAs with and without clamping diodes, using Above-IC inductors.

of the inductor L_{ESD} (5.5 Ω compared to 0.6 Ω for Above-IC), results in a higher voltage overshoot at the RF input pin decreasing its ESD protection level. This is also visible in Fig. 4.22, where the measured 2 kV HBM voltage waveforms between input and ground on both the LNAs, using above-IC and BEOL inductors respectively, are superimposed.

4.4.3 VFTLP results

Despite the excellent HBM and MM results described earlier, the applicability of an inductor as ESD protection for CDM stress remains a big concern due to potential voltage overshoots, which is addressed in this section. In this section, VFTLP measurements have been performed on both normal BEOL and Above-IC LNAs with and without additional clamping diodes. The HBM and MM results of these circuits were summarized in Table 4.2 and Table 4.3 respectively.

Table 4.3: Summary of ESD measurement results for Above-IC processing, stressed input to ground.

Input to ground	**LNA**	**ESD-LNA w/o diodes**	**ESD-LNA with diodes**
HBM [kV]	0.009	6	>8
MM [V]	-	550	1k

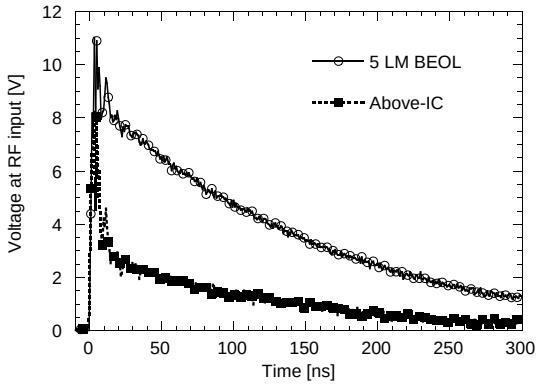

Figure 4.22: Measured voltage waveform during a 2 kV HBM pulse on the ESD protected LNA with 5 LM BEOL inductors and Above-IC inductors.

Since the gate oxide is more fragile when stressed in inversion rather than in accumulation, see Fig. 4.14, only positive stress between input and ground is considered. Even though other pin-to-pin ESD stress combinations might yield lower robustness, this can be restored by improving power clamp design and avoiding parasitic current paths in the core circuit.

The voltage overshoot across L_{ESD} during a fast transient ESD current was defined by (4.5). Very high voltages can be expected due to the fast, high current nature of the CDM pulse because the LdI/dt component cannot be neglected anymore. This voltage overshoot is coupled across the decoupling capacitor C_C (Fig. 4.10) and can cause internal circuit damage at the fragile gate oxide of transistor M_1 if not well understood and controlled.

The rise time of the VFTLP tester used is 200 ps, however this rise time is not seen at the device level. Probe needles were chosen for flexibility and cost reasons instead of RF-needles and their parasitic inductance lowers the rise time. The rise time reaching the device is around 400 ps, which is according to the CDM specification [CDM 08]. Fig. 4.23 shows VFTLP simulations of 2.3 A (around 200 V CDM of Class II [CDM 08]) with 3 ns pulse width and 400 ps rise time when stressing input positive to ground. This yields a maximum

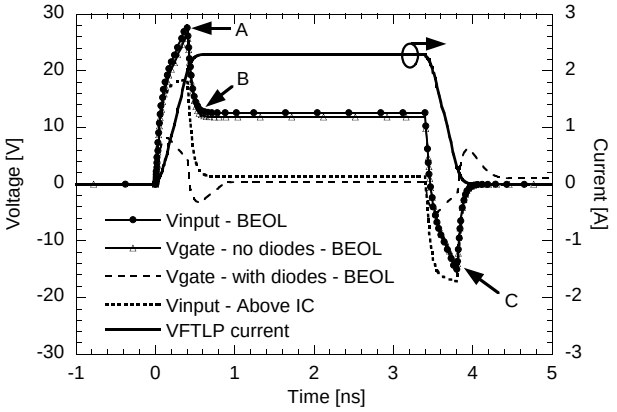

Figure 4.23: Simulated voltages during a 2.3 A VFTLP pulse of 400 ps rise time and 3 ns pulse width, with and without clamping diodes. The clamping diodes remove the voltage overshoot generated by the ESD inductor L_{ESD} at the gate.

peak voltage of 30 V for standard BEOL L_{ESD} (3 nH, R=5.5 Ω) at 400 ps (point A in Fig. 4.23). The positive dV/dt charges up the floating gate node according to the capacitive division between C_C and the capacitance of M_1, according to (4.6).

Since C_C is a large decoupling capacitor of about 2.3 pF and M_1 has a gate capacitance of around 150 fF, around 94% of the voltage overshoot is transmitted across C_C onto M_1 (V_{gate} - no diodes - BEOL, Fig. 4.23). When the VFTLP pulse reaches its stable region, dI/dt equals zero and the voltage drops down to $R * I$ (point B in Fig. 4.23) at the input, while the gate node follows according to (4.6). The latter voltage remains at the gate for the full duration of the VFTLP pulse width, after which a negative voltage spike (point C in Fig. 4.23) is measured when the VFTLP pulse switches off. The 90 nm gate oxide cannot withstand such voltage stress and fails already at 0.9 A (Table 4.4). More information on gate oxide reliability in the ESD time domain can be found in [Ille 06] and [Chen 07].

When using clamping diodes at the gate of M_1, the gate voltage is clamped to 7-8 V peak as seen in Fig. 4.23) (V_{gate} - with diodes - BEOL). Even though this peak voltage still causes gate oxide damage, by using clamping diodes the ESD robustness is improved, Table 4.4. However, this improvement was smaller than the factor of 3 expected by simulated results. The reason is due to the voltage overshoot of the STI defined diodes used here, which was not considered in the simulation. Further improvement is possible by changing the type of clamping diode from STI to poly defined. These poly defined diodes were found to have less voltage overshoot during ESD pulses than STI defined diodes as described in section 2.5.3 and thus should be used for voltage clamping, especially during

Table 4.4: Summary of VFTLP measurement results (200 ps rise time and 3 ns pulse width).

VFTLP RF_{IN}+ V_{SS}-	**Normal BEOL**	**Above-IC**
No clamping diodes	0.9 A	1.7 A
With clamping diodes	1.3 A	2.7 A

fast CDM events. The size of each clamping diode was 5x2 μm^2 yielding a parasitic capacitance of 11 fF. The influence of the clamping diodes on the RF performance was found to be marginal as described in the previous section. However, the ESD performance can be further increased by enlarging the clamping diodes at the expense of RF performance. It is preferred to take the diode parasitics into account during circuit design, and as such an optimal ESD-RF performance can be "co-designed".

Since L_{ESD} is the same, both for standard BEOL and for the Above-IC inductor, only the ohmic part of the voltage overshoot is reduced when using Above-IC. In Fig. 4.23, the decrease in voltage at the input pad can be observed when comparing Above-IC with standard BEOL. This results in a significant improvement up to 2.7 A as seen in Table 4.4.

These results indicate that an inductor to ground can be used as CDM protection element in combination with clamping diodes when high-quality inductors are available.

4.4.4 Overall comparison

In summary, Table 4.5 shows the comparison of all 90 nm CMOS LNA case studies investigated in this work, clearly showing the impact of various ESD protection strategies on the RF performance and the achieved ESD robustness.

4.5 Scaling Aspects of Inductor to Ground Approach

This section expands the inductor to ground strategy to several narrowband circuits (LNA and PA) operating at higher frequencies, ranging from 5 to 60 GHz implemented in a 45 nm planar or FinFET CMOS technology, with or without Above-IC. The ESD protection has been fully implemented by the RF-designers for each of their circuits based on our input, demonstrating the ease of implementation. It has been designed either as plug-and-play, or in a

Table 4.5: Comparison of RF and ESD performance of 90 nm CMOS LNAs with different ESD protection strategies.

Circuit	**LNA**	**ESD-LNA diodes**	**ESD-LNA codesign**	**ESD-LNA inductor w/o diodes**	**ESD-LNA inductor with diodes**	**LNA Above-IC**	**ESD-LNA Above-IC inductor w/o diodes**	**ESD-LNA Above-IC inductor with diodes**
V_{DD} [V]	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Current [mA]	7.5	7.5	7.5	7.5	7.5	2	2	2
Gain [dB]	13.5	13	16.2	12.6	12	16.5	16	15.2
S_{11} [dB]	-21	-18	-11.5	-18	-24	-12.5	-19.7	-12.5
S_{22} [dB]	-11	-14.5	-8	-14	-14	-11.6	-12.9	-13.2
S_{12} [dB]	-31	-30	-25.4	-32	-32	-28.4	-28.4	-28
NF [dB]	2.2	3	3.5	3.2	3.4	2	2.5	2.7
1dB CP [dBm]	-11.5	-10.6	-15.4	-10.5	-9.6	-23.2	-21.7	-20.2
IIP3 [dBm]	-1	-0.4	-5	-0.5	0.4	-17	-14	-13
TLP [A]	-	-	-	2.2	4	-	-	-
HBM [kV]	0.009	0.5	1.9	2.5	5.5	0.009	6	>8
MM [V]	-	-	-	225	350	-	550	1k
VFTLP [A]	-	-	-	0.9	1.3	-	1.7	2.7

codesign approach where the inductor has also been used to resonate out the pad capacitance.

The ESD performance of these circuits is investigated using both HBM and VFTLP measurements. The goal of this subsection is to see how the inductor to ground strategy is behaving under ESD conditions for applications in future technologies. For each circuit, references are included which discuss the RF performance results since these are beyond the scope of our work.

First, the inductor to ground methodology is demonstrated on 5 GHz LNA circuits implemented in 45 nm planar and FinFET CMOS technologies. Next, a 13 GHz LNA is protected in a 45 nm planar CMOS technology with Above-IC inductors. Finally, our methodology is applied to two 60 GHz circuits, namely a LNA and PA implemented in 45 nm planar CMOS technology with Above-IC and a digital backend, respectively.

4.5.1 5 GHz LNA in 45 nm planar and FinFET CMOS technology

Similar 5 GHz LNA circuits have been implemented both in a 45 nm planar and FinFET CMOS technology. First, classical dual diodes were used as ESD protection. When changing CMOS technology from bulk to SOI, the ESD robustness of active ESD protection devices, such as diodes and grounded gate NMOS, typically decreases. Besides the ESD performance, also the RF performance in terms of parasitic capacitance should be considered. As an example, [Junj 07] shows diode data in a 45 nm planar technology (It_2=32 mA/μm and C_{tot}=0.7 fF/μm) leading to a FOM It_2/C_{tot} of 46 mA/fF. This FOM decreases to 20 mA/fF in a 45 nm SOI technology according to [Junj 08] (It_2=8 mA/μm and C_{tot}=0.4 fF/μm). This results in a direct impact on circuit level. The ESD protection level decreases from 2.5 kV HBM for the planar version to only 850 V for the SOI FinFET version.

Secondly, an ESD inductor was placed at the RF input as plug-and-play, in combination with single-contact clamping diodes, according to Fig. 4.10. HBM measurement results show 5 kV for the planar LNA and 7 kV for the FinFET LNA. The increased robustness for the FinFET LNA can be attributed to the slightly wider metal tracks, and therefore lower resistance. These results indicate another strong aspect of the inductor to ground methodology. Namely, that the inductor-based ESD protection robustness is not dependendent on the front-end but mainly determined by the BEOL quality, which remains rather constant for the RF requirements.

VFTLP measurements show an unexpected low result, namely only 0.8 A for both the planar and FinFET LNA, which were attributed to failure of the single-contact sized clamping diodes. This should be easily solved by increasing

their size.

RF measurement results are discussed in [Borr 08] and show that when consuming similar power, FinFET LNAs achieve similar gain but worse noise, compared to the planar LNAs.

4.5.2 13 GHz LNA in 45 nm planar CMOS technology with Above-IC inductors

A LNA with inductor to ground type ESD protection was designed in a 45 nm planar bulk CMOS technology with Above-IC inductor, operating at 13 GHz. Single-contact sized (minimum design rule) clamping diodes were implemented. Due to the increased RF operating frequency, the required inductance of L_{ESD}, according to the RF-ESD trade-off discussed in section 4.1, is only 1 nH which reduces the inductive voltage overshoot (4.5) with a factor 3 compared to the 90 nm design example. The voltage overshoot (4.5) caused by the ohmic effect is also greatly reduced due to the use of Above-IC and the fact that inductors with lower inductance require fewer turns and wider metal tracks. Fig. 4.5 also indicates that less ESD signal will be coupled inside the RF circuit at this increased operating frequency.

This reduction in voltage overshoot directly translates into an improved HBM and VFTLP result. When stressing the RF input positively to ground, a robustness of 5 kV HBM and 2.9 A VFTLP was measured, complying with Class II CDM [CDM 08]. This result was obtained even with minimum sized clamping diodes, which did not fail as was the case in the previous example due to the reduced voltage overshoot. Further ESD improvement can still be obtained by increasing the diode size (limited by the allowed RF performance degradation) and by changing them from STI to faster poly defined diodes, as was discussed in section 2.5.3.

RF measurement results are shown in [Borr 08] for the circuit without ESD inductor. It is demonstrated that by using Above-IC, at 13 GHz a very low noise figure of 2.1 dB is achieved for just 5.3 mW power consumption.

4.5.3 60 GHz LNA in 45 nm planar CMOS technology with Above-IC inductors

Inductive ESD protection has been added as plug-and-play to a two-stage 60 GHz LNA using Above-IC microstrip lines in a 45 nm planar CMOS technology. Due to the high operating frequency, no clamping diodes were added. A power clamp is implemented as two series diodes in forward between V_{DD} and V_{SS} and one reverse diode for the opposite stress polarity. Due to the relative high power consumption of the RF circuit ($\sim$ mA), the leakage

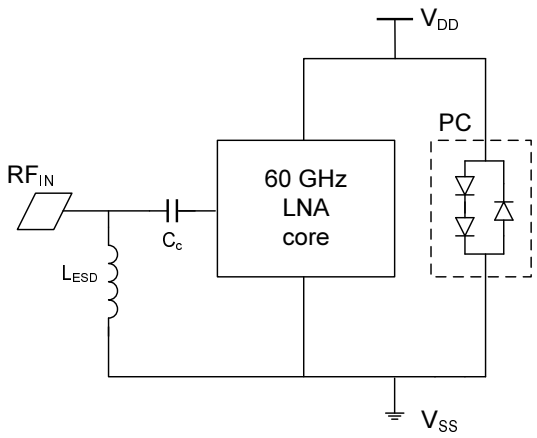

Figure 4.24: ESD protection schematic for the 60 GHz LNA.

current of the powerclamp can be neglected. The ESD protection schematic is shown in Fig. 4.24.

L_{ESD} has been designed as a $\lambda/4$ transmission line such that it transforms a short into an open at 60 GHz. A chip micrograph of the LNA is shown in Fig. 4.25 (left). In order to minimally impact the RF layout, the ESD protection was added outside of the bondpads. L_{ESD} shorts the RF input to ground and is implemented as a meander line. Due to such implementation, no under/over-pass is needed for the inductor, eliminating the need for via's, which are known to be the inductor weak spot during ESD stress, as was shown in section 4.4. The powerclamp is added on the top of the circuit, PC in Fig. 4.25.

HBM measurements between RF_{IN}+ and V_{SS}- were stopped at 8 kV due to tester limitations, without observing any failure. When stressing the weakest pin-combination, namely V_{DD}+RF_{IN}-, failure was noticed at 6.3 kV by a sudden leakage increase at the V_{DD} pad. Visually inspecting the LNA after this failure, Fig. 4.25 (right), reveals that the two Harvi's (A in Fig. 4.25) which connect the V_{DD} pad to the powerclamp diodes have blown open. As a consequence, the ESD current subsequently finds a way through the core circuit, which evidently also blows up (B in Fig. 4.25).

VFTLP measurements yield more than 10.6 A for stress between RF_{IN}+ and V_{SS}-, while 7.3 A was obtained between V_{DD}+ and RF_{IN}-. The fast VFTLP transients caused failure in the core of the LNA, and no Harvi damage was noticed during optical inspection of the LNA. A summary of the ESD measurement results is shown in Table 4.6, which nicely demonstrates the good scalability of the inductor solution.

S-parameters measurements of the ESD protected 60 GHz LNA are compared

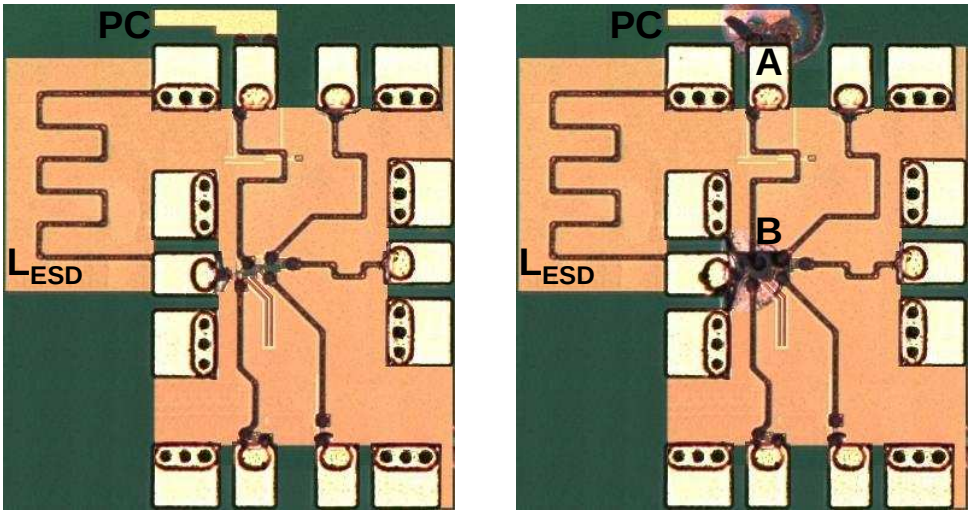

Figure 4.25: Micrograph of the 60 GHz LNA, before (left) and after (right) HBM stress between V_{DD}+ and V_{SS}-.

Table 4.6: ESD measurement results summary.

	$\boldsymbol{RF_{IN}}$+$\boldsymbol{V_{SS}}$-	$\boldsymbol{V_{DD}}$+$\boldsymbol{RF_{IN}}$-
HBM [kV]	>8 kV	6.3 kV
VFTLP [A]	>10.6 A	7.3 A

to the version without ESD protection in Fig. 4.26. A gain of 10 dB and input matching <-10 dB is obtained around 48 GHz, instead of the designed 60 GHz. This shift most likely can be attributed due to inaccurate microstrip models and technology variations. It is important to notice that the addition of L_{ESD} does not alter the input matching and even increases the gain a little.

Unfortunately, noise figure measurements could not be performed at this high operating frequency. However, only a negligible impact on the NF is expected according to (4.4). Due to the high-Q Above-IC $\lambda/4$ L_{ESD} and the high operating frequency of 60 GHz, F_{ESD} becomes very small. This makes this ESD protection methodology attractive in terms of both RF and ESD performance.

4.5.4 60 GHz PA in 45 nm planar digital CMOS technology

One of the building blocks of a transceiver is the PA which needs to supply enough energy for signal transmission. This subsection presents a 60 GHz PA implemented in a 45 nm digital low power CMOS technology. A digital

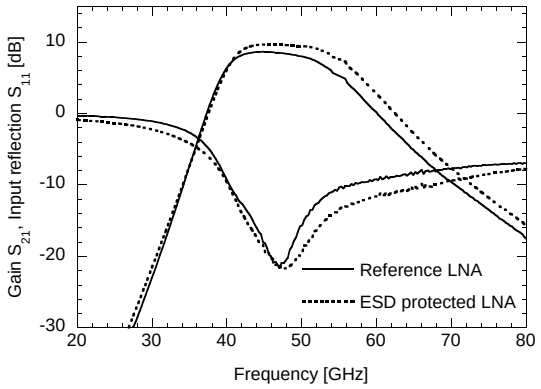

Figure 4.26: S-parameter measurements of the 60 GHz LNA, with and without ESD protection inductor.

technology was chosen since integration of the digital part together with the transceiver is beneficial for cost reasons. The main challenges of such RF design are the low-quality passives in digital CMOS technology, together with the limited power handling capabilities of downscaled CMOS. Since the PA drives an off-chip antenna, ESD protection is a must. Adequate ESD protection should not interfere with the 60 GHz RF operation, while it should protect the fragile 45 nm CMOS core transistors efficiently against the worst case CDM type of ESD stress.

The circuit schematic is shown in Fig. 4.27 and employs a two-stage common-source topology. Matching networks are provided at input, output and between the two stages. Since the PA will eventually be integrated with digital logic on the same chip, separate grounds were chosen for the RF-circuit (VSS_{CORE}) and the digital ground bus (VSS_{ESD}). This represents also worse ESD conditions rather then if only a single ground would have been used. Back-to-back ESD diodes are placed between these two grounds, see Fig. 4.27. ESD inductors are placed between the RF pins and VSS_{CORE}. Besides providing a low impedance ESD discharge path to ground, these ESD inductors are codesigned to be part of the RF matching network by tuning out the pad capacitance.

Almost no additional area is used by these ESD inductors (Fig. 4.28). Standard foundry power pads (RC-timed active clamp) are connected to the VSS_{ESD} ground bus around the RF core, which can be seen in Fig. 4.28 (left) together with a chip micrograph in Fig. 4.28 (right).

Separate biasing pads are foreseen for drain and gate of each transistor for tuning purposes. The second stage provides power amplification, while the first stage acts as a buffer. The design was optimized towards maximum output power and more RF design details can be found in [Racz 09], where also a similar differential push-pull configuration is discussed.

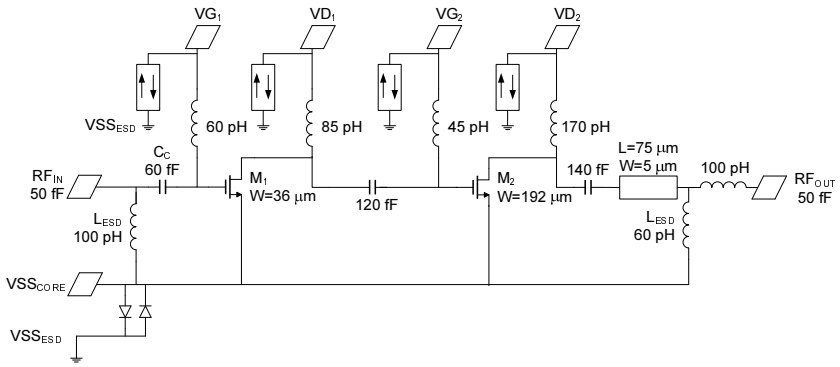

Figure 4.27: Schematic of the two-stage common source power amplifier.

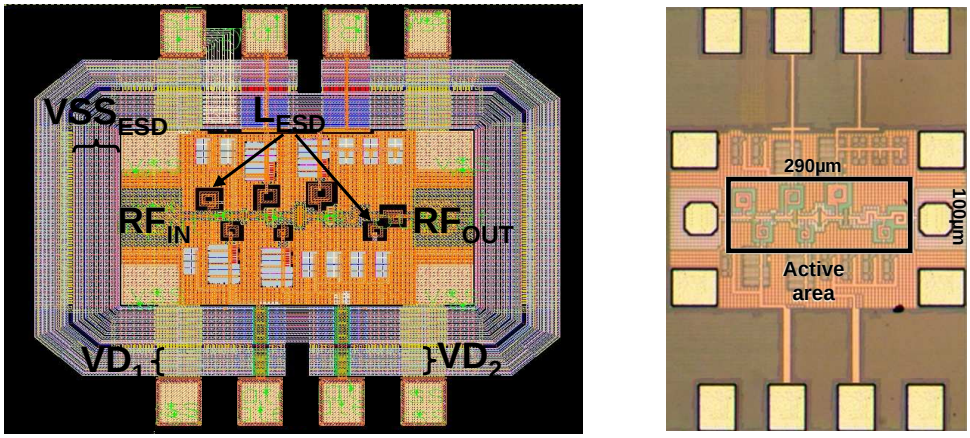

Figure 4.28: Cadence layout (left) indicating the separate ESD ground bus and corresponding micrograph (right).

RF measurements

S-parameter measurements show in Fig. 4.29 the input (S_{11}) and output (S_{22}) matching together with the small signal gain (S_{21}) which has a maximum of 5.8 dB at 52 GHz.

However, these are beyond the scope of this thesis.

ESD measurements

In the previous examples, inductor-based ESD protection was shown to protect efficiently against CDM when high-quality inductors are available in combination with clamping diodes, neither of which could be used for this design due to the digital BEOL and RF restrictions. In such a digital BEOL, no thick top metal is available for low resistive inductors.

VFTLP measurements have been performed using 3 ns pulse width and 400 ps

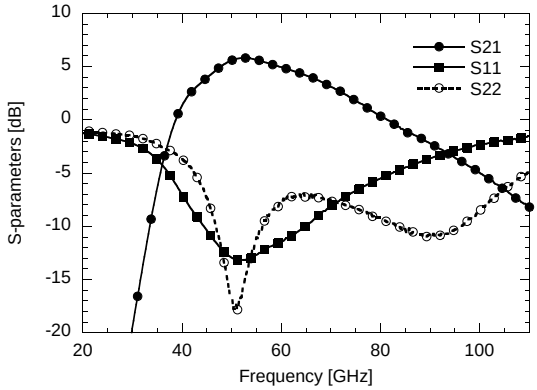

Figure 4.29: Measured small signal S-parameters of the PA.

rise time (measured at the DUT), which meets the CDM pulse specification given in the JEDEC standard [CDM 08]. When stressing RF_{IN} and RF_{OUT} separately versus VSS_{CORE}, measurements were stopped at 8.5 A VFTLP, due to limited amount of samples, without observing failure in both cases. Failure was monitored by DC measurements after each VFLTP pulse between VD_1 and VSS_{CORE} for stress at RF_{IN}, and between VD_2 and VSS_{CORE} for RF_{OUT} (Fig. 4.27). This failure level of >8.5 A corresponds roughly to >765 V CDM for small packages (Class C4 [CDM 99]). Stressing RF_{IN}/RF_{OUT} to VSS_{ESD} yields the same result of >8.5 A as the voltage stress on the transistors does not depend on the additional diode voltage drop between VSS_{CORE} and VSS_{ESD} since both source and bulk of the core transistors are tied to VSS_{CORE}. Typically, failure is observed at the gate oxide of transistor M_1 during VFTLP stress at the RF_{IN} pin, due to voltage overshoots. However, this high VFTLP robustness can be attributed to five elements:

1. The 60 GHz RF operating frequency allows for a smaller L_{ESD} at RF_{IN} of only 100 pH and associated lower parasitic resistance R_{ESD} of 1.8 Ω. The generated voltage overshoot during 8.5 A VFTLP across the inductor is 17.4 V according to (4.5).
2. According to (4.6) with C_C=60 fF and C_{M1}=50 fF, the voltage which would be coupled from RF_{IN} onto the gate of transistor M_1 would be reduced to 9.5 V because of the small decoupling capacitor C_C . This 9.5 V peak value would still cause gate oxide breakdown of M_1, which is around 4 V and therefore additional voltage clamping is needed.
3. This voltage clamping at the gate of M_1 is achieved by the active MOS power clamp at pad VG_1. This power clamp is connected to the gate of M_1 through a 60 pH, making it invisible for the 60 GHz RF-signal. Even though in a real product the bias voltage VG_1 will be derived internally, placing such power clamp connected through an appropriate inductor will always be feasible and advised. Otherwise, using the gate

oxide failure voltage of 4 V for M_1, a failure current of only 3.5 A can be estimated according to (4.5) and (4.6), compared to >8.5 A with additional inductor and power clamp. Note that this additional power clamp has the same voltage clamping function as the clamping diodes shown in Fig. 4.10.

4. In case of RF_{OUT}, the drain-junction of M_2 has to be protected instead of its gate, increasing the allowed voltage overshoots.
5. Metal-Oxide-Metal (MOM) capacitors were used instead of Metal-Insulator-Metal (MIM) capacitors because MIMs were not available in the digital BEOL. Such MOM-type of capacitor is more robust than MIM due to the thicker Inter-Metal Dielectric (IMD) layer compared to the MIM insulator layer.

Since the inductor-to-ground methodology always requires a serial input capacitance (C_C), its impact on the performance of RFCMOS ICs should be highlighted. Ideally, the decoupling capacitor C_C should be as large as possible to remain invisible for the RF signal. However, the bigger the capacitance is, the lower is its resonance frequency, puting a maximum boundary at the capacitance value. Since the resonance frequency of the 60 fF capacitance is somewhat >100 GHz, it can be used for 60 GHz operation. However, it is required to take this capacitance into account during the design of the input matching network. The ESD inductor adds another degree of freedom which can be used to tune out the remaining capacitances, including the bondpad capacitance, resulting in a very good input matching as seen in Fig. 4.29.

Since the voltage overshoot is not an issue, additional HBM measurements were performed to apply ESD stress with more severe power content. For the same pin combination as VFTLP, circuit failure is due to the ESD inductors both for RF_{IN} and RF_{OUT}. They fail during HBM to an open due to melting of the tracks at 5.3 kV, see Fig. 4.30. Subsequently the MOM capacitor fails.

When stressing VD_1 to VSS_{ESD}, >8.5 A VFTLP and 5 kV HBM is measured. However, when stressing to VSS_{CORE}, only 4.4 A VFTLP is reached and 3 kV HBM. This indicates a parasitic current path through the core transistor M_1 next to the intended ESD path through the power clamp. The gate of M_1 is floating and gate coupling can induce MOS current. Eventually, bipolar current will flow when breakdown of the drain-substrate junction is reached. In case of stress to VSS_{ESD}, the power clamp is competing with M_1 in series with a diode. However, when stressing VD_1 to VSS_{CORE}, the diode switches sides and is now in the ESD current path and removed from the parasitic core path. Therefore, more current will flow through M_1, explaining the reduced robustness for stress to VSS_{CORE}.

When stressing VD_1 versus RF_{IN}, the ESD current has to travel first to VSS_{CORE} via the power clamp and then through L_{ESD} to RF_{IN}. Even though the drain to source voltage of the core transistor remains unaltered

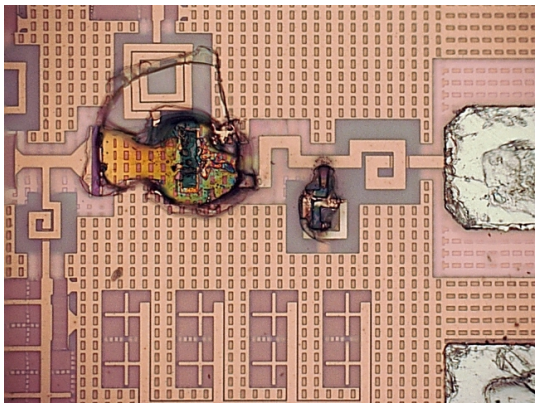

Figure 4.30: Micrograph showing the failed ESD inductor at the output and subsequently the blown-up MOM capacitor during HBM stress.

compared to stress to VSS_{CORE}, a decrease in HBM robustness is measured, which most likely can be related to different gate bias conditions of the core transistor. The transient coupled gate voltage is lower when stressing to RF_{IN} than when stressing to VSS_{CORE}, due to larger capacitances from gate to RF_{IN}. A larger gate bias is known to improve uniform triggering of the lateral n-p-n, also for fully silicided transistors [Duvv 92].

In case of stress between VD_2 and VSS_{CORE}/VSS_{ESD}, the parasitic path through core transistor M_2 is strengthened due to its increased size compared to M_1. This directly results in an improved VFTLP robustness to VSS_{CORE} of >8.5 A and HBM robustness of >6.5 kV to VSS_{ESD} and 4.5 kV to VSS_{CORE}. The reverse polarity to VSS_{CORE} fails at 5.5 kV. For this stress combination, the intended ESD path consisting of two series diodes is competing with the substrate-drain diode in M_2 in series with an inductor. Most likely the inductor is the limiting element.

An overview of the different measured pin-to-pin combinations for both VFTLP and HBM are shown in Table 4.7 and Table 4.8, respectively. Weak spots are indicated by shaded areas.

VD_1 and VD_2 were separated in this testchip for measurement and tuning flexibility. However, in a real product, both VD_1 and VD_2 will be connected to a single V_{DD} pad, and hence M_1 and M_2 could work in parallel (depending on various parisitic elements). This would then restore the overall ESD robustness of the weak spots.

For this circuit, a first time right design was achieved, both in terms of RF and ESD performance. No additional silicon run was needed for ESD optimization, indicating the ease of implementation for an RF designer.

Table 4.7: VFTLP measurement results [A] for different pin-to-pin combinations. Weak spots are highlighted.

+/-	RF_{OUT}	RF_{IN}	VD_1	VD_2	VSS_{CORE}	VSS_{ESD}
RF_{OUT}			>8.5	>8.5	>8.5	>8.5
RF_{IN}					>8.5	>8.5
VD_1		4.3			4.4	>8.5
VD_2	>8.5	>8.5			>8.5	>8.5
VSS_{CORE}						
VSS_{ESD}				>8.5		

Table 4.8: HBM measurement results [kV] for different pin-to-pin combinations. Weak spots are highlighted.

+/-	RF_{OUT}	RF_{IN}	VD_1	VD_2	VSS_{CORE}	VSS_{ESD}
RF_{OUT}					5.3	5.3
RF_{IN}					5.3	5.3
VD_1		2			3	5
VD_2	4	3.8			4.5	>6.5
VSS_{CORE}				5.5		>8
VSS_{ESD}					>8	

4.5.5 Discussion

Using the inductor to ground approach, very high ESD protection levels have been demonstrated. Therefore, in order to further optimize this plug-and-play concept, a larger L_{ESD} can be selected (e.g., 5 nH instead of 3 nH for the 5 GHz LNA). This will improve the RF performance by reducing the impact of the ESD-protection, see Fig. 4.12 (right). Although the higher series resistance of the inductor (longer metal tracks in the inductor) will degrade the ESD robustness of the LNA, adding clamping diodes (D1-D3) at the gate of M_1, described before, can still provide adequate ESD robustness. The ESD protection should be designed to reach the ESD protection targets (both HBM and CDM) with the best possible RF performance.

Besides using the plug-and-play approach, the ESD inductor can also be used to tune-out any remaining parasitic capacitance, such as the bondpad capacitance. As such, the inductor dimensioning can be taken into account during the RF design, resulting in a codesign approach.

The clamping diodes, used to increase the ESD protection level by shifting the

failure mode from oxide breakdown of M_1 to failure of the MIM capacitance C_C, were chosen 5x2 μm^2 wide and they can withstand 360 mA TLP stress (72 mA/μm). Simulation results indicate that the additional diodes are only required to conduct 10 mA for a 5 kV HBM pulse on the BEOL ESD-LNA [Thijs 06]. This means that theoretically the diode size can even be reduced to minimum size. Such diodes will not introduce any RF performance degradation, yet provide the additional ESD protection. However, enough safety margin has to be taken to ensure that these minimum sized diodes do not fail themselves during the transient stress.

As the operating frequencies of the RF circuits continue to increase, the RF and ESD frequency spectrum get more and more clearly separated. Hence, lower value inductors can be used as protection element, needing fewer turns (smaller area), and thus lowering the series resistance. As both the LdI/dt and the $R * I$ component in (4.5) decrease, not only the HBM, but also the CDM performance will improve a lot. Eventually, when the operating frequency is high enough, the ESD inductor can be implemented as a simple microstrip line shortening input to ground ($\lambda/4$ line). In this way, all ESD stress is deviated away from the core, with the lowest possible inductance and on-resistance while letting the RF signal pass into the circuit. Also the area consumed by the ESD protection is then greatly reduced.

By using an ESD protection inductor, the scaling limitations of "classical" ESD concepts have been overcome, yielding a solution with no scaling limits.

4.6 Transformer Based Methodology

To avoid the area penalty introduced by L_{ESD}, the ESD inductor can be shifted underneath the gate matching inductor L_G and hence a transformer based ESD protection circuit is created as shown in Fig. 4.31. At first glance, it can be understood that the input transformer consisting of a primary coil L_1 and secondary L_2 can be used in the resonant input matching. The high-order equivalent network can be used for either narrowband or wideband input matching. Such protection technique has the drawback that the transformer needs to be designed together with the RF design and therefore is not plug-and-play anymore.

In the case of an ESD event, the primary winding of the transformer, L_1, sinks the current. The galvanic seperation, which is realized between the input and the gate of the transistor heavily attenuates the possible residual voltage overshoot at the input for the ESD frequency range, and thus increases the protection level. To further increase the ESD robustness, additional voltage clamping diodes can be implemented the same way as in section 4.4, see Fig. 4.31. This figure also shows the power clamp consisting of three

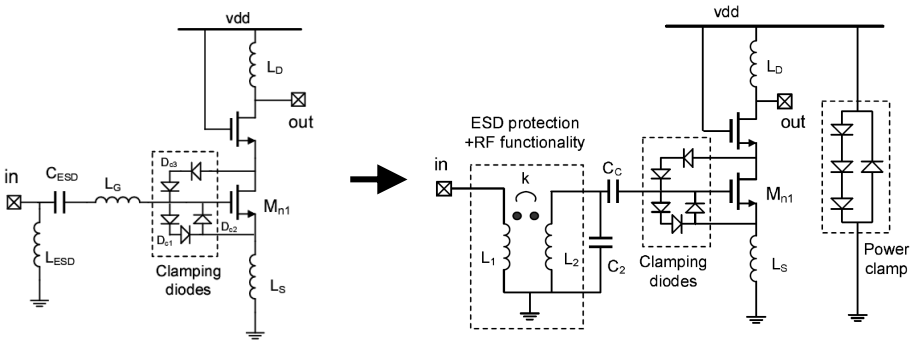

Figure 4.31: Inductor-based ESD protection (left) and transformer-based ESD protection (right).

series diodes and one reverse diode to complete the ESD protection of the LNA. Diodes have been chosen for their simplicity and their availability and compatibility in any technology.

To increase design freedom, it is interesting to enable capacitance and inductance selection, regardless of the input transistor's parameters. In that case, input matching and noise matching of the LNA are decoupled, and the device and passives can be designed to optimize both. The extra capacitance C_2 is used to achieve this freedom, see Fig. 4.31. Now, the resonance frequency can be lowered for a relatively small inductor L_1 by increasing C_2, which benefits both area and noise. Furthermore, C_2 can be modified independently from the transistor's width and overdrive, allowing a dedicated power-noise optimization. The complete RF design details can be found in [Borr 07].

The circuit has been designed for 5-6 GHz operation in a 0.13 μm CMOS technology. During design a trade-off has been made between noise degradation, minimum resistance in the ESD path, and acceptable power consumption. The transformer has been designed using ASITIC [ASITIC] and verified with HFSS 3D ElectroMagnetic field simulation [HFSS]. Designing the transformer (Fig. 4.32) as two inductors on top of each other eases the desired turn ratio n selection. A turn ratio n of 1.6 and a coupling factor k of 0.82 are achieved. The secondary inductor is designed in the lowest resistance metal layer (M8: top metal) with an aluminum (Al) overpass. The primary inductor (lowest number of turns) is drawn in metal 7 (M7) with M6 underpass. Its tracks are wider for low parasitic resistance and to achieve a similar resonance frequency as the secondary. As will be shown by the ESD measurements, the transformer-based ESD protection methodology can reach very high HBM and VFTLP robustness. Therefore, from the RF-ESD co-design point of view, it is wiser to optimize the RF behavior. Due to noise considerations, the primary inductor should be implemented in the second best metal layer as explained in [Borr 07]. Fig. 4.33

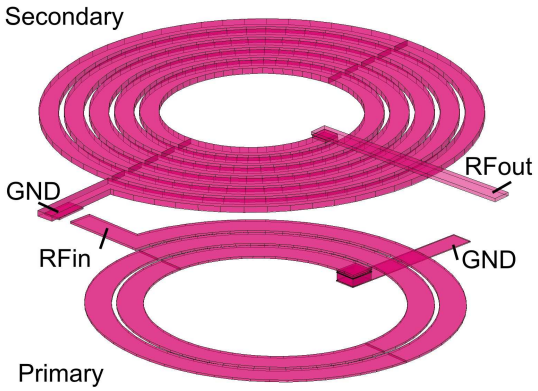

Figure 4.32: Transformer geometry.

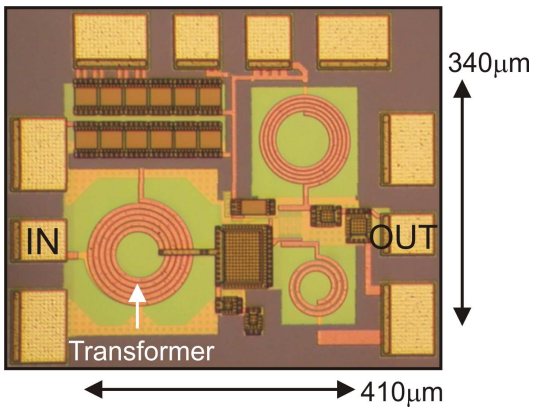

Figure 4.33: Chip micrograph.

shows a chip micrograph where no additional area is required for the ESD inductor, as opposed to Fig. 4.16.

S-parameters have been measured on wafer for the LNA with and without clamping diodes, showing nearly no difference between both, Fig. 4.34 (left). A peak power gain of 14.8 dB is achieved with an adequate input match from 4.5 to 7 GHz, drawing 5.6 mA from a 1.2 V supply voltage. The 3 dB bandwidth ranges from 4.6 to 6 GHz, and is determined dominantly by the Q-factor of the load. Unlike the S-parameters, the noise figure is slightly deteriorated due to the clamping diodes, Fig. 4.34 (right), especially at higher frequencies. While the LNA without diodes has a minimum NF of 2.4 dB, the clamping diodes add 0.3 dB on the average.

An HBM robustness of 4.5 kV is measured at the RF input, which is increased to at least 7.3 kV by addition of the voltage clamping diodes. This robustness is achieved on all pin-to-pin combinations. A summary of the HBM results is

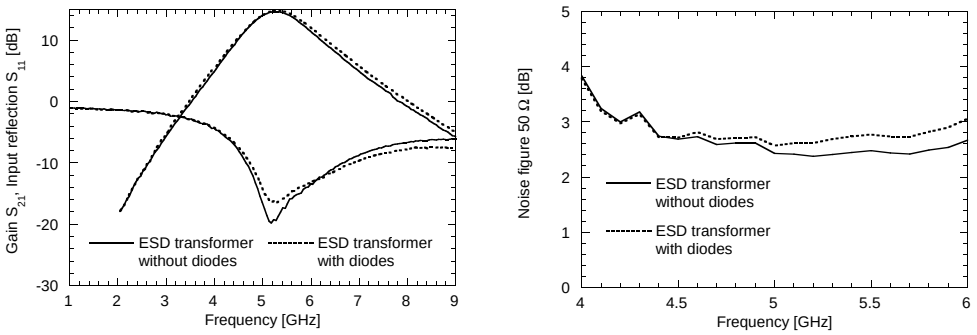

Figure 4.34: Gain and S_{11} (left), and noise figure (right) of the transformer-based ESD protected LNA with and without additional clamping diodes at the input nMOS gate. The impact on the RF performance of the diodes is marginal.

Table 4.9: Summary of HBM measurement results with and without additional clamping diodes.

HBM [kV]	**No diodes**	**With diodes**
$\boldsymbol{RF_{IN}+V_{SS}}$-	4.5	7.3
$\boldsymbol{V_{SS}+RF_{IN}}$-	4.6	>8
$\boldsymbol{RF_{IN}+V_{DD}}$-	-	7.3
$\boldsymbol{V_{DD}+RF_{IN}}$-	-	7.3
$\boldsymbol{V_{DD}+V_{SS}}$-	-	>8
$\boldsymbol{V_{SS}+V_{DD}}$-	-	>8

shown in Table 4.9.

Since an inductive component is used as ESD protection element, special attention needs to be paid to its behavior under CDM stress. The CDM robustness is assessed by means of VFTLP measurements. At the RF-input, a VFTLP robustness of 3.2 A has been measured. Clamping diodes increase this robustness to 5 A. The VFTLP measurements were done with 200 ps rise time and 3 ns pulse width. The failure mechanism has been attributed to oxide breakdown of the input device M_1. The observed VFTLP robustness roughly corresponds to a CDM value of 300 V, as this is known to depend also on the package. These are very high results compared to the 1.3 A VFTLP achieved using the inductor to ground methodology. This improvement cannot be attributed only to the use of a 130 nm CMOS technology and hence a deeper study of the behavior of the transformer under VFTLP stress is needed. L_1 is the inductor of the transformer at the input pad and L_2 is the inductor near the core circuit as seen in Fig. 4.31. R_1 and R_2 are their parasitic resistances (not

indicated in the figure) and I_1 and I_2 the currents through them respectively. The voltage overshoot at the RF input pad V_{input} is equal to:

$$V_{input} = L_1 \frac{dI_1}{dt} + R_1 I_1 + M \frac{dI_2}{dt} \tag{4.7}$$

$$M = k\sqrt{L_1 L_2} = nL_1 \tag{4.8}$$

where M is the mutual inductance, k the coupling factor and n the turn ratio of the transformer. I_1 equals the ESD current while I_2 is only in the order of mA due to the presence of the MIM decoupling capacitor and gate oxide of M_1. Therefore, the last term can be neglected in (4.7) with respect to the first. The voltage right after the transformer V_{trafo} is calculated using:

$$V_{trafo} = nL_1 \frac{dI_1}{dt} + L_2 \frac{dI_2}{dt} + R_2 I_2 \tag{4.9}$$

From (4.9), it can be seen that V_{trafo} only depends on the transient current through L_1 since the last two terms can be neglected. The inductive overshoot voltage at the input pad is up-converted with a factor n after the transformer. For this application, n and k are respectively 1.6 and 0.82 as indicated earlier.

For HBM, due to the relative slow rise time (small dI/dt), the voltage overshoot is dominated by $R * I$. Since only the inductive part is coupled across the transformer, the voltage after the transformer is much smaller than at the input pad. However, for VFTLP, dI/dt is dominant for the voltage overshoot, which is then up-converted across the transformer. This results in V_{trafo} being larger than V_{input}, as shown in Fig. 4.35. The inductor L_1 which has to ground the ESD current, has an inductance value of 0.8 nH [Borr 07] and despite the voltage up-conversion, the voltage overshoot is still lower than in the case of the 3 nH inductor to ground, which was used in section 4.4. Fig. 4.35 shows the different simulated voltages during 3 A VFTLP stress conditions. The simulated rise time was 400 ps, which is expected to reach the circuit instead of the 200 ps tester rise time due to the system parasitics, section 2.5.2. It is also important to notice that V_{trafo} is independent of both the parasitic resistances R_1 and R_2 of L_1 and L_2, according to (4.9) with the last two terms neglected, meaning that for the transformer-based ESD protection above-IC is not expected to improve the CDM robustness.

Interestingly, (4.9) yields also another important benefit of the use of the transformer for VFTLP. When dI_1/dt equals zero, namely after the rising part of the VFTLP pulse, the full voltage after the transformer V_{trafo} drops to zero

Table 4.10: Summary of VFTLP measurement results (200 ps rise time and 3 ns pulse width) with and without additional clamping diodes.

VFTLP [A]	**No diodes**	**With diodes**
$\boldsymbol{RF_{IN}+V_{SS}}$-	3.2	5
$\boldsymbol{V_{SS}+RF_{IN}}$-	3.6	5.4

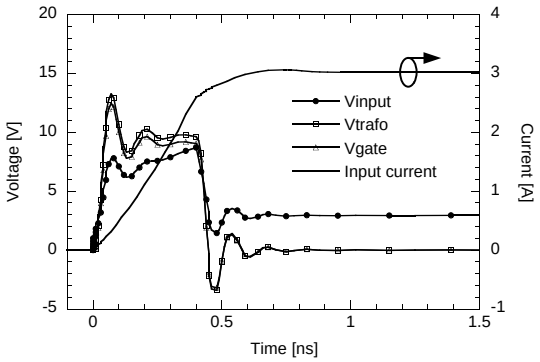

Figure 4.35: Simulated voltages during a 3 A VFTLP pulse of 400 ps rise time and 3 ns pulse width for the ideal transformer ESD protection. No clamping diodes were present.

as can be seen in Fig. 4.35, and consecutively also the voltage at the gate of transistor M_1 (according to (4.6) with V_{trafo} instead of V_{input}). Note that in the case of CDM, there will always be a dI/dt component present.

When comparing Fig. 4.23 and Fig. 4.35, in the case of a transformer based ESD protection, the voltage stress at the gate is only present during the transient part of the VFTLP pulse, i.e. during 400 ps, whereas in the case of the inductor to ground, the stress is present during the full 3 ns of the VFTLP pulse. This reduction in voltage stress time is a significant benefit for the transformer based ESD protection solution compared to the inductor to ground as shown by the excellent VFTLP measurement results in Table 4.10.

An overview of both the RF and ESD performance of the transformer-based ESD protection compared to plug-and-play inductor to ground is shown in Table 4.11. The benefit of the transformer-based ESD protection solution is the increased VFTLP robustness and the zero area consumption. These come at the cost of increased design complexity.

Table 4.11: Comparison RF and ESD performance between inductor to ground and transformer based. Both designs have additional clamping diodes.

	Transformer based	**Inductor to ground**
Technology [CMOS]	0.13 μm	90 nm
f_C [GHz]	5.5	5
Power [mW]	6.6	9
Gain [dB]	12.4	12
NF [dB]	2.6	3.4
Approx. area [mm^2]	0.14	$\sim$0.8
HBM [kV]	7.3	5.5
VFTLP [A]	5	1.3

4.7 State-of-the-Art Comparison

Very few ESD protected narrowband RF designs exist which are implemented in advanced CMOS (90 nm or below). The inductor to ground methodology has been benchmarked to other RF-ESD protection methodologies in [PhDLinten], which were implemented in 0.5-0.18 μm CMOS. Our approach, implemented in 90 nm and 45 nm CMOS technology was found to yield the highest overall RF-ESD performance. In Table 4.11, the transformer based solution (0.13 μm CMOS) has been compared to the inductor to ground approach (90 nm CMOS), yielding improved RF and ESD performance at the expense of increased design complexity. Several examples were given for the inductor to ground methodology in 45 nm CMOS technology. The RF operating frequency has been increased up to 60 GHz, leading to excellent RF performance, ESD performance (both HBM and VFTLP) and small area occupation. Only two comparing ESD protected RF circuits at 60 GHz were found in literature and are discussed below.

Regular ESD protection diodes in combination with an RC power clamp for a 60 GHz LNA are incorporated in [Borr 09] which is implemented in 45 nm digital CMOS. This ESD protection results in 1.2 kV HBM between worst-case pin-to-pin combination RF_{IN}+ V_{SS}-. The RF penalty is a large 2 dB increase in NF which in many cases is untolerable. Since no decoupling capacitor C_C is present as in Fig. 4.24, any voltage transients during VFTLP testing will directly stress the gate oxide of the input transistor and hence rather low VFTLP robustness is expected.

In [Huang 09], a 60 GHz LNA in 0.13 μm CMOS technology is reported using the impedance-isolation technique [Ker 03] as ESD protection, which adds

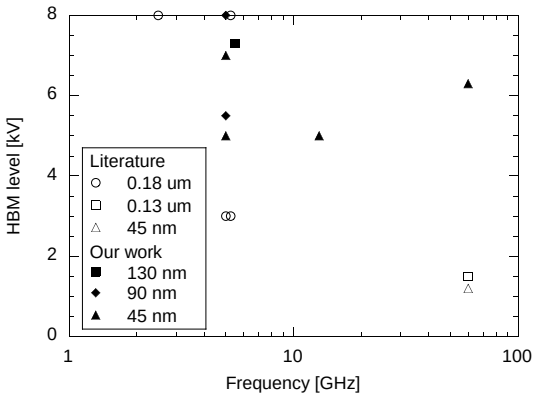

Figure 4.36: Benchmarking of our work (solid symbols) against other published results (open symbols). The HBM robustness [kV] is plotted as function of RF frequency [GHz].

1.5 dB in NF. In this protection methodology, the parasitic capacitance of the ESD protection diode is cancelled out using an LC-tank. The LNA core fails at 1.5 kV HBM robustness, which is lower than the 6.5 kV ESD diode robustness indicating core failure due to voltage overshoots. As no decoupling capacitance C_C is present, the voltage overshoot will be fully coupled onto the fragile gate oxide. When using this protection methodology in a 45 nm CMOS technology, even lower ESD robustness is expected due to the lower gate oxide breakdown voltage. No VFTLP results were published but they are expected to be very low since catastrophic voltage overshoots were already observed during HBM stress. Therefore, this method is considered not to be a valid candidate for CDM protected RF circuits.

In Fig. 4.36, a graphical overview is given, where the results of our ESD protected narrowband CMOS LNAs are benchmarked against literature. A few results in 0.18 μm CMOS are included as well. We achieved the highest HBM robustness levels for the highest frequencies in the most advanced CMOS technologies in the world. Note that a similar comparison regarding VFTLP measurements is not possible since nobody else has published such results.

4.8 Conclusions

In this chapter, first the scaling limitations of the classical dual diode were demonstrated using a 90 nm narrowband 5 GHz CMOS LNA as demonstrator. This "plug-and-play" dual diode approach can be used up to 5 GHz. A codesign approach was presented as an alternative solution where the ESD protection was integrated into the RF design. By codesigning the low-capacitive ESD

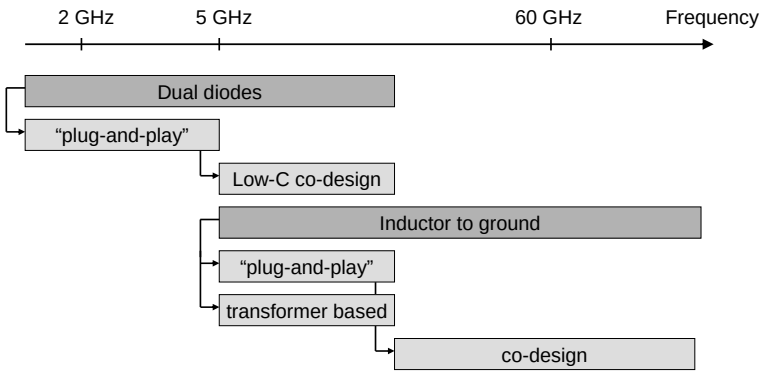

Figure 4.37: Narrowband RF-ESD protection methodology as function of application frequency.

protection devices into the RF design, their use can be extended to higher frequencies, however with limited ESD robustness.

Inductive ESD protection was investigated for RF circuits with frequencies of 5 GHz and above. Two different inductor-based ESD protection methodologies, namely inductor to ground and transformer-based, were studied for their impact on HBM and CDM robustness of narrowband RF circuits. Specifically CDM protection is a challenge due to occuring voltage overshoots over the inductive ESD protection elements. For the first time, VFTLP measurements were performed on RF circuits, which is crucial to predict CDM robustness. Analysis of the transient voltage response revealed the benefits of transformer-based protection. Using an Above-IC inductor or a transformer as well as additional clamping diodes yields both excellent HBM, MM and TLP results, as well as very high VFTLP results. This robustness was further improved by optimizing the diode type and size, making the inductor-based ESD protection methodology efficient against CDM stress.

When changing from bulk CMOS technology to SOI, the ESD robustness of active ESD protection devices typically decreases, which makes low-capacitance based RF-ESD solutions less efficient. However, inductor-based ESD protection robustness is mainly determined by the BEOL quality, which remains rather constant for the RF requirements. The future scaling possibilities of the inductor to ground approach were demonstrated in 45 nm planar and FinFET CMOS technologies, up to RF frequencies of 60 GHz. At these frequencies, less ESD signal couples into the RF circuit and due to the decreased inductance of the inductor to ground, less voltage overshoot is present. Therefore, with increasing frequency, the inductor to ground methodology becomes better in terms of RF performance, ESD performance and area consumption, yielding world-record results.

By an increased design effort, the inductor to ground methodology can be changed into a transformer based protection scheme with decreased area consumption and improved ESD robustness. However, given the excellent RF and ESD performance of the "plug-and-play" inductor to ground for circuits with increased operating frequency, the inductor to ground methodology is preferred over the transformer based solution because of the reduced design complexity. Integration of the inductor to ground methodology is straightforward for an RF designer since the impact on the RF performance can easily be simulated. The ESD inductor can even be used to tune out any remaining parasitic capacitance in a codesign approach. Therefore, using an inductor to ground is an excellent candidate for ESD protection for narrowband mm-wave applications.

A graphical overview of the different narrowband RF-ESD protection strategies is given in Fig. 4.37 as function of application frequency.

Chapter 5

ESD Protection for Wideband RF CMOS Circuits

As wideband RF circuits are getting implemented in CMOS, there is a need for adequate ESD protection for these circuits. Current solutions are either limited in terms of RF performance, power consumption, ESD performance and/or area consumption. In this work we present a novel T-diode-based solution as an excellent plug-and-play candidate yielding both excellent RF and ESD performance using limited amount of area. For extreme wideband Distributed Amplifiers (DA), a Center Balanced Distributed ESD (CBDESD) protection is proposed without the need for redesign of each gain stage.

5.1 Introduction

Wireless communications are expanding with increasing number of application standards such as Wireless Local Access Network (WLAN), Ultra WideBand (UWB), Wideband Code Division Multiple Access (WCDMA), etc., all operating at different carrier frequencies. This results in an increasing interest in the realization of multi-standard transceivers in mainstream CMOS technologies. One possible realization is a Software-Defined Wireless Receiver [Bagh 06], where the entire available signal band is received at the input of one wideband RF LNA.

Such a wideband RF LNA needs ESD protection at its RF input pin, while maintaining adequate input matching over the entire operating frequency band. Narrowband cancellation techniques as discussed in the previous chapter, cannot be used as they only provide input matching around a certain frequency and not over a wide band.

In this chapter, we propose two ESD solutions for wideband RF applications. First, in section 5.2, the concept "T-diode" is introduced as a candidate for plug-and-play ESD protection for wideband circuits. In addition, a generic methodology is demonstrated on the T-diode to prevent circuit failure due to parasitic current paths inside the core circuit. This methodology is also widely applicable for narrowband RF circuits, and even for any other type of circuit. Secondly, a distributed ESD concept called Center Balanced Distributed ESD protection (CB-DESD) is implemented for a DA in section 5.3. Finally in section 5.4 a comparison is made with the state-of-the-art publications on ESD protected wideband RF circuits.

5.2 T-diodes

This section introduces a novel "plug-and-play" "T-diode" ESD protection methodology for wideband RF circuits, consisting of an integrated transformer and ESD diodes. The technique requires no additional power consumption, and maintains the full RF bandwidth.

First, the T-diode design methodology is discussed in section 5.2.1. Section 5.2.2 and section 5.2.3 present two design examples implemented in a 0.18 μm and a 90 nm CMOS technology respectively. RF and ESD results are discussed in detail. Finally, a general method to avoid triggering of parasitic current paths in the functional core circuit during ESD stress is described in section 5.2.4.

5.2.1 T-diode design methodology

An ESD protection circuit for a wideband RF amplifier needs to maintain a good input matching of the amplifier over its entire bandwidth.

The classical dual-diode ESD protection, as shown in Fig. 5.1 (left), is rather unsuitable for protecting the input of a wideband RF amplifier, as the total capacitive load added by the diodes D_1 and D_2 (C_D) deteriorates the input impedance reducing the overall bandwidth of the amplifier [Sold 05]. For example a 2x230 fF capacitive ESD load has an impedance of 346 Ω at 1 GHz, 69 Ω at 5 GHz, and 45 Ω at 10 GHz. When placed in parallel with the 50 Ω input impedance of the amplifier, the overall input matching is considerably lowered, and hence degraded.

A method to overcome this bandwidth limiting problem is proposed, referred to as T-diodes (transformer plus diodes), which use two coupled inductors L_1, L_2, and a capacitor C_c in Fig. 5.1 (right). Together with the capacitances of diode D_1 and D_2 (C_D) at the specific LNA bias voltage used, the structure closely approximates a lossless transmission line [Horng 03] as shown in Fig. 5.2.

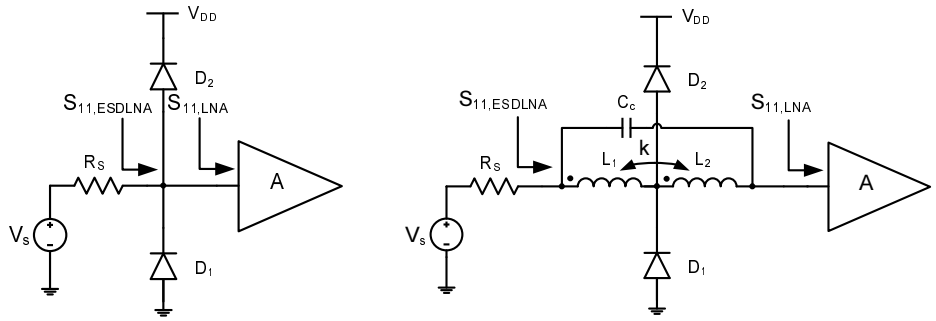

Figure 5.1: ESD protection for a wideband RF amplifier: classical dual-diode approach (left), and new plug-and-play transformer-diode approach or T-diodes (right).

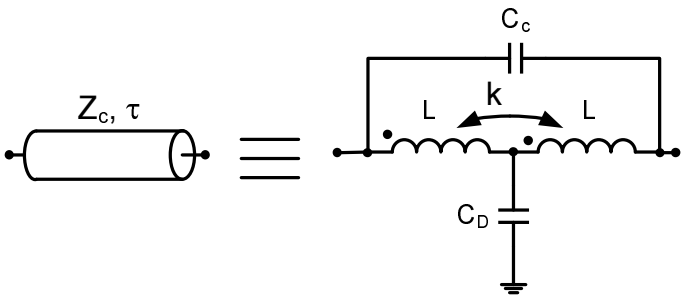

Figure 5.2: Equivalence of the T-circuit with a lossless transmission line. C_D represents the diode capacitance.

This T-diode concept is based on the T-coil-based ESD protection for high-speed digital I/O's as proposed by Galal [Galal 03]. The principal schematic is shown in Fig. 5.3, where the capacitance of the ESD protection (C_D) at the digital I/O is tuned out using the T-coil composed of L_1, L_2 and C_B. Wideband input matching is obtained using the 50 Ω on-chip termination resistor R_T. Obviously, such solution cannot be used for RF applications due to the added noise of R_T. However, by replacing R_T with the matched input of the RF circuit, we get the same cancellation of C_D, resulting in the T-diode solution as shown in Fig. 5.1 (right).

The equivalent transmission line has a characteristic impedance Z_c and an electrical delay of τ. By comparing the Y and Z parameters of Fig. 5.2, the following design equations are derived [Horng 03]:

$$C_D = \frac{\tau}{Z_C} \tag{5.1}$$

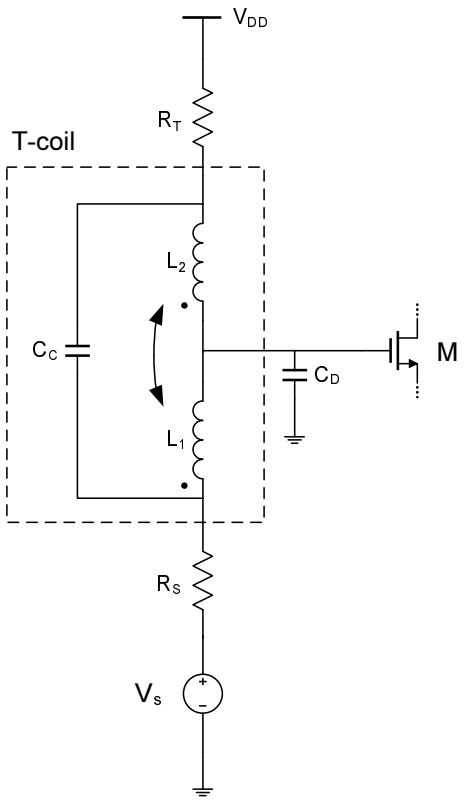

Figure 5.3: T-coil solution as proposed by Galal for high-speed digital IO's [Galal 03].

$$L = L_1 = L_2 = Z_C \tau \left(\frac{1}{4} + \frac{1}{\pi^2} \right) \tag{5.2}$$

$$M = Z_C \tau \left(\frac{1}{4} - \frac{1}{\pi^2} \right) \tag{5.3}$$

$$C_C = \frac{\tau}{Z_C \pi^2} \tag{5.4}$$

$$k = \frac{M}{L} \tag{5.5}$$

In this way, an equivalent transmission line is placed in front of the wideband RF LNA, as shown in Fig. 5.1 (right). The impact of the transmission line on

the input reflection coefficient of the unprotected LNA ($S_{11,LNA}$) is described by:

$$S_{11,ESDLNA} = S_{11,LNA} \cdot e^{-2j\omega\tau} \tag{5.6}$$

Therefore, the T-diodes have no impact on the magnitude of the input reflection coefficient:

$$|S_{11,ESDLNA}| = |S_{11,LNA}| \cdot \left|e^{-2j\omega\tau}\right| = |S_{11,LNA}| \tag{5.7}$$

As a consequence, T-diodes as ESD protection preserve the input matching bandwidth of the amplifier.

A simple design plan to realize T-diodes for a given wideband application is as follows. The minimum size of the ESD protection elements (in this case the diodes D_1 and D_2) is fixed based on the required diode ESD robustness (e.g., TLP It_2/Vt_2) and the target ESD robustness of the circuit terminal (e.g., 2 kV HBM). This determines the minimum value of the capacitance C_D. From (5.1), the electrical delay τ is defined, for a characteristic impedance Z_c (50 Ω). L is then calculated from (5.2), and k from (5.3) and (5.5). Finally C_c is determined by (5.4).

Since L_1=L_2, we propose to realize the transformer as a centre tapped symmetrical inductor, shown in Fig. 5.4. The coils are routed in the top metal for best ESD and RF performance. The ESD protection diodes between V_{DD} and V_{SS} (Fig. 5.1 (right)) are connected at the centre tap node X in Fig. 5.4. Metal routing to the V_{DD} and V_{SS} connection of the diodes is placed along the symmetry axis of the transformer to minimize any impact on the transformer RF performance. Alternatively, the routing could be elegantly integrated in the ground shield of the transformer.

ASITIC [ASITIC] is extensively used to design and optimize the on-chip transformer mentioned above. The length of the spiral determines the inductance values, while the spacing between the different windings determines the coupling factor k. Using ASITIC, C_c can be realized by the parasitic capacitance between L_1 and L_2 benefiting a low area consumption. If needed, additionally a separate capacitance can be added. In case C_C is smaller than the parasitic capacitance already present between L_1 and L_2, and additional re-optimization step in ASITIC is required. τ needs to be made larger and as a consequence C_D needs to be increased as well.

A lumped wideband RF model is extracted from ASITIC simulations, as shown in Fig. 5.5. L_{1i} and L_{2i} together with R_{1i} and R_{2i} model the skin effect in the

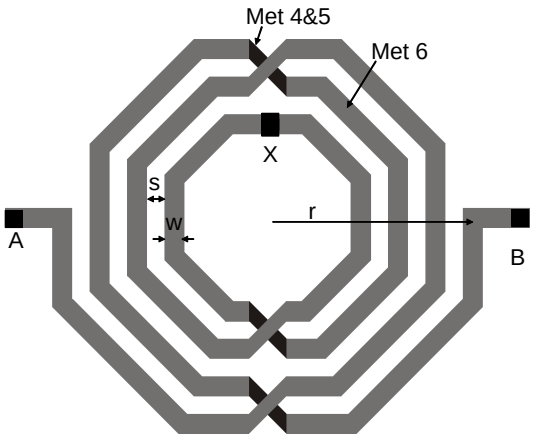

Figure 5.4: Layout of the on-chip transformer (r=75 μm, w=7 μm, s=6 μm, 4 turns).

electrical windings of the transformer and C_p the parasitic capacitive coupling between the windings (in parallel with C_c). C_{ox}, C_{sub} and R_{sub} model the coupling to the substrate with its associated losses.

5.2.2 Symmetric T-diode

To demonstrate the new T-diode solution, a wideband RF LNA, designed in SilTerra 0.18 μm CMOS technology was protected against ESD with symmetric T-diodes (Fig. 5.6) as described in the previous section. The cascode amplifying stage has a wideband resistive load R_{load} while shunt-shunt feedback by transistor M_3 provides 50 Ω input matching. Two parallel 65 μm wide ESD diodes are used, with a total capacitive load of 460 fF. These diodes are sized very large in order to demonstrate the capability of the T-diodes approach. A Diode-Triggered SCR is used as a power clamp [Merg 03]. Four trigger diodes are used, to ensure low leakage during normal operation bias conditions of 1.8 V. The number of diodes also defines the trigger voltage of the protection device. The transformer is realized in the top thick metal layer 6 to minimize the resistive, capacitive, and substrate losses. The parameters of the T-diode according to equations (5.1)-(5.5) for 460 fF C_D are shown in Table 5.1. The micrograph of the processed LNA with the T-diodes is shown in Fig. 5.7.

Both RF and ESD measurement results, together with implemented improvements, are discussed next.

RF measurements

The LNA consumes 2.7 mA from a 1.8 V supply. The buffer together with an off-chip bias-T drives the off-chip load of the measurement setup, and consumes

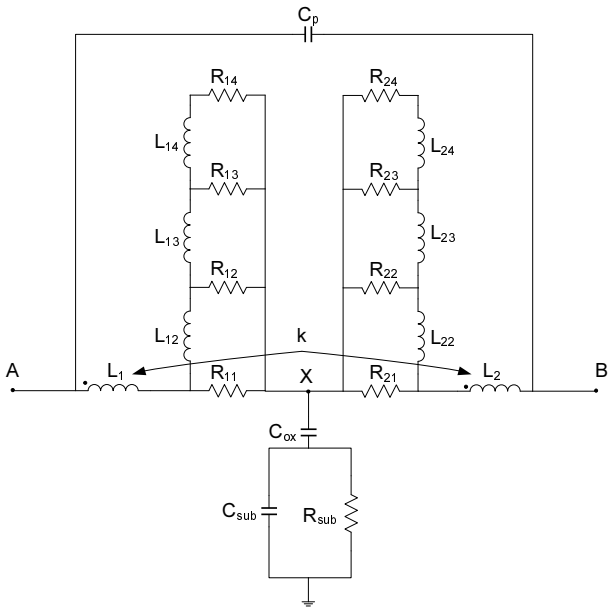

Figure 5.5: Schematic wideband model of T-diode. (Standard RF diode model connected to node X not shown.)

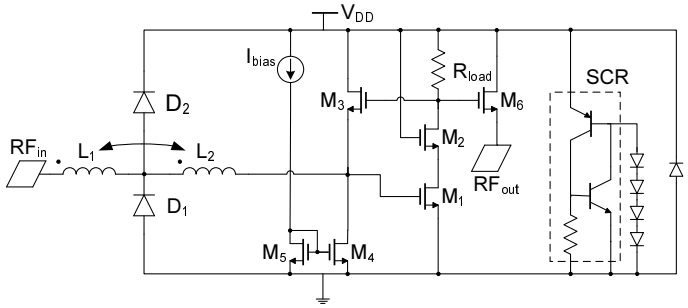

Figure 5.6: Schematic of T-diode ESD protected wideband LNA.

38 mA with a 1.8 V supply. Measured S-parameter and noise figure of the wideband amplifier with and without the T-diodes are shown in Fig. 5.8 and Fig. 5.9, respectively. By adding the T-diode, the input matching bandwidth up to 2 GHz of the core ciruit is maintained. Only a slight degradation in gain and noise figure is measured. In section 5.2.3, the T-diode methodology is demonstrated on an LNA with 16 GHz bandwidth.

ESD measurements

On-wafer HBM and TLP measurements have been performed. TLP measurements on the stand-alone diode, on-chip transformer and T-diodes are shown in Fig. 5.10. Measured It_2 values are 5, 3.5, and 3.5 A, with an on-resistance of

Table 5.1: T-diode design values for a diode capacitance C_D of 460 fF.

Parameter	Value
C_D	460 fF
Z_C	50 Ω
τ	23 ps
L	0.4 nH
M	0.17 nH
C_C	46 fF
k	0.425

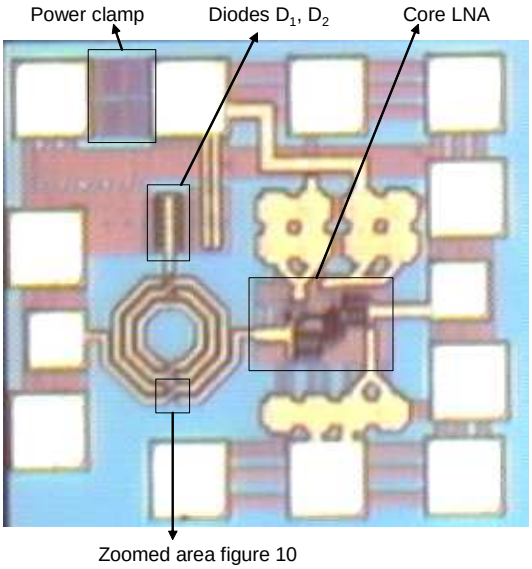

Figure 5.7: Micrograph of T-diode ESD protected wideband LNA circuit. The total chip area, including the bond pads, is 545x500 μm^2.

0.25, 4.2 and 4.45 Ω respectively. The diode passes a 7 kV HBM stress, while the transformer and the T-diodes fail at 5.5 kV HBM stress. This, together with the failure micrograph in Fig. 5.11, proves that the failure of the T-diodes is due to the thermal failure of the underpass in the transformer.

HBM measurements on the ESD protected circuit are summarized in Table 5.2. The circuit fails with V_{DD} to RF_{IN} stress at 2 kV (passes 1.5 kV), for RF_{IN} to V_{SS} stress it survives a 2 kV HBM stress. When stressed V_{SS} to RF_{IN} and RF_{IN} to V_{DD}, it passes 5 kV HBM and fails at 5.5 kV HBM. This corresponds to the HBM failure level of the stand-alone transformer.

From this table, it can be observed that any ESD path that runs through the

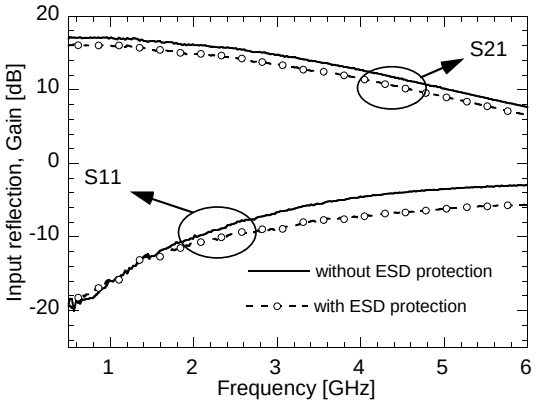

Figure 5.8: Measured S-parameters (S_{11} and S_{21}) of the wideband LNA, with and without T-diode ESD protection.

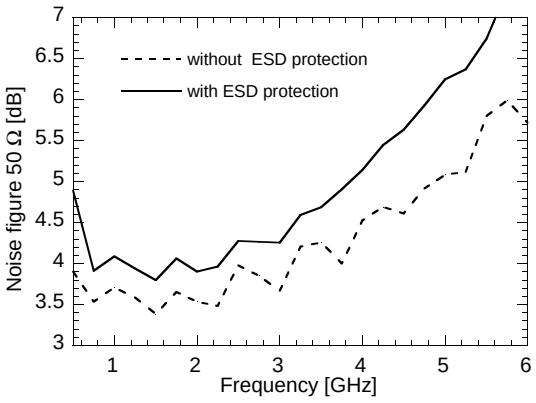

Figure 5.9: Measured 50 Ω noise figure of the wideband LNA, with and without T-diode ESD protection.

power clamp results in a lower ESD robustness. The stand-alone power clamp has an It_2 of 4.2 A TLP, which corresponds to a robustness of more than 5 kV HBM. The TLP-IV of the power clamp is shown in Fig. 5.12. This ESD level of 5 kV HBM is not achieved on circuit level, indicating the presence of a parasitic path through the core during ESD stress.

During ESD stress from V_{DD} to V_{SS}, the lower ESD failure level is attributed to a drain-source filament of the amplifying transistor M_1. This is confirmed by leakage measurements between different pin combinations. A possible improvement is to replace the power clamp with a faster clamp (according to section 2.5.3.1) as will be demonstrated further on.

Similarly, RF_{IN} to V_{SS} TLP measurements on the unprotected LNA reveal that M_4 is going into snapback around 4.5 V. As M_4 is a small fully-silicided

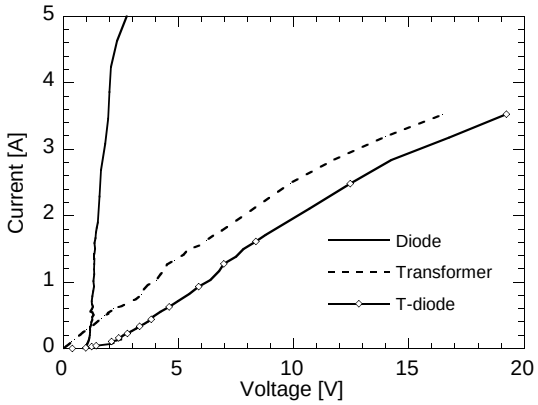

Figure 5.10: TLP-IV curves of diode, on-chip transformer and T-diode.

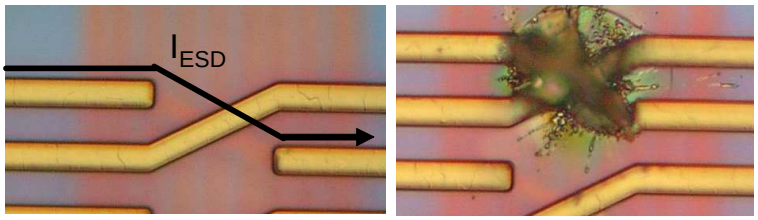

Figure 5.11: Optical micrograph of T-diodes: left - ESD current path through the under pass; right - the ESD induced failure.

Table 5.2: HBM measurements [kV] on the ESD protected LNA.

+/-	RF_{IN}	V_{SS}	V_{DD}
RF_{IN}		2	5
V_{SS}	5		5
V_{DD}	1.5	3	

transistor, it fails as soon as its snapback is reached, explaining the reduced HBM performance in Table 5.2. Fig. 5.13 shows that in the case of the ESD protected LNA with the T-diodes, this failure of M_4 is reached at 0.7 A TLP stress from RF_{IN} to V_{SS}. However, in the ESD protected LNA with standard dual-diodes (same diodes as in the T-diode), this failure is already reached around 0.6 A TLP. It is clear that the parasitic series resistance of L_2 in the T-coil acts as a ballast resistance for M_4 and increases the triggering point of the parasitic bipolar in M_4. Similar reasoning explains the early failure when stress is applied between V_{DD} and RF_{IN} (M_3 goes in early snapback and fails).

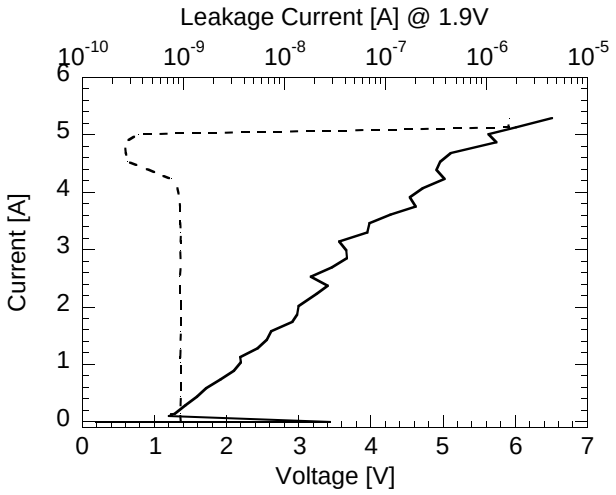

Figure 5.12: TLP-IV curve of the power clamp. The power clamp is a Diode-Triggered SCR with four trigger diodes.

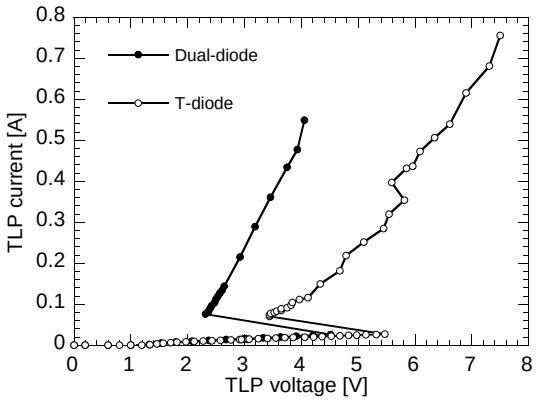

Figure 5.13: TLP-IV curve during stress from RF_{IN} to V_{SS}. The power clamp is a Diode-Triggered SCR with four trigger diodes.

Improved architecture

The ESD robustness of the circuit shown in Fig. 5.6 can be further improved for V_{DD}-RF_{IN} and RF_{IN}-V_{SS} ESD stress. In the previous section, it was indicated that the snapback of M_4 is delayed in the RF_{IN} to V_{SS} stress by the parasitic resistance of L_2 in the T-diode. This effect can be extended by adding an integrated resistance R_2 in series with the drain of M_4, without interfering with the RF circuit operation, as shown in Fig. 5.14. This is possible since M_4 is a bias transistor with a high impedance at the drain side (g_{ds} of M_4). The (rather small) resistor is thus in series with a current source, therefore not influencing the noise performance.

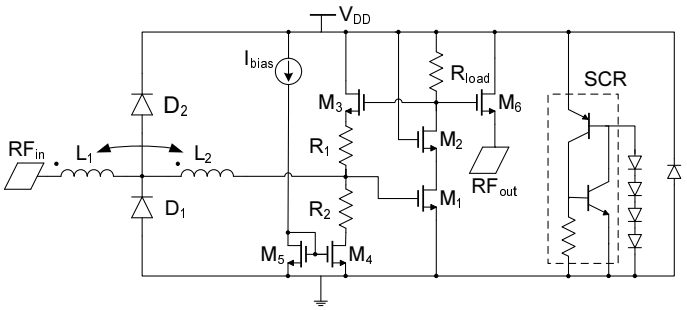

Figure 5.14: Schematic of ESD-protected LNA where R_1 and R_2 increase the ESD robustness for stress between V_{DD}-RF_{IN} and RF_{IN}-V_{SS}.

Similarly, for V_{DD} to RF_{IN} robustness improvement, an integrated resistance R_1 can be placed in series with the source of the feedback transistor M_3, see Fig. 5.14. This again prevents M_3 to go early in snapback. Unlike R_2, resistor R_1 cannot be added without slightly altering the core of the LNA. In order to still provide a 50 Ω input impedance, the g_m of M_3 must be resized according to:

$$\frac{1}{g_{m,M3}} = R_s \cdot (1 + g_{m,M1} R_{load}) - R_1 \tag{5.8}$$

R_1 will increase the linearity of the amplifier, which is desired for the RF design. In our implementation, R_1 and R_2 both were chosen to be 100 Ω. The measured S-parameters of the wideband LNA with and without the additional resistances R_1 and R_2 are shown in Fig. 5.15, showing no influence of the added resistances on S_{11} and S_{21}.

These techniques are no longer a "plug-and-play"-compatible strategy. However, the problems tackled by the previous suggestions are specific to the very nature of the feedback-type LNA. They can be considered as good practice designing such types of LNA for ESD compatibility, since these resistors have no significant impact on the RF performance.

For V_{DD} to V_{SS} stress, it was already argued that a faster power clamp would be needed to avoid core damage. As such, the original power clamp (based on STI isolation) was replaced by a faster design (based on poly isolation) as proven in [Scho 07b]. The transformer in the T-diodes was re-optimized in order to consume less area. As a result the width of the turns increased, leading to improved ESD performance.

The ESD results are shown in Table 5.3 and Table 5.4, where the first table shows the improvements due to the improved transformer and faster power clamp. The latter table shows the improvements when additionally resistances

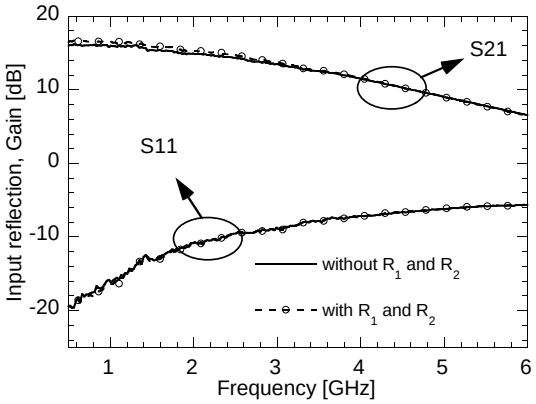

Figure 5.15: Measured S-parameters (S_{11} and S_{21}) of the wideband LNA, with and without additional resistors R_1 and R_2.

Table 5.3: The improved transformer and faster power clamp show an increased HBM robustness [kV].

+/-	$\boldsymbol{RF_{IN}}$	$\boldsymbol{V_{SS}}$	$\boldsymbol{V_{DD}}$
$\boldsymbol{RF_{IN}}$		3	3.2
$\boldsymbol{V_{SS}}$	6		>8
$\boldsymbol{V_{DD}}$	6	>8	

Table 5.4: The additional resistances R_1 and R_2 further improve the HBM robustness [kV] of the circuit.

+/-	$\boldsymbol{RF_{IN}}$	$\boldsymbol{V_{SS}}$	$\boldsymbol{V_{DD}}$
$\boldsymbol{RF_{IN}}$		4.6	6
$\boldsymbol{V_{SS}}$	6		>8
$\boldsymbol{V_{DD}}$	5.6	>8	

R_1 and R_2 are placed. The weakest pin to pin combination (RF_{IN}-V_{SS}) shows now even a robustness of 4.6 kV HBM.

The use of T-diodes themselves can be further optimized. For example, the occupied area can be minimized by using a more compact multi-layer transformer. This will be demonstrated in section 5.2.3. On the other hand, the size of the diodes can be reduced so that their It_2 matches the It_2 of the transformer (3.5 A TLP). This results in smaller C_D, and therefore a lower required inductance value, (5.1)-(5.2). This leads to smaller inductor footprint, lower series resistance, and a higher bandwidth.

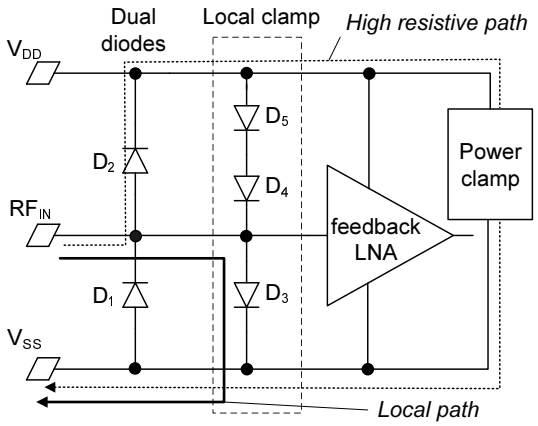

Figure 5.16: Concept of dual-diode ESD protection solution with additional local clamp.

During a CDM event, voltage overshoot can occur inside the core circuit, which can lead to failure. A special local clamping technique is implemented in section 5.2.3 and its benefit is demonstrated using VFTLP measurements.

5.2.3 Asymmetric T-diode with built-in local ESD protection

In this subsection, a DC-to-16.1 GHz wideband LNA in 90 nm digital CMOS is ESD protected by adding a new compact wideband RF ESD protection component on its RF input: an area-efficient multi-metal layer asymmetric T-diode with built-in local ESD protection, which does not degrade the RF bandwidth of the LNA. This solution occupies less silicon real-estate than the symmetric T-diodes from the previous subsection.

A classical dual-diode ESD protection (Fig. 5.16) with a power clamp between V_{DD} and V_{SS}, is commonly used as low-capacitance RF-ESD protection solution. A feedback LNA is selected (Fig. 5.16), similar as in the previous section, to obtain a wide bandwidth. For this LNA topology, two worst case ESD stress conditions exist: RF_{IN}+ to V_{SS}- stress, and V_{DD}+ to RF_{IN}-. For the first condition, the ESD current path is indicated by the dotted line in Fig. 5.16. An early LNA failure will occur due to the low oxide breakdown voltage of the input transistor of the feedback LNA (4.5 V using TLP), before the thermal failure of diode D_2 is reached. This is caused by the relative high resistive path of the ESD current which results in a high voltage build up at the input of the LNA. For the second condition, a parasitic ESD current path through the feedback transistor will be triggered (see previous section), and will result in thermal failure of that feedback transistor. This burn-out can be prevented with the correct sizing of R_{bal} as indicated in section 5.2.2.

Local ESD clamp

To increase the ESD robustness, a local ESD clamp suitable for this LNA topology is added, see the dotted box in Fig. 5.16: one forward diode D_3 between RF_{IN} and V_{SS} and two series forward diodes D_4-D_5 between V_{DD} and RF_{IN}. These diodes remain off during normal operation as the nominal bias voltage of RF_{IN} is 0.4 V. Of course, the number of required series diodes depends on the RF specifications, such as leakage current at high temperature. The ESD current can now flow locally from RF_{IN} to V_{SS} via D_3 (solid line in Fig. 5.16), without passing the power rails and the power clamp. Hence, during an ESD event, a lower voltage is build up at the input of the LNA, and thus early failure due to oxide breakdown is prevented. Similarly in case of V_{DD} to RF_{IN} stress, the ESD current flows locally to RF_{IN} through diodes D_4-D_5, preventing burn-out of parasitic current paths in the core feedback LNA. An alternative solution, which turns off this parasitic path during the ESD event, is proposed in section 5.2.4.

Compact multi-metal level asymmetric T-diode

Adding the local clamp roughly doubles the total parasitic ESD capacitance from 100 fF to 200 fF (when including interconnect and nwell-pwell parasitic capacitances), which will have a direct negative impact on the RF performance. However, the T-diode concept can be used to compensate for such high capacitive loading. Therefore in this subsection, the impact of the dual diode ESD protection including local clamping with and without T-diode is compared to the reference design.

The demonstrator LNA (Fig. 5.17) is an active feedback, common source amplifier [Borremans 07b]. It operates from DC-to-16.1 GHz and is implemented in a 90 nm digital CMOS technology. A cascode stage M_{n1}-M_{ncas} offers gain, while the feedback via the source- follower M_{n2} and R_{bal} ensures input matching. A 30x30 μm^2 multilayer 0.9 nH shunt peaking inductor L_{load} is added in series with the load resistor R_{load} to boost the bandwidth. The second stage M_{nbuf} works as a buffer to drive the measurement setup. The LNA consumes 12.36 mW power with a 1.2 V supply. The measured gain, input matching and noise figure of the unprotected LNA are shown in Fig. 5.18 and Fig. 5.19, respectively.

All diodes in Fig. 5.17 consist of 40 μm width with 50 fF parasitic capacitance and with 3.2 kV HBM robustness. An RC-triggered NMOS or Diode Triggered SCR is selected as a power clamp.

The addition of the dual diode with local clamping degrades the input matching bandwidth by 3 GHz with respect to the unprotected LNA, see Fig. 5.18 (right). To compensate for this loss in bandwidth, a compact asymmetric T-diode is introduced, Fig. 5.17 and Fig. 5.20, which consists of an on-chip transformer and the ESD diodes D_1-D_5 as discussed above. The T-diode acts as an

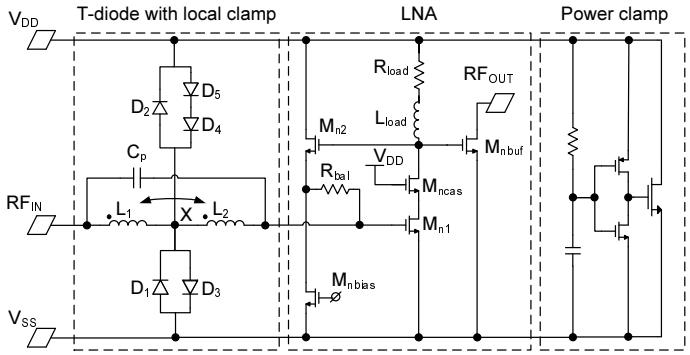

Figure 5.17: Schematic of ESD protected wideband RF LNA.

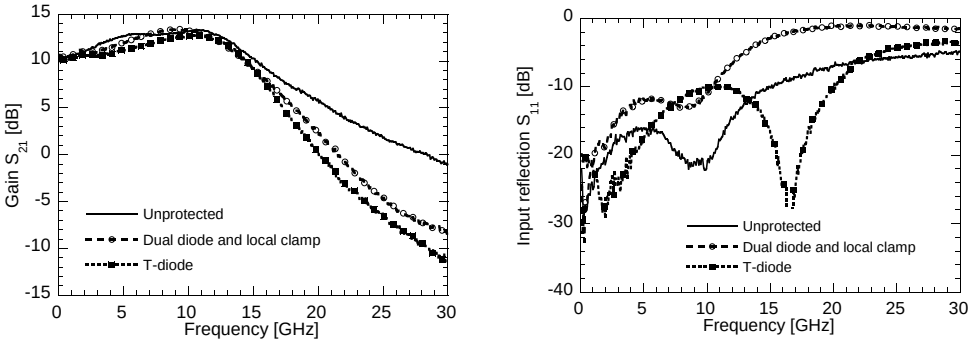

Figure 5.18: Measured gain S_{21} (left) and input matching S_{11} (right) of: the unprotected LNA, LNA with dual-diode and local clamp ESD protection, and T-diode ESD protection with local clamp.

equivalent transmission line placed in front of the RF circuit that needs to be protected. This new improved T-diode uses an asymmetric transformer (L_1>L_2) which compensates, besides for the diode capacitance, also for the parasitic resistor losses (R_{esd}=3 Ω) of the ESD diodes at high frequencies. This makes this T-diode a suitable extreme wideband RF plug-and play ESD protection element. Its size is based on the design equations of a T-coil in Fig. 5.20 [Feuc 90]. In these equations the input impedance (R_t) of the LNA is assumed to be 50 Ω over the whole bandwidth. The transformer is realized as a compact multilayer transformer (50x50 μm^2) with a patterned ground shield, and optimized with HFSS [HFSS]. C_p is realized by the inter-winding capacitance of the transformer.

Using the T-diode as ESD protection for the wideband RF LNA, Fig. 5.17, the input matching is significantly improved from 14.5 GHz for the unprotected LNA to 20.1 GHz, Fig. 5.18 (right). By using this solution, the bandwidth of the LNA is not limited anymore by the capacitance of the ESD diodes (dual-diode and local clamp), and can even further improve the RF input matching by

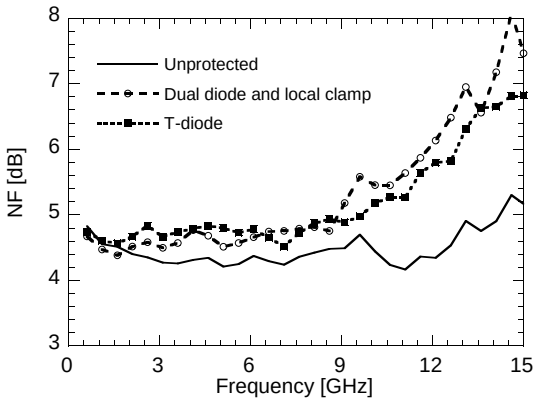

Figure 5.19: Measured noise figure of: the unprotected LNA, LNA with dual-diode and local clamp ESD protection, and T-diode ESD protection with local clamp.

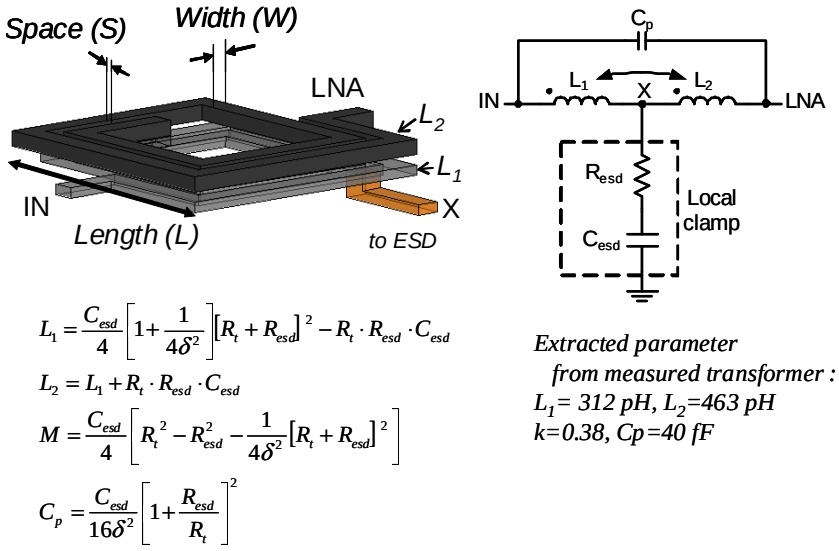

Figure 5.20: Asymmetric (L_2>L_1) T-diode layout design (L=55 μm, W=4.6 μm and S=0.57 μm) and equivalent schematic.

tuning out the parasitic input capacitance of the LNA. This enables the T-diode to be used in RF-ESD co-design approaches. The minimum NF is increased by only 0.3 dB compared to the unprotected LNA (Fig. 5.19), resulting from the contribution of the ESD diode noise levels and the transformer interconnect resistances. The ESD protection solution does not have a significant impact on IIP3 (2-3 dB reduction of the -9 dBm IIP3 at 5 GHz). The micrograph of the LNA is shown in Fig. 5.21.

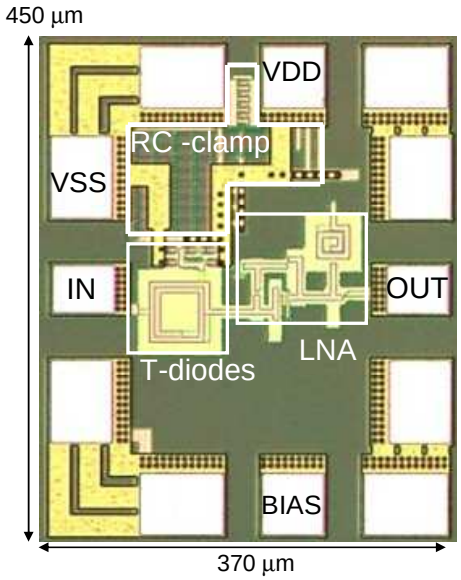

Figure 5.21: Micrograph of ESD protected LNA. Total active area of the design is 200x215 μm^2.

Table 5.5: On-wafer HBM measurement [kV] summary.

+/-	$\boldsymbol{RF_{IN}}$	$\boldsymbol{V_{SS}}$	$\boldsymbol{V_{DD}}$
$\boldsymbol{RF_{IN}}$		4.5	4.6
$\boldsymbol{V_{SS}}$	4.8		>6
$\boldsymbol{V_{DD}}$	2.4	2.4	

ESD measurement summary

A performance summary of the on-wafer Human Body Model (HBM) ESD measurements on the T-diode LNA using the RC-triggered NMOS as power clamp, is shown in Table 5.5. A 4.5 kV HBM robustness for RF_{IN} to V_{SS} stress is achieved. Since the diode can sustain only 3.2 kV, it is clear that the ESD current path through the power clamp (dashed line in Fig. 5.16) contributes as well. In case 3.2 kV is sufficient, the power clamp can be removed because the diodes D_3, D_4 and D_5 work as a local power clamp. This will reduce the chip area needed for ESD protection.

A 2.4 kV HBM robustness is reached for the worst pin to pin combination, V_{DD} to RF_{IN} stress, which is caused by degradation of the resistor R_{bal} at high current density. This is confirmed by HBM measurements on the same LNA implemented without R_{bal}, which survives 4 kV HBM. In [Lee 01], non-silicided poly resistors were shown to change their resistance value under high current

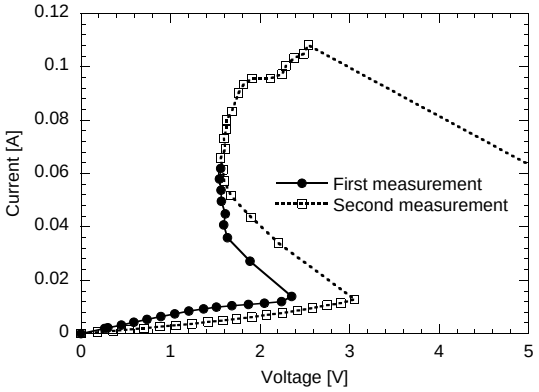

Figure 5.22: TLP-IV of non-silicided polysilicon resistor with 1 μm width and length.

conditions, which occurs after their breakdown voltage has been reached. This is attributed to a change in the number of activated impurities in the polysilicon under high-current stress. TLP measurements have been performed on R_{bal} in Fig. 5.22. R_{bal} is a non-silicided resistor with both width and length 1 μm. The first measurement has been stopped after snapback, before thermal failure. When restarting the measurement on the same device, a change in initial resistance is observed from 140 to 315 Ω. The distortion of this resistance characteristics causes severe impedance mismatch and should be considered as failure.

However, in the previous section, the addition of such resistor was shown to improve the ESD robustness and not degrade it. For that design, the resistor was implemented with 4 μm width and 6 μm length. The higher operating frequencies of the new LNA impose a limit on the parasitic capacitance of R_{bal}, reducing the allowed size of the resistor to 1 μm square for the present LNA design. In [Lee 01], the breakdown voltage of the polyresistor was shown to be independent of width, but proportional to length. Our measurements on resistors with length 1 μm and 3 μm yield a breakdown voltage of 2.35 V and 5.9 V respectively, confirming this trend. Therefore, the previous resistor with 6 μm length was not degraded due to its higher breakdown voltage of around 12 V. The smaller resistor dimensions make it very vulnerable to ESD stress. However, as the addition of such resistance was shown to improve the linearity of the LNA, it became an inherent part of the RF design and hence cannot be removed. Local clamping was only protecting the resistor up to 2.4 kV, so other protection techniques are needed, as will be discussed in section 5.2.4.

VFTLP measurements have been performed as a measure to assess the CDM robustness of the LNA using the DTSCR as power clamp instead of the RC-triggered NMOS. The speed improved poly-isolated DTSCR power clamp

(section 2.5.3.1) was not allowed because of Design Rule Check (DRC) violations. Therefore, the slower STI-based version was used as power clamp. When stressing the worst case combination RF_{IN}+ to V_{SS}-, failure occurs already at 0.25 A VFTLP. Addition of the local clamp as in Fig. 5.16 results in survival of 3.8 A VFTLP on all pin-to-pin combinations. This roughly corresponds to a CDM value of 300 V [CDM 08]. This high robustness against CDM-like events is achieved as the local ESD diodes in the T-diode suppress voltage overshoots, by the availability of a local low resistive current path.

5.2.4 ESD turn-off circuit

In the previous subsection, the core LNA fails early in the V_{DD}+ V_{SS}- and V_{DD}+RF_{IN} stress combination as a result from triggering of parasitic ESD current paths in the core of the LNA. An alternative methodology to boost the ESD robustness is to keep these parasitic paths off during an ESD event, by means of an ESD turn-off circuit.

The addition of such turn-off circuits is a general strategy to keep any parasitic current path off during ESD stress. Possible triggering of parasitic current paths during ESD events is easily overlooked. In fact, failure due to such effects can occur well before gate oxide breakdown as demonstrated in the previous subsection.

When ESD stress occurs between V_{DD}+ and V_{SS}-, the cascode transistor M_{ncasc} is pulled fully open, leading to failure of transistor M_{n1}. This parasitic current path through the core can be kept off during ESD by turning off the gate of M_{ncasc}. As the gate of M_{ncasc} normally is hard wired to V_{DD}, a simple transient RC-timer can be used. This RC-timer can be implemented using R_{TO} and C_{TO} as shown in Fig. 5.23. During normal operation, C_{TO} is charged to V_{DD}, providing a stable DC bias to the gate of M_{ncasc}. However, during ESD stress, C_{TO} needs some time to charge depending on $C_{TO} * R_{TO}$. This keeps the gate of M_{ncasc} low, thereby switching off the parasitic current path.

When stressing V_{DD}+ to RF_{IN}-, feedback transistor M_{n2} is conducting and R_{bal} will fail as shown in the previous subsection. The gate of M_{n2} cannot be controlled with a RC turn-off circuit similar to M_{ncasc}, since now the gate is connected to an RF node, instead of a DC node. Therefore, an additional transistor M_{nTO} (TO=Turn Off) is added at the drain of M_{n2}, Fig. 5.23. The gate of M_{nTO} can now be connected to the RC turn-off timer. During normal operation conditions, the gate of M_{nTO} is pulled to V_{DD} turning it fully open, and therefore the addition of this transistor does not impact normal RF circuit operation. During an ESD event between V_{DD}+ and RF_{IN}-, M_{nTO} is kept off for the initial first ns, forcing the ESD current to flow through the power clamp, instead of through the parasitic ESD path.

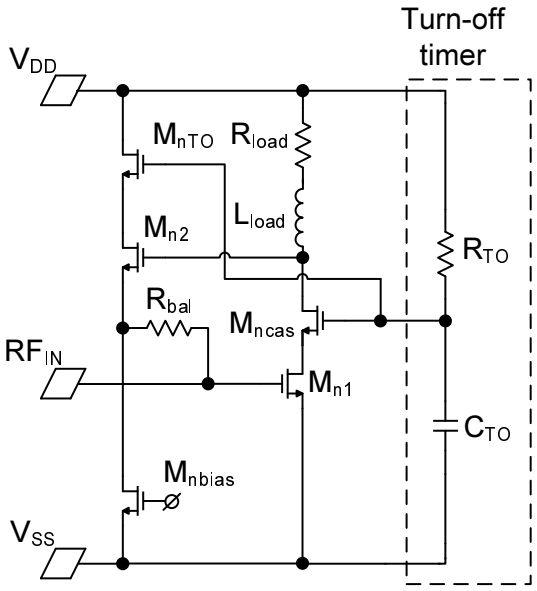

Figure 5.23: LNA topology with ESD turn-off circuit.

The RC of the turn-off circuits can be shared to turn off several possible parasitic ESD paths as shown in Fig. 5.23. Further, in case when an RC-triggered power clamp is used, its RC can also be used to control the different turn-off circuits. In that case, no additional RC turn-off timer is needed for the turn-off circuits.

ESD simulations

Fig. 5.23 replaces the LNA block in Fig. 5.17 for the full circuit including ESD protection elements. A DTSCR power clamp is used instead of the RC-triggered power clamp. Fig. 5.24 shows the simulated voltage and current waveforms during a 1 kV HBM V_{DD}+ to RF_{IN}- stress, without (left) and with (right) turn-off circuit. Without turn-off, a hazardeous current of 250 mA peak flows through the core circuit, before the power clamp has turned on. By adding the turn-off circuit, the parasitic current path through the core LNA is switched off, reducing the peak current to 20 mA. This will significantly improve the overall ESD robustness.

ESD measurements

HBM measurements with 250 V voltage steps, have been performed on the LNA with local clamping (Fig. 5.17) where the DTSCR was used as power clamp, and with the shared turn-off circuit as shown in Fig. 5.23. The turn-off timer was constructed with a 20 kΩ resistor and a 25 pF capacitor, yielding an RC time constant of 500 ns. Due to addition of the turn-off circuit, the HBM level is increased from 2.25 kV to 4 kV. The normalized leakage evolution after

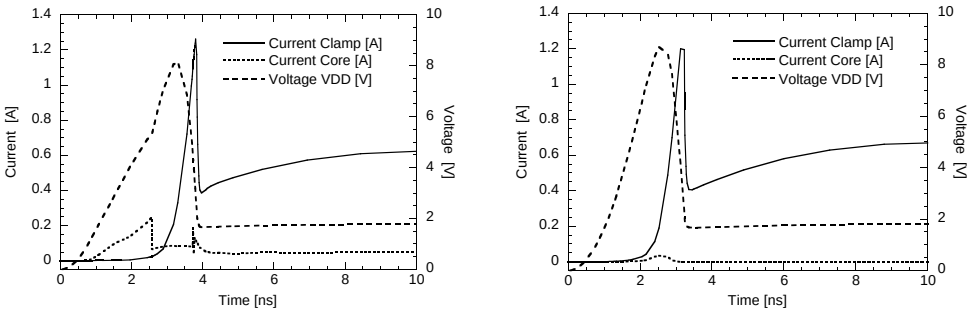

Figure 5.24: Simulated V_{DD}+ to RF_{IN}- 1 kV HBM stress, without (left) and with (right) ESD turn-off circuit.

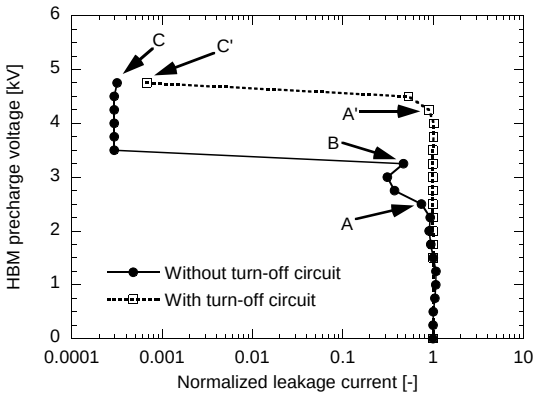

Figure 5.25: Normalized leakage current after different HBM stress levels for the LNAs without and with turn-off circuitry.

each HBM level is compared in Fig. 5.25 without and with turn-off. Markers are included to indicate the different failure points. Without turn-off, a leakage decrease in seen at 2.5 kV (point A), caused by the resistance increase of R_{bal}. This effect happens at 4 kV when the turn-off is used (point A'). When increasing the HBM level on the circuit without turn-off, R_{bal} fuses to an open at 3.25 kV (point B) resulting in another leakage decrease. Finally, at a HBM level of 4.75 kV, the Tcoil inductor fuses in both cases (points C and C'), which was observed by visual inspection.

When using only turn-off circuitry without local clamping in absence of R_{bal}, an HBM robustness of 3.5 kV was measured, limited by failure of the feedback transitor M_{n2} in Fig. 5.23. In case this protection level is sufficient, it is better to use the turn-off solution instead of local clamping. Local clamping puts an extra capacitive loading on the RF input (which needs to be compensated by the Tcoil), while the turn-off solution comes for free. It even does not require any additional area, as generally in an RF circuit a lot of decoupling

Table 5.6: On-wafer HBM measurement [kV] summary.

R_{bal}	Local clamping	Turn-off 500 ns	Turn-off 200 ns	Turn-off 20 ns	HBM [kV] V_{DD}+RF_{IN}-	HBM [kV] V_{DD}+V_{SS}-
-	-	-	-	-	1.5	3
-	X	-	-	-	4	-
X	X	-	-	-	2.25/2.4	4.75
X	X	X	-	-	4	7
-	-	X	-	-	3.75	6.5
-	-	-	X	-	3.75	-
-	-	-	-	X	3.75	-

capacitances are present to stabilize the power lines. A few of these decoupling capacitances can easily be used for the turn-off circuit. The combination of both local clamping and turn-off yields the highest protection level, even when the fragile R_{bal} is present. When decreasing the RC-time constant of the turn-off timer from 500 ns to 200 ns and 20 ns respectively, no ESD performance degradation is noticed, indicating that the turn-off circuit is only needed during the first ns, defined by the turn-on time of the powerclamp. This is in correspondence with the simulations in Fig. 5.24.

In case of stress between V_{DD}+ and V_{SS}-, failure was observed in transistor M_{n1} due to a parasitic current path through the core LNA at 3 kV HBM stress. By addition of the local clamping, the robustness was increased to 4.75 kV. The turn-off circuit was also connected to the gate of cascode transistor M_{ncas}, see Fig. 5.23. This results in an increased performance between V_{DD}+ and V_{SS}- up to 7 kV.

An overview of the HBM measurements on the different circuit variations for the weakest pin combinations V_{DD}+ to RF_{IN}- and V_{DD}+ to V_{SS}- is shown in Table 5.6.

5.3 Center Balanced Distributed ESD Methodology

Distributed Amplifiers (DA) are widely used to achieve flat gain over very wide frequency bands [Pava 05] in applications such as instrumentation, electronic warfare and wireless communication systems. As the RF input is connected to the outside world via an antenna, adequate ESD protection is required.

Distributed ESD protection was first introduced by Kleveland as a possible solution for wideband RF circuits where the parasitic ESD capacitance is distributed in an artificial transmission line [Klev 00], such that matching

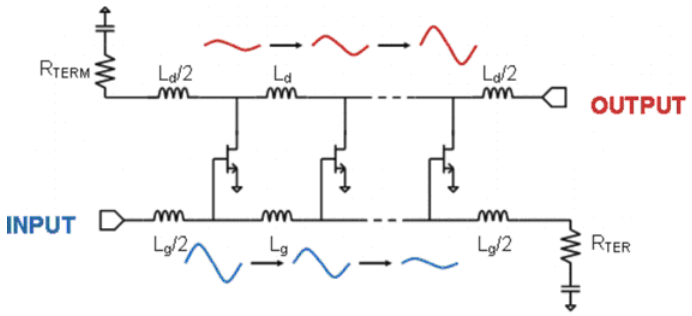

Figure 5.26: Circuit diagram of a distributed amplifier.

conditions can be maintained at 50 Ω over the full RF bandwidth.

In a DA, a set of artificial input and output transmission lines, which are coupled through the transconductance of gain cells, are connected in parallel. A principal schematic is shown in Fig. 5.26. ESD elements can be placed distributed at each gain stage. In such design, all ESD protection elements are equal in size, referred to as Equal-Sized Distributed ESD (ES-DESD). In [Ker 05], it was shown that such design fails prematurely since the efficiency of the ESD protection elements decreases with increasing number of stages and therefore, a Decreasing-Sized Distributed ESD (DS-DESD) co-design technique was proposed where the first ESD element is largest and then decreases over the next stages. However, a careful ESD-RF codesign of each gain stage should be done in order to achieve reasonable good RF performance.

Topology description

In this section, a Center Balanced Distributed ESD (CB-DESD) protection methodology is presented. A 1-110 GHz DA is used as demonstrator in a 45 nm CMOS technology using Above-IC technology [Carch 04]. In each stage, a cascode topology was chosen to reduce the Miller effect typically for nanometer-scale CMOS, which results in higher power gain, wider bandwidth and improved reverse isolation. In addition, a loss-compensation technique for the drain artificial transmission line was used. This technique is built on the properties of the common-gate FET of the cascode pair, which can present at its drain a broad-band (frequency-dependent) negative resistance [Deib 89]. The compensation is realized with two additional transmission lines, L_{cg} and L_{sd}. L_{cg} increases negative resistance and improves gain at high frequencies. L_{sd} changes the frequency dependence of the negative resistance term and its value is optimized in order to ensure end-of-band stability and to obtain a flat frequency response, Fig. 5.27 [Kimura 96].

The artificial transmission lines are composed of microstrip line sections implemented with Above-IC technology. The number of stages was fixed to 5.

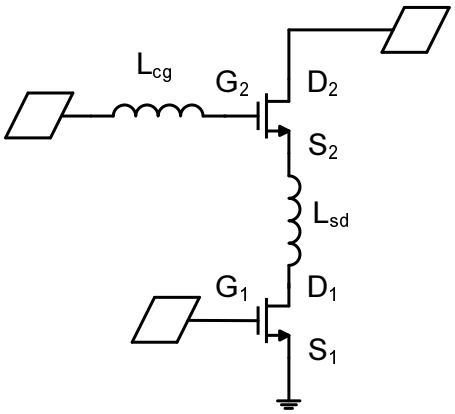

Figure 5.27: Cascode pair with two additional transmission lines L_{cg} and L_{sd} for drain line loss compensation.

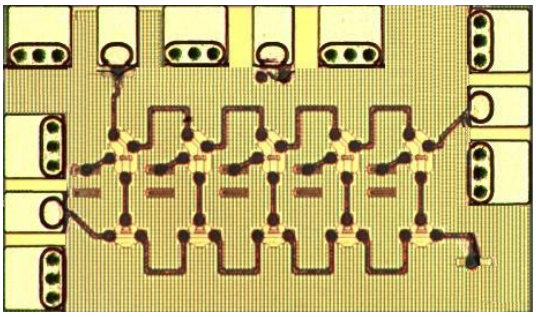

Figure 5.28: Chip micrograph (size: 675x395 μm^2).

Additional details concerning the design procedure can be found in [PhD-Pavageau]. A chip micrograph is shown in Fig. 5.28, where the different amplification stages are clearly visible.

In each stage, an ESD protection cell is placed as seen in Fig. 5.29. Only minor layout modifications are needed. Such ESD protection cell consists of dual diodes and a small local power clamp. By placing a local power clamp, any additional bus resistance is avoided. A schematic of an individual ESD cell is shown in Fig. 5.30.

The diodes are poly-defined because of speed reasons [Scho 07b]. As power clamp, a gated DTSCR with two gated trigger diodes is used [Scho 07b]. The leakage current of the PC can be neglected when compared to the circuit operating current. When used as local clamp, it is 8 μm wide, while a separate 60 μm version is used as big power clamp.

Three DA versions have been realized. A first version is implemented without any ESD protection (no-ESD). In a second version, the dual diodes have a

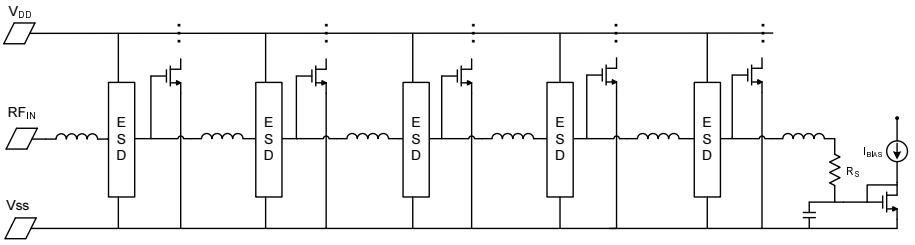

Figure 5.29: Schematic of the gate transmission line of the DA with distributed ESD protection.

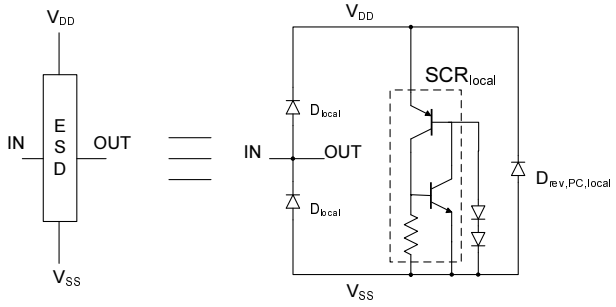

Figure 5.30: ESD protection elements that have been distributed along the transmission line.

width of 8 μm in each stage (ES-DESD). This roughly corresponds to 10 fF parasitic capacitance, which can be tolerated by the RF design (see subsection RF performance). Since the ESD performance of ES-DESD protection devices is not efficient [Ker 05], a novel methodology is developed without the need for going into complex ESD-RF co-design solutions. In this third version, diodes D_{local} in Fig. 5.30 of the first two stages are each replaced by two series diodes of double size, i.e. 16 μm as shown in Fig. 5.31. As such, the total parasitic capacitance contribution remains roughly the same, allowing each RF stage to remain unaltered. To be precise, the capacitance contribution from the nwell-pwell junction should be accounted for as well. In this ESD solution, the center stage will turn-on first (Center Balanced Distributed ESD CB-DESD), since the first two stages require two diodes to be forward biased instead of one before they start conducting. At higher current levels, the first two stages will kick in as well.

Spectre simulations are used to investigate the new proposed architecture. Fig. 5.32 compares the ES-DESD topology with the CB-DESD during a 1 and 2 kV HBM simulation. 2 kV HBM was the ESD target specification. The peak current through each stage is plotted. For 1 kV HBM, ES-DESD shows a maximum current of 220 mA in the first stage, which decreases in the next stages. CB-DESD shows similar maximum current, which is now reached in

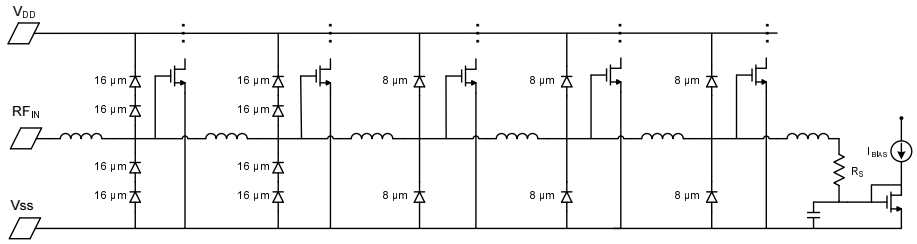

Figure 5.31: Schematic of the gate transmission line of the DA with CB-DESD protection.

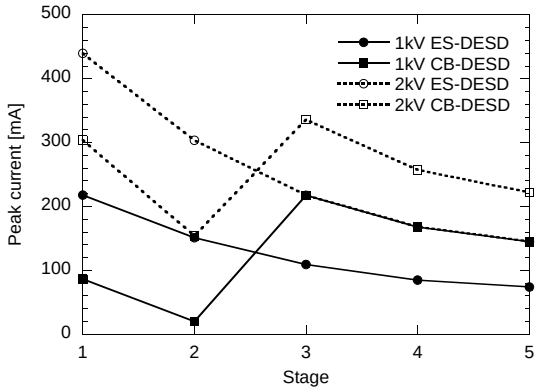

Figure 5.32: HBM spectre simulations of 1 and on a 5 stage distributed ESD protection according to ES-DESD and CB-DESD.

stage 3 rather than in stage 1. When comparing the distribution of current, ES-DESD is more evenly distributed than CB-DESD, because in the latter, stage 2 almost does not contribute to the current conduction. The voltage required to forward bias the two series diodes in stage 2 is barely reached. The benefit of the new Center Balanced Distributed architecture is only visible when increasing the ESD stress level. Fig. 5.32 also shows the peak current results in each stage during a 2 kV HBM simulation. Now the situation is altered as the maximum peak current in stage 1 for ES-DESD (440 mA) is much larger than the maximum peak current in stage 3 for CB-DESD (336 mA). During a 2 kV HBM pulse, CB-DESD distributes the current more evenly than ES-DESD as the first two stages start to turn on as well. When further increasing the ESD level, these first two stages will take more and more of the current until finally failure occurs. For a typical ESD robustness of 50 mA/μm per width for a symmetrical 2-sided diode in such CMOS technology, the 8 μm diode in the first stage of ES-DESD would fail during the 2 kV HBM stress, while all diodes would survive in CB-DESD.

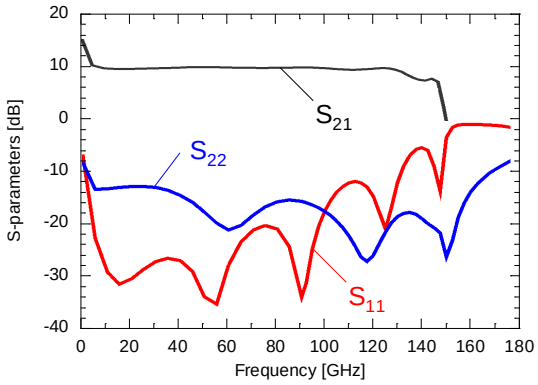

Figure 5.33: S-parameter simulation results for design no-ESD. (Power gain S_{21} and input and output matching S_{11} and S_{22}, respectively.)

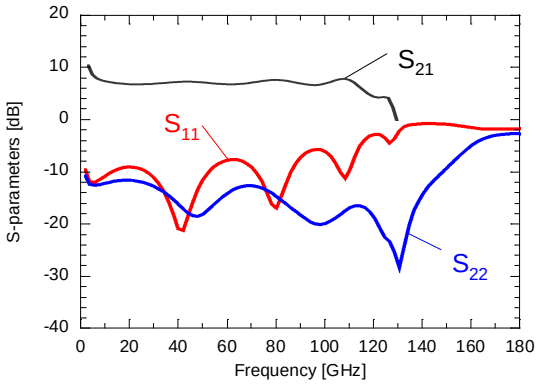

Figure 5.34: S-parameter simulation results for design ES-ESD and CB-DESD. (Power gain S_{21} and input and output matching S_{11} and S_{22}, respectively.)

RF performance

The impact on the RF performance of the distributed ESD protection is analyzed based on ADS simulation results as RF measurements are currently not yet available. Therefore, S-parameter simulation results are shown in Fig. 5.33. Biasing the unprotected design up to a power consumption of 38 mW, a power gain of 9.3 dB is simulated between 1 and 136 GHz with a 3 dB cut-off frequency of 148 GHz. A gain-bandwidth product of 426 GHz is achieved. Up to 130 GHz, input and output matching are better than -10 dB and -12.8 dB, respectively.

By adding the ESD protection diodes (ES-DESD and CB-DESD), a slight performance degradation is noticed. Fig. 5.34 shows the small signal S-parameters of design ES-DESD and CB-DESD. An RF performance summary is presented

Table 5.7: RF simulation performance summary.

	No-ESD	**ES-DESD & CB-DESD**
BW [GHz]	1-130	1-110
$\boldsymbol{S_{21}}$ **[dB]**	9.1 ± 0.4	8 ± 0.6
$\boldsymbol{S_{11}}$ **[dB]**	<-10	<-6.5
$\boldsymbol{S_{22}}$ **[dB]**	<-12.8	<-12
NF [dB]	<4.5	-
$\boldsymbol{f_{\text{-3dB}}}$ **[GHz]**	148	120
GBW [GHz]	426	305
FOM	30.9	22.2

in Table 5.7, where the FOM is defined as:

$$FOM = \frac{Gain}{P_{DC}} \cdot \frac{f_{-3dB}}{f_t^{NMOS}} \tag{5.9}$$

ESD performance

TLP measurements were performed to compare the ESD robustness of ES-DESD and CB-DESD. A short-calibration has been performed to yield accurate voltage measurement results. Fig. 5.35-Fig. 5.37 show the TLP-IV curves for different pin combinations. In all cases, an It_2 improvement of at least 50 % is measured for CB-DESD. For example, in Fig. 5.35, TLP pulses were applied between V_{SS}+ and RF_{IN}-. CB-DESD initially has higher on-resistance, because the third stage starts to conduct first, however it fails at 1.5 A TLP compared to 1 A for the reference ES-DESD. This corresponds to the targeted 2 kV HBM robustness for CB-DESD as predicted by the spectre simulations in Fig. 5.32.

Fig. 5.36 shows similar results for TLP stress between RF_{IN}+ and V_{DD}-. When stressing RF_{IN}+ to V_{SS}-, Fig. 5.37, the current will flow through the diode up and then through the local power clamp to ground. The increased failure level of 1.8 A for CB-DESD can be attributed to the additional current path to V_{SS}, formed by the parasitic pnp of the nwell diode between RF_{IN} and V_{DD}. An overview of the TLP measurement results is presented in Table 5.8.

Since CDM robustness is more difficult to obtain than HBM, on-wafer VFTLP measurements have been performed between different pin-to-pin combinations to find weak spots in the design. The VFTLP pulses which arrive at the bondpad (i.e. after the probe needles) have 3 ns pulse width and 400 ps

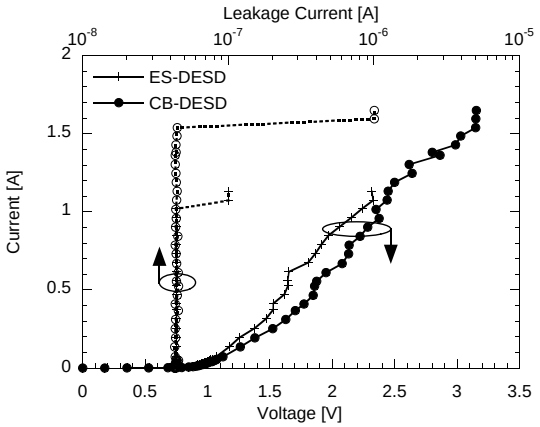

Figure 5.35: TLP-IV measurements for stress between V_{SS}+ and RF_{IN}-. CB-DESD has 50 % improved It_2 over ES-DESD.

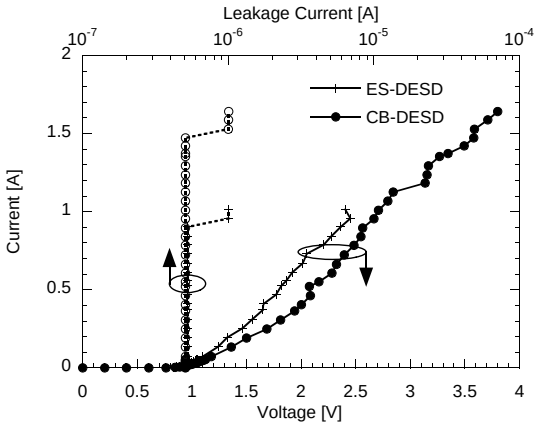

Figure 5.36: TLP-IV measurements for stress between RF_{IN}+ and V_{DD}-. CB-DESD has 65 % improved It_2 over ES-DESD.

rise time, which meets the CDM pulse specification given in the JEDEC standard [CDM 08]. An overview of the VFTLP measurement results is given in Table 5.9. Very high VFTLP values are obtained already for the reference ES-DESD design. Further, an average improvement with 32 % is obtained using CB-DESD, giving VFTLP results up to 12.8 A.

In both cases for all stress combinations, failure was visually observed in the ESD protection diodes of the first amplification stage. Also for CB-DESD, failure occurs at the first stage, indicating that at high current levels, the majority of the ESD current flows through the first stage, as was predicted by the HBM spectre simulations.

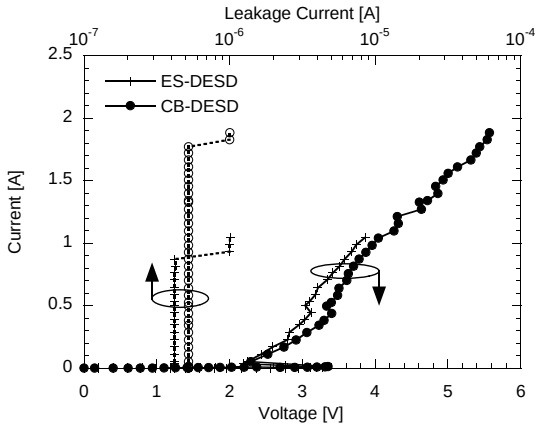

Figure 5.37: TLP-IV measurements for stress between $RF_{IN}+$ and V_{SS}-. CB-DESD has 100 % improved It_2 over ES-DESD.

Table 5.8: TLP measurement summary.

TLP [A]	**ES-DESD**	**CB-DESD**
$\boldsymbol{V_{SS}+RF_{IN}-}$	1	1.5
$\boldsymbol{RF_{IN}+V_{DD}-}$	0.9	1.4
$\boldsymbol{RF_{IN}+V_{SS}-}$	0.9	1.8

Table 5.9: VFTLP measurement summary.

VFTLP [A]	**ES-DESD**	**CB-DESD**
$\boldsymbol{V_{SS}+RF_{IN}-}$	9.5	12.8
$\boldsymbol{RF_{IN}+V_{DD}-}$	8.7	11.5
$\boldsymbol{RF_{IN}+V_{SS}-}$	9.2	12.1

5.4 State-of-the-Art Comparison

Only a few ESD protected wideband RF designs are available in literature. These designs are discussed below and compared to our results.

In [Sold 05], a classical dual diode ESD protection was implemented on a DC-5.7 GHz LNA, implemented in 0.13 μm CMOS technology. Such protection methodology yields a protection level of only 0.85 A TLP when stressing $RF_{IN}+$ to V_{SS}-, which is attributed to the bus resistance and required power clamp. Therefore, another solution is proposed which does not rely on a power clamp. A low-capacitive SCR solution conducts current directly from $RF_{IN}+$

to V_{SS}-, improving the ESD robustness up to 3 kV HBM. A common-gate implementation achieves a robustness of 5 kV. Since there is no decoupling capacitor at the RF input, any overshoot generated by the SCR is directly visible at the gate oxide of the core transistor. Therefore, such methodology should be carefully investigated in more advanced technologies under CDM stress conditions to prove its applicability. The main conclusion from this paper is that above 5 GHz, alternative ESD protection approaches will be required.

The limitations of the classical dual diode protection become clearly visible in [Borremans 07b], where they are used to protect a DC-6 GHz inductorless feedback LNA, implemented in 90 nm digital CMOS. A robustness of 3.2 kV HBM is measured between RF_{IN}+ to V_{DD}- and V_{SS}+ to RF_{IN}-. These pin combinations are easiest to protect and do not tell the full ESD story. In this design, no power clamp was implemented. Low ESD results are expected due to oxide breakdown for stress between RF_{IN}+ and V_{SS}-, especially for VFTLP. Moreover, we demonstrated in section 5.2 that besides the fragile gate oxide, also parasitic current paths through the core LNA can be the weak spot and therefore, all pin-to-pin combinations should be considered during ESD testing.

In [Bhat 06], the use of dual diodes has been extended to a 3-10 GHz LNA, implemented in 0.13 μm CMOS technology. In this design, a g_m enhancement technique is applied to a common gate amplifier, allowing for more freedom to add diode capacitance. An excellent robustness of 4.2 kV HBM is measured. When carefully evaluating this design, an inductor to ground was found parallel to the ESD protection diode between RF_{IN} and V_{SS} together with a decoupling capacitor. The ESD diodes were additionally added as the authors feared CDM problems due to voltage overshoots over the inductor, referring to [Hyvo 03b]. However, we have demonstrated in section 4.4, that by adding small clamping diodes inside the core circuit, a good CDM robustness can still be achieved, even in a 90 nm CMOS technology. As such, the additional ESD diodes are not needed, which would result in an RF improvement.

Besides low-capacitive solutions, other innovative wideband ESD protection methodologies were proposed. In [Galal 03], a T-coil is used to provide ESD protection for digital circuits up to 10 Gb/s, implemented in a 0.18 μm CMOS technology. This T-coil solution features an integrated noisy resistor in order to achieve input matching over the entire bandwidth, preventing it to be used for RF low-noise applications. Therefore, in section 5.2 we have updated this concept to make it usable for wideband RF circuits, which was demonstrated for a DC-16.1 GHz LNA in 90 nm CMOS.

Already in the year 2000, Kleveland reported the concept of distributed ESD protection for wideband digital and RF circuits [Klev 00], where the ESD protection elements are distributed along an artificial transmission line. Implemented in a 0.5 μm CMOS technology, the distributed ESD solution

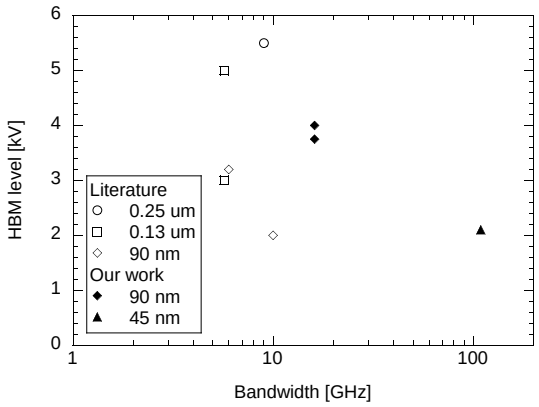

Figure 5.38: Benchmarking of our work (solid symbols) against other published wideband CMOS LNAs (open symbols). The HBM robustness [kV] is plotted as function of RF bandwidth [GHz].

consisted of a long (=bulky) transmission line with a rather large series loss. Therefore, Ker revisited this methodology in [Ker 05] to protect a 1-10 GHz DA, in a 0.25 μm CMOS technology. Codesign of each applification stage allowed the incorporation of ESD protection of decreasing size for each subsequent DA amplification stage, resulting in excellent ESD performance of 5.5 kV HBM. To avoid the RF-redesign of each stage to include the ESD protection elements, we have developed the Center Balanced Distributed ESD protection in section 5.3, where each stage has the same capacitive load of the ESD protection devices. Implemented on a DC-110 GHz DA in 45 nm CMOS with Above-IC, an improvement of at least 50 % in ESD performance was measured.

Finally, in [Soldner 07], an innovative technique is described where the parasitic capacitance of the ESD protection SCRs at the RF input is compensated by a bootstrapping feedback network. The penalty of this bootstrapping is that it uses an active feedback network which consumes power during normal operation, e.g. an additional power consumption of 19 mW for a 10 GHz amplifier in 90 nm CMOS technology. Further work is needed to optimize this methodology.

In Fig. 5.38, a graphical overview is given, where the results of our ESD protected wideband CMOS LNAs are benchmarked against literature. We achieved the highest HBM robustness levels for the highest bandwidths in the most advanced CMOS technologies in the world. Note that a similar comparison regarding VFTLP measurements is not possible since nobody else has published such results.

5.5 Conclusions

Providing adequate ESD protection for wideband RF circuits in CMOS is a challenge. Moreover, when these circuits are implemented in the most advanced CMOS technology nodes, larger RF-bandwiths can be obtained which increases the ESD design complexity. Simultaneously, the technology itself becomes more vulnerable to ESD stress.

Very few publications are availabe addressing ESD protection for wideband RF CMOS circuits, specifically for very advanced CMOS technologies. The current solutions are either limited in terms of RF performance, power consumption, ESD performance and/or area consumption as was discussed in section 5.4. Therefore, in this chapter two novel ESD protection techniques for wideband RF ESD protection are developed and demonstrated in 90 nm and 45 nm CMOS technologies up to frequencies of 110 GHz.

The T-coil protection from [Galal 03] was transformed into an ESD solution compatible with RF requirements, yielding the T-diode concept discussed in section 5.2. Using the T-diode, the parasitic capacitance of the dual-diode at the RF input is tuned out over a wide frequency band. Input matching was maintained from DC to 16.1 GHz, in a 90 nm digital CMOS technology. Two novel ESD techniques were introduced to improve the T-diode ESD protection. First, local clamping diodes provide a low resistive ESD path to ground, without relying on current conduction through the power clamp. The additional diode capacitance is compensated by the T-diode. Secondly, addition of turn-off circuitry ensures the turn-on of the power clamp before triggering of parasitic current paths in the core circuit. An ESD robustness of 4.5 kV HBM and 3.8 A VFTLP was measured.

A novel distributed ESD concept was developed, specifically for distributed amplifier circuits. The developed Center Balanced Distributed ESD protection improves current uniformity between the different ESD protection stages. It can be easily implemented without the need for redesign of each gain stage and has almost no impact on the RF performance of the circuit. A 1-110 GHz distributed amplifier in 45 nm CMOS was protected using this methodology, yielding an ESD robustness of 1.4 A TLP and 11.5 A VFTLP.

Chapter 6

Conclusions, Future Work and Outlook

ESD is not a showstopper for the introduction of FinFET technology, provided a design methodology to select the delicate layout optimum and adequate processing options are applied. Further, efficient ESD solutions can be implemented for narrow- and wideband RF circuits which exhibit both excellent RF and ESD performance.

6.1 Conclusions

In this thesis, two major challenges for ESD protection design have been addressed. First, the basic ESD performance of common protection devices implemented in a SOI FinFET technology has been analyzed. Large dependencies on device layout parameters and process options have been found. This has fueled the need for a specific normalization method for accurate data interpretation and the development of a design methodology to optimize the ESD protection structures. Secondly, new ESD protection techniques have been developed for both narrow- and wideband RF circuits. These solutions were shown to have excellent HBM and CDM robustness without significantly degrading the RF performance. To perform this in depth research, new measurement equipment and calibration methods have been developed, which enabled ESD evaluation of the devices and circuits under more realistic ESD stress conditions.

In Chapter 2, the basic component-level ESD stress models have been discussed together with various TLP implementations. These have served as an input to develop more enhanced ESD characterization and analysis techniques. By using a multi-level TLP system, accurate holding voltage determination was

made possible, without being limited by the system loadline. Besides the quasi-static device behavior which is obtained from TLP measurements, also the transient device respons could be obtained by analyzing the TLP voltage and current waveforms. These waveforms were calibrated to remove the system parasitic contributions, revealing the true device behavior. Voltage and current waveforms have been captured during HBM stress, yielding an HBM-IV curve for each HBM stress level. Besides the same quasi-static device information as obtained from TLP, also HBM transient effects could be studied. A few examples of miscorrelation between TLP and HBM have been presented, highlighting the usefulness of HBM-IV.

In Chapter 3, the ESD performance of grounded gate MOS devices and gated diodes, implemented in a FinFET technology has been studied. Compared to bulk technologies, an area efficiency of 50 % for NMOS and 30 % for gated diodes was measured. ESD robustness scaling with device width was demonstrated, yielding several kV HBM levels for multi-finger multi-fin devices. On the other hand, voltage clamping capability seemed more of a concern due to the reduced oxide breakdown voltage. The influence of various geometrical parameters on the ESD robustness has been studied. Besides yielding guidelines on how to optimize the device layout for best ESD performance given a set of functional constraints, prediction of the ESD behavior of future FinFET processing targets could be established. A performance drop of 50 % was predicted for the 22 nm FinFET technology node based on further downscaling of the geometrical device parameters. However, the ESD performance was found to also heavily depend on the different process options. A large ESD performance improvement was measured using SEG, which will be standard for the 22 nm node, and which will restore the ESD performance of the 22 nm node to a certain extent.

In Chapter 4, the scaling limitations of the classical dual diode protection were demonstrated. A codesign approach was presented as an alternative solution where the ESD protection was integrated into the RF design. As such, the use of low-capacitive ESD protection could be extended to higher frequencies, however with limited ESD robustness. When RF frequencies further increase, novel ESD protection strategies are required. We presented an inductive based ESD protection approach, either implemented as a “plug-and-play” inductor to ground, or using an RF-ESD codesigned transformer. The impact of inductor-based ESD protection on narrowband RF circuits was studied and their HBM and CDM performance was evaluated. Even though many people question the use of inductive elements for CDM protection, a high VFTLP robustness level was achieved provided high-quality inductors and voltage clamping diodes are used. By codesigning the inductor to ground into a transformer, no additional area was required for the ESD inductor. When technology scales further down, higher RF operating frequencies can be achieved. Therefore, the required inductance of the ESD protection inductor could be decreased, leading to

an improved RF performance, ESD performance and area consumption. As such, the inductor to ground methodology is preferred over the transformer based solution because of the reduced design complexity. Very high ESD levels of 6.3 kV HBM and 7.3 A VFTLP were demonstrated on a 60 GHz LNA, implemented in a 45 nm CMOS technology.

In Chapter 5, two novel wideband RF-ESD protection strategies were presented to overcome the limitations of the current solutions, in terms of RF performance, power consumption, ESD performance and area consumption. The developed T-coil protection was used to tune out the parasitic ESD diode capacitance over a wide frequency range, and was demonstrated to work up to 16 GHz. To improve the ESD robustness, local clamping at the RF input to the power rails was implemented, and the additional capacitance was compensated by the T-coil network. Turn-off circuitry was added to turn-off any parasitic current path through the core circuit during the ESD stress. These improvements resulted in an ESD robustness of 4.5 kV HBM and 3.8 A VFTLP on a 90 nm CMOS LNA. Further, a novel distributed ESD concept was developed, improving the current uniformity between the different ESD protection stages. An increase with 50 % TLP and 32 % VFTLP over the conventional solution was obtained on a 1-110 GHz DA in 45 nm CMOS.

6.2 Future Work

At the end of this PhD, I would like to make some recommendations for future research in this field.

1. As many manufacturers of integrated circuits face the difficulty of providing reliable products to system vendors even without knowing the final application, a clear need is present to correlate system-level ESD behavior with component-level ESD characterization results. The first steps have been taken in section 2.3.2, where on-wafer measurements of system-level stress using the Human Metal Model (HMM) were performed. First results indicated a large dependence of the correlation factor between HBM and HMM, depending on the device type being considered. More understanding is needed regarding the underlying physical reasons for such differences. Future work will need to address the relationship between ESD robustness on wafer-level, package-level and complete system level.
2. The ESD performance evaluation performed in this thesis on SOI FinFET devices needs to be further expanded. Some items are still open regarding the impact on area efficiency by folding of the multi-finger transistors, and regarding the different failure mechanisms in multi-fin grounded gate NMOS transistors. For the latter, failure analysis should provide

clear answers. Future work to study the turn-on and failure uniformity of FinFET devices is planned using Transient Interferometric Mapping (TIM) [Furb 00]. The TIM technique is a powerful tool to analyze internal temperature and free carrier distribution in ESD protection devices, but it is a question whether high enough spatial resolution for FinFET devices can be reached.

3. In this thesis, FinFET devices are fabricated on SOI substrate. However, SOI wafers have disadvantages with respect to their self-heating properties, cost, defect density etc., when compared to bulk silicon substrates. In addition, bulk silicon substrates are compatible with the existing standard planar CMOS process technologies [Okan 05]. It is therefore useful and cost-effective to implement FinFET technology on bulk silicon wafers. A TEM cross-section of a multi-fin bulk FinFET is shown in Fig. 6.1. Only the top part of the fin above the SiO_2, indicated by H_{fin}, is surrounded by the gate. The fin is connected by a triangular shape to the silicon substrate, which makes the fin height definition difficult. First characterization results have been performed on bulk FinFET structures and are compared to SOI FinFET results. Fig. 6.2 shows the IV curves for both bulk and SOI narrow-fin NMOS FinFETs with different gate length stressed in parasitic bipolar mode. For SOI FinFETs no snapback is observed as the parasitic BJT has its base floating. For bulk FinFETs no snapback is observed for short gate lengths ($\leq$ 70 nm) either, while for medium and long gate lengths the IV curves are similar to the ones of planar MOS technologies, where the holding voltage is distinct from the triggering voltage. A different L_g dependency of It_2 is observed. For SOI FinFET, It_2 increases with increasing L_g, as the current uniformity at high current levels increases with increasing L_g, and slightly drops down for the largest L_g, as the dissipated energy is increased due to the increase in voltage drop (V_h). This leads to a maximum intrinsic It_2 (11.5 mA/μm) at medium L_g. On the contrary, for bulk FinFETs It_2 decreases monotonically with increasing L_g, leading to a maximum intrinsic It_2 (41.1 mA/μm) at the smallest L_g. This higher robustness can mainly be attributed to the trapezoidal fin shape of bulk FinFETs (Fig. 6.1), which improves the heat dissipation through the bulk silicon and to the increased junction area because of the addition of the bottom junction. Moreover, for medium and long L_g, It_2 is unexpected lower than for SOI FinFETs. Gate-oxide breakdown could be the reason for this early failure. An improvement up to 3.5x in maximum It_2 is observed for narrow-fin bulk FinFETs over SOI FinFETs. More details on these initial results on the ESD performance of bulk FinFET devices can be found in [Griff 09].
4. Throughout this thesis, several narrow- and wideband RF-ESD protection methodologies have been developed and analyzed regarding their ESD and RF performance. A lot of further research still can be done in this

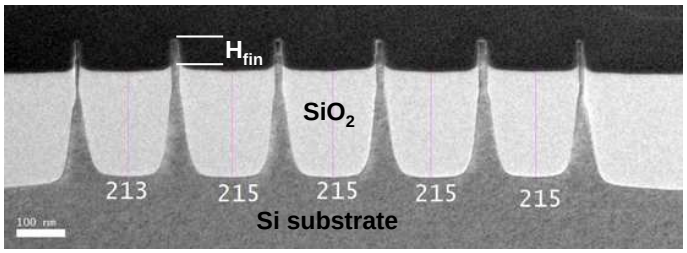

Figure 6.1: TEM cross-section of a multi-fin bulk FinFET.

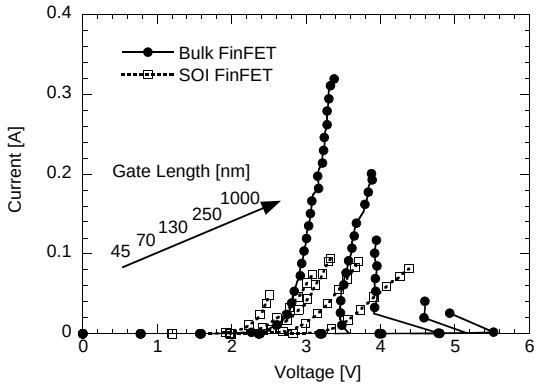

Figure 6.2: TLP-IV curves for NMOS bulk and SOI FinFETs in parasitic bipolar mode with different gate lengths. The devices have 20 nm fin width, 180 nm fin spacing, and 400 fins in parallel.

field to develop new ideas which can be applied to the most advanced technologies and for the highest RF frequencies. VFTLP measurements have been used in this work in order to assess the CDM robustness of these ESD protected RF circuits on wafer-level, without the need of packaging. Since the actual discharge current path during a CDM event differs from two-pin VFTLP testing, VFTLP measurements were performed on all possible pin-to-pin combinations for both polarities. As such, the weakest path could be found and strengthened. Future work would require real CDM measurements on packaged samples in order to determine the correlation factor with the VFTLP results.

6.3 Outlook

To conclude this thesis, a brief outlook for future ESD research is given. Due to an explosively growing number of technology options, tremendous challenges are posed to the ESD protection community.

Besides novel device architectures such as 3D-FinFET devices, also new materials may be used to continue down Moore's road. New high mobility channels such as germanium and III-V compounds may be needed for future device generations.

In general, ESD protection for high voltage technologies still holds a lot of challenges.

Further, the study of the reliability and failure mechanisms of Micro Electro-Mechanical System (MEMS) actuators under ESD stress has received increasing attention in recent times. Very high sensitivity levels towards ESD have been demonstrated already for micromirrors. RF-MEMS ohmic and capacitive switches have also been shown to have serious reliability problems both under DC and ESD stress.

Carbon Nano Tubes (CNT) and graphene nanoribbons are currently being researched since they have many properties, from their unique dimensions (a diameter close to 1 nm, while their length can be up to 1000 times longer) to an unusual current conduction mechanism, that make them ideal components for electrical circuits. No ESD results have been published so far.

IMEC recently demonstrated the first functional 3D integrated circuits obtained by die-to-die stacking using 5 μm Cu Through-Silicon Vias (TSV). 3D integration seems promising for system integration with applications ranging from electronics for consumer, automotive and medical applications. During the stacking process, CDM-like discharge events could occur from die to die and therefore adequate ESD protection would be required. Due to increased interconnect resistances across the different dies, novel ESD protection strategies might be required.

Other exciting new technology developments include biosensors, neurons-on-chip, plastic and organic electronics, etc. Little or nothing is known how these technologies behave under ESD stress conditions. Therefore, there are many unexplored ESD problems which are waiting for new solutions.

ESD will remain a challenge for the next years to come!

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Curriculum Vitæ

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