A Methodology for Measuring Transistor Ageing Effects Towards Accurate Reliability Simulation

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Abstract—Emerging die-level stress effects (i.e. NBTI, HCI, TDDB, etc.) in nanometer CMOS technologies cause both analog and digital circuit parameters to degrade over time. To efficiently evaluate these degradation effects in modern ICs, a reliability simulator, using accurate first order degradation models, is needed. In this work, we propose a new measurement workflow addressing several modelling and measurement issues involved with developing these new degradation models. A new on-the-fly measurement technique, avoiding complicated NBTI relaxation problems, is introduced. This technique provides a complete set of easy-to-use modelling parameters and allows the modelling of both DC and AC stress effects in all transistor operating regions. To eliminate large extrapolation errors, we also propose a simple measurement circuit suited for fast and accurate degradation modelling at nominal voltages and temperatures. Avoiding the use of complicated and technology restricted transistor models, this new methodology is very flexible and can be used over a broad range of nanometer CMOS processes.

I. INTRODUCTION

Increasing reliability challenges due to high electric fields in modern CMOS technologies raise the need for reliability-aware design. According to the ITRS roadmap both analog and digital ICs start to suffer from die-level reliability phenomena, for example Negative Bias Temperature Instability (NBTI) and Hot Carrier degradation (HC) [1], [2]. An in-design reliability simulator using accurate and fast to evaluate degradation models is needed in order to develop robust analog and digital designs in a increasingly unreliable technology. However, originating in very complex nanometer CMOS processes, these effects are discovered to be extremely difficult to model. Degradation phenomena are affected by a large number of mutually interacting parameters (e.g. voltages, temperature, dimensions, etc.). In addition, some phenomena (e.g. NBTI) also suffer from relaxation effects after stress relieve [3]. The very long time-scale over which transistors degrade, forces researchers to overstress devices to obtain measurement results in a reasonably short time-frame. However, this technique might introduce other or more severe degradation effects not present at nominal stress voltages and temperatures (i.e. under normal operating conditions). Furthermore, to be compatible with a digital or analog reliability simulator, degradation models should be able to cope with a broad range of time-varying, voltage and temperature dependent stress factors. The models should also be characterised for different transistor sizes. Degradation models, based on conventional measuring techniques, do not combine these modelling issues and are

therefore not always sufficiently accurate or suited for a reliability simulator.

This paper proposes a simple, straightforward workflow that allows the reader to accurately develop models for deterministic degradation phenomena (e.g. NBTI, PBTI, HC, etc.) in any arbitrary nanometer CMOS technology. This workflow has a number of advantages over existing techniques:

- It is applicable over a broad range of nanometer CMOS processes.
- It allows on-the-fly parameter extraction avoiding complication by NBTI relaxation effects.
- It offers a complete set of transistor parameters covering both DC and AC degradation behavior.
- It provides fast and accurate results at low-voltage stresses avoiding extrapolation problems.
- It is applicable to several deterministic degradation effects.

To obtain this result, a careful study of different measurement and modelling problems, associated with the most important degradation phenomena, was performed. The workflow intends to be a useful tool to get a first order estimate of the impact of degradation on digital and analog circuits [4]. As such it is complementary to existing measurement techniques intended to understand the physical nature of different degradation effects [3], [5]. Combining both should allow us to develop models, for common deterministic degradation effects, well suited for analog and digital circuit reliability simulation.

Section II of this paper briefly situates the different problems associated with modelling die-level degradation effects and proposes a new workflow to cope with these problems. In the following sections, different aspects of the workflow are explained in more detail. Section III introduces a new methodology to perform on-the-fly (i.e. relaxation-free) measurements while section IV proposes an addition to this methodology to measure and verify degradation at low stress voltages using a replica circuit. Finally, conclusions are drawn in section V.

II. DEGRADATION MODELS FOR CIRCUIT SIMULATION

Emerging reliability problems demand solutions at circuit level to assure reliable circuits in modern nanometer CMOS processes. Also, ever-narrowing design margins need to be increased wherever possible in order to get better performing systems and to avoid overdesign. To cope with these issues reliability simulators, capable of detecting reliability problems

Fig. 1. Conventional models introduce large extrapolation errors due to small measurement errors at large stress voltages.

Fig. 2. A new workflow allows the design of time-varying aware degradation models with smaller extrapolation errors at low stress voltages.

in both analog and digital circuits, need to be developed. In literature, different simulator methodologies have been proposed [4], [6], [7], [8]. For digital circuit simulation, DC only simulations provide a good insight in the behavior of a circuit over time. In analog circuits, however, subtle variations between matched transistors can already cause huge problems. Here, analog (AC) stress signals need to be taken into account when calculating the degradation.

Both analog and digital reliability simulators intend to estimate the degradation of a circuit operating at nominal stress voltages. Conventional degradation models, however, are developed using measurement results originating from overstressed devices, since this guarantees significant degradation in a reasonable measurement time. Fig. 1 indicates how conventional modelling techniques can lead to significant extrapolation errors when predicting degradation at nominal stress values. Here, a limited number of measurements at fairly high stresses (i.e. around 2.0V) leads to a first order DC model. Different measurements at the same stress voltages lead to slightly different model parameters. However, evaluating the models at lower stress voltages quickly introduces huge extrapolation errors for both models.

Fig. 2 presents a schematic overview of the new workflow which enables degradation measurements to cope with both above-mentioned modelling problems. First, a literature study provides insight in a particular degradation phenomenon. This study can also deliver a first order model for the effect and provides different stress and geometrical factors affecting the degradation phenomenon (e.g. transistor length, gate and drain voltages, temperature, etc.). Different measurements at high stress voltages, for various combinations of these factors,

combined with low voltage stress measurements, leads to a final degradation model. This final model is capable of handling both AC and DC stress effects and is fairly accurate over a broad range of input stress voltages. In the next two sections every new part in this workflow is explained in more detail.

III. PERFORMING ON-THE-FLY TIME-VARYING STRESS MEASUREMENTS

In this section, a new on-the-fly technique to measure the degradation of transistor parameters is proposed. The methodology is based on a physical understanding of different degradation mechanisms and uses a basic transistor circuit to extract the effect of degradation without stress relieve. Since it is applicable to any deterministic degradation effect, the technique allows to consistently characterise degradation in a new CMOS technology and develop practical degradation models for simulation purposes.

A. Measurement issues

Hot Carrier degradation (HC) and Negative Bias Temperature Instability (NBTI) are considered to be two of the most important effects regarding analog and digital circuit operation [2]. HC degradation does not have a significant relaxation component [9] and can therefore be modeled using interrupted stress measurements. NBTI, however, has a significant relaxation component due to which conventional measurement techniques tend to underestimate the degradation behavior [3], [5]. Several techniques (e.g. direct-current current-voltage or DCIV and charge pumping) have been developed to accurately measure NBTI degradation [3]. However, these techniques are intended to study the origin of NBTI degradation and relaxation mechanisms in different CMOS technologies. They are less suited to develop useful models for reliability simulation, especially for analog CMOS. These measurements are often limited to DC stress conditions and use restricted stress conditions to prevent other degradation effects from happening (e.g. NBTI measurements with limited drain source voltage to prevent HC effects). The technique presented here is both applicable to PMOS and NMOS (i.e. can be used to model HC, NBTI and PBTI) and is also useful when modelling the effect of time-varying (AC) stress voltages.

Fig. 3 illustrates how different stress factors create interface and oxide traps, in its turn shifting important transistor model parameters and therefore influencing transistor performance parameters (e.g. drain current, current noise, etc.).

These performance parameters are the only effect of degradation that can be measured directly. Nanometer scale transistors have a ever-increasing complex behavior due to short-channel effects (e.g. velocity saturation, DIBL, channel length modulation, etc.). Therefore the nominal behavior of transistors in a 90nm process and beyond is described using very complicated transistor models (e.g. BSIM or EKV models) with over 200 physical and process dependent parameters. Moreover, when going to 45nm and beyond, today's transistor models will be replaced by a more advanced and completely

Fig. 3. Transistor stress factors affect external transistor characteristics. φ is the phase difference between gate and drain voltage, N_{IT} and N_{OT} are the number of interface and oxide traps, β is the carrier mobility, λ is the channel length modulation factor, γ is the bulk modulation factor and n is the subthreshold slope.

Fig. 4. Basic setup to measure transistor degradation effects on NMOS and PMOS devices under large stress voltages.

different model (i.e. the PSP model [10]). Finding sufficiently accurate equations to extract the effect of degradation on some of the most important transistor parameters (e.g. the threshold voltage V_{TH} or the carrier mobility μ) is therefore not only very hard but is also limited to the technology for which these equations are valid. In this work we propose the extraction and modelling of only externally measurable performance characteristics, describing the degradation of both DC and AC transistor behavior. This provides several advantages:

- 1) On-the-fly measurement (i.e. without relaxation effects) is possible.
- 2) Performance characteristics describing both DC and AC behavior of the transistor allow a full coverage of varying transistor parameters.
- 3) Model errors are limited to measurement errors.

B. Measurement setup

To measure transistor characteristics without stress relieve, a one stage resistive amplifier, as depicted in Fig. 4, is used. Stress voltages are applied to the transistor via the gate (V_G) and drain (V_{DD}) voltage. The applied stress voltages can have a time-varying (AC) behavior superimposed on top of a constant (DC) stress (i.e. $V_G = V_{GS} + V_{gs}$). A very small resistor R (e.g. 10Ω) allows to monitor the transistor drain current I_D , by measuring the voltage drop over the resistor (also see Fig. 4). Fig. 5 indicates how, depending on the operating region of the transistor and the type of stress voltages (DC only or DC and AC), different characteristics can be measured. Voltages at the different nodes of a transistor are considered as inputs, where the transistor drain current is considered an output with a time-dependent behavior due to

Fig. 5. Flowchart indicating the stress-measurement flow of a transistor under a given stress. Stress voltages are applied at the input, transistor characteristics based on the drain current behavior are measured at the output.

Fig. 6. Measurement scheme to extract the output conductance. Gate and drain voltage stress schemes (top) and current output (bottom).

transistor degradation. A DC stress at the gate of the transistor (V_{GS}) manifests itself as a DC current (I_{DS}). This current can be measured and degrades over time:

$$I_{DS}(t) = I_{DS}(0) + \Delta I_{DS}(t) \quad (1)$$

An AC stress at the gate initiates an AC current (I_{ds}) which allows to monitor the transconductance degradation:

$$\frac{I_{ds}}{V_{gs}}(t) = \frac{dI_{DS}}{dV_{GS}}(t) = g_m(0) + \Delta g_m(t) \quad (2)$$

To calculate the voltage gain of a transistor when it is in saturation (i.e. $V_{GS} - V_{TH} < \min(V_{DS}, V_{DSAT})$), its output conductance is also needed. To extract the output conductance the drain voltage is varied over a very short time while measuring the drain current (see Fig. 6), giving:

$$g_o(t) = \frac{I_{DS1} - I_{DS2}}{V_{DS1} - V_{DS2}}(t) \quad (3)$$

where I_{DS1} and V_{DS1} represent one voltage-current pair and I_{DS2} and V_{DS2} represent another. Interrupted or varied V_{DS}

stress does not cause significant relaxation effects since the oxide electric field (E_{ox}) is the dominant source for transistor degradation [9]. Therefore this methodology, using a varying V_{DS} to measure the output conductance, is still considered an on-the-fly measurement. On Fig. 5 all different measurements (executed by a monitor) are included as part of a loop with a timer to decide when to measure again. The timer triggers the monitor at logarithmically distributed time points, because both HC and NBTI have a behavior with a logarithmic time dependence.

C. Extraction of transistor parameters

In section III-A we indicated how hard it is to find quantitative results for the degradation of transistor model parameters (e.g. the threshold voltage degradation). However, using first order transistor equations we can still gain qualitative insight in the impact of degradation on these parameters. For a transistor in linear region for example:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta \beta}{\beta} - \frac{\Delta V_{TH}}{V_{GS} - V_{TH}} \quad (4)$$

$$\frac{\Delta g_m}{g_m} = \frac{\Delta \beta}{\beta} \quad (5)$$

where β represents a term including the transistor size (W/L), the oxide capacitance (C_{ox}) and the carrier mobility (μ). Equation (4) and (5) describe the relative time-dependent variation of two transistor characteristics and are, in very first order, also valid for a transistor in velocity saturation. These equations can provide additional insight for designers although they do not give accurate estimates for the degradation of separate transistor parameters.

IV. LOW VOLTAGE STRESS MEASUREMENTS

As explained in section II, degradation models will be used under nominal stress conditions. However, classically the models are fitted with measurements originating from overstressed devices. Therefore, model extrapolation is needed and huge errors can be introduced. To avoid this, degradation measurements at nominal stress voltages are also needed. Unfortunately, a measurement structure as proposed in section III is not adequate here, since any degradation effect under low stress voltages will be very small, if measured over a short time. Therefore, a small, unintended, variation of the stress voltages V_{GS} or V_{DS} (e.g. due to temperature variation), can already corrupt the measurement results:

$$\frac{\Delta I_{DS}}{I_{DS}} \propto \frac{\Delta \beta}{\beta} + \frac{-\Delta V_{TH}}{V_{GS} - V_{TH}} + \frac{\Delta V_{GS}}{V_{GS} - V_{TH}} \quad (6)$$

where $\frac{\Delta I_{DS}}{I_{DS}}$ represents the current variation of a transistor in linear region. ΔV_{GS} is negligible for severely degraded transistors (which is true under large stress). However, ΔV_{GS} can be considerably large compared to ΔV_{TH} and $\Delta \beta$ under nominal stress conditions over a short time. To eliminate these problems, a differential structure (see Fig. 7) is used to obtain a good estimate for the transistor degradation under low voltage stress conditions. The differential output voltage

Fig. 7. Measurement setup for degradation modelling under low voltage stressing. Stress phase (left) and measurement phase (right).

is insensitive to variations of the supply and gate voltage, but is very sensitive to variations between the two transistors. Fig. 7 (left) indicates how, in a first stage, the transistor under test M_1 (indicated in a gray box) is stressed by V_G and V_{DD} . A reference transistor M_2 , together with one of the current sources, is turned off. When measuring the degradation of the transistor under test (Fig. 7 (right)), two current sources are used to keep the stress on transistor M_1 constant and avoid relaxation effects. Transistor M_2 acts as a reference transistor. Using this structure, very small time-dependent variations of both the DC current I_{DS} and the transconductance g_m can be measured. Remark how this differential structure (Fig. 7) is essentially formed by adding a replica to the structure presented in section III. As such, this new setup can also be used to study transistor degradation under high stress voltages and is compatible with the workflow presented in Fig. 5.

A. Calculation of the DC current degradation

When applying a DC voltage at the gate of M_1 and M_2 , the degradation of the DC current, ΔI_{DS} , can be calculated from the offset voltage at the output of the differential pair:

$$V_{OUT} = g_m R \left(\frac{\Delta R}{R} + \frac{-\Delta V_{TH}}{V_{GS} - V_{TH}} + \frac{\Delta \beta}{\beta} \right) \quad (7)$$

where M_1 and M_2 are assumed to be in velocity saturation. Similar equations can be derived for other transistor operating regions. From equation (7), we can calculate the sensitivity of the output voltage to different varying components:

$$S_{V_{GS}}^{V_{OUT}} = g_m R \frac{\Delta V_{TH}}{(V_{GS} - V_{TH})^2} \frac{V_{GS}}{V_{OUT}} \quad (8)$$

$$S_{\Delta V_{TH}}^{V_{OUT}} = g_m R \frac{1}{V_{GS} - V_{TH}} \frac{\Delta V_{TH}}{V_{OUT}} \quad (9)$$

$$S_{\Delta \beta}^{V_{OUT}} = g_m R \frac{1}{\beta} \frac{\Delta \beta}{V_{OUT}} \quad (10)$$

Clearly, the output voltage is insensitive to variations of the gate voltage V_{GS} , since its sensitivity is directly proportional to the threshold voltage offset, which is very small.

The output voltage of the differential pair V_{OUT} gives an indication for the degradation of transistor M_1 (also see equation (7)). However, to compare this result with accelerated stress measurements (see section III) the drain current degradation

Fig. 8. Extraction of the current difference between two sides of a differential pair, using the differential output of the amplifier.

ΔI_{DS} needs to be extracted. On Fig. 8 the drain current I_{DS} is plotted as a function of the drain voltage V_{DS} . Using the load line of the resistor we get:

$$\tan(\alpha) = \frac{V_{DD}}{RV_{DD}} = \frac{1}{R} \quad (11)$$

and

$$\tan(\alpha) = \frac{\Delta I_{DS}}{\Delta V_{DS}} \quad (12)$$

Combining (11) and (12), we get an expression for the relative DC current degradation:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta V_{DS}}{I_{DS}R} = \frac{V_{OUT}}{I_{DS}R} \quad (13)$$

On Fig. 8 the two resistors of the differential pair are considered equal. However, a mismatch between the two resistors will affect the difference in drain current, calculated from the offset voltage:

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{V_{OUT}}{I_{DS}R} - \frac{\Delta R}{R} \quad (14)$$

where $\frac{\Delta R}{R}$ represents the relative mismatch between the two resistors. Initial transistor mismatches, due to process variations, will also create an initial offset voltage V_{OUT} . However, these initial mismatches do not change over time if the resistors R are chosen sufficiently small compared to the output resistance of the transistors. Any variation of the DC current is therefore a result of transistor degradation. On Fig. 9 a simulation of the proposed low voltage stress measurement technique is depicted. The X-axis represents the percentual increase in mismatch (due to degradation) compared to the initial mismatch (due to process variations). On the Y-axis the error on the extracted DC current degradation is plotted. Very small mismatch increase, caused by transistor degradation, brings about large errors due to measurement errors (e.g. $\varepsilon = 20\%$ for $\frac{\Delta V_{TH}}{V_{TH0}} = 0.1\%$). Very large values of degradation cause distortion in the circuit which also leads larger measurement errors (e.g. $\varepsilon = 50\%$ for $\frac{\Delta V_{TH}}{V_{TH0}} = 1000\%$). The circuit is most accurate for an offset degradation in the same order of magnitude as the initial offset due to process variations. Therefore, to be able to measure very small degradation effects, both the resistors and the transistors of the differential pair should be matched very carefully when lay-outing the circuit. The plot on

Fig. 9. Simulation of the DC current degradation indicates a good accuracy of the proposed measurement methodology despite the use of first order transistor models.

figure 9 is obtained using complex transistor models including short channel effects. Therefore, this graph also proves the presented method to be very useful, although it is based on first order transistor equations.

Temperature variations will also affect resistor and transistor behavior. However, the temperature of the different circuit components can always be considered equal and therefore temperature dependent parameters at both sides of the differential pair will shift equally under temperature variations without affecting the differential output voltage V_{OUT} .

B. Calculation of the transconductance degradation

The differential pair in Fig. 7 also allows to estimate very small variations of the transconductance. To do this, an AC signal needs to be superimposed on top of the DC stress signal at the gates of both M_1 and M_2 . The differential AC output V_{out} on top of the DC offset V_{OUT} can then be expressed as:

$$V_{out} = V_{gs}((g_m + \Delta g_m)(R + \Delta R) - g_m R) \quad (15)$$

$$\approx V_{gs}(\Delta g_m R + g_m \Delta R) \quad (16)$$

$$(17)$$

which results in:

$$\frac{\Delta g_m}{g_m} = \frac{V_{out}}{I_{ds}R} - \frac{\Delta R}{R} \quad (18)$$

Again, initial mismatches will create an initial V_{out} , while a time-dependent degradation of M_1 will create an additional Δg_m .

C. Degradation amplification

When stressing a transistor under nominal voltages, the offset voltage at the output of the differential pair can be very small. Using a cascade of differential pair structures (see Fig. 10) allows to on-chip amplify the offset of the first structure, eliminating signal noise as much as possible. The first amplifier in Fig. 10 is designed identical to the differential pair in Fig. 7, the next amplifiers are optimized for high gain. The first transistor of the first amplifier is the transistor under test and is stressed, the other amplifiers are intended for reference and amplification purposes. Longer cascades of differential amplifiers can also be used. However, this is limited by voltage clipping at the output of the amplifier chain, introducing faulty measurement results.

Fig. 10. Cascaded differential pair structure to amplify transistor degradation.

D. Measurement accuracy at nominal stress voltages

In this paper, we measure transistor degradation under nominal stress voltages with a differential structure. However, despite the use of a replica circuit, noise and a limited accuracy of the measurement itself can still introduce a significant error on the measured output voltage (cfr. Fig. 7). This is especially true when measuring very small degradation effects over a short stress time (e.g. 2 hours). However, since these nominal stress voltage measurements are complementary to results obtained from overstressed devices, these measurements can still improve the uncertainty on calculated model parameters. To illustrate this, we took a simple DC NBTI model from literature [2]:

$$D(t) = C \exp(\alpha V_G) t^n \quad (19)$$

where D represents the transistor degradation (e.g. degradation of the DC current, I_D), V_G is the applied stress voltage, t the stress time and C , α and n are parameters depending on the used technology and the measured ageing effect. Linearizing this model, by applying a logarithmic operation, and evaluating it at one time instance, we get a linear equation with one variable parameter; V_G :

$$D' = [\log(C) + n \log(t)] + \alpha V_G \quad (20)$$

$$= K_1 + K_2 V_G \quad (21)$$

To get an estimation of the technology parameters (K_1 and K_2) used in this model, we perform a number of measurements with k different values for V_G : $V_{G,i}$ with $i = 1 \dots k$ resulting in k values for D' : D'_i with $i = 1 \dots k$. A least square fit algorithm gives an estimation for the model parameters K_1 and K_2 . Any measurement error will propagate to the model parameters, resulting in a non-zero variance of these parameters:

$$\sigma_{K_1}^2 = \frac{\sigma_{D'}^2 \sum_{i=1}^k V_{G,i}^2}{\Delta} \quad (22)$$

$$\sigma_{K_2}^2 = \frac{k \sigma_{D'}^2}{\Delta} \quad (23)$$

with

$$\sigma_{D'}^2 = \frac{\sum_{i=1}^k (D'_i - K_1 - K_2 V_{G,i})^2}{k} \quad (24)$$

$$\Delta = k \sum_{i=1}^k (V_{G,i} - \bar{V}_G)^2 \quad (25)$$

with $\bar{V}_G$ the average value for V_G . If measurements at overstress are completed with nominal stress measurements, parameter Δ will increase (due to a larger spread of parameter V_G). Even though the relative error on these extra measurements is larger, the absolute error remains the same (signal noise and measurement accuracy are considered constant), therefore $\sigma_{D'}^2$ will not change. From equations (22) and (23), we can thus conclude that the accuracy of the measurements will increase if nominal stress measurements are completed with overstress measurements, since both variances $\sigma_{K_1}^2$ and $\sigma_{K_2}^2$ will decrease.

V. CONCLUSIONS

In this paper we proposed a new workflow to measure degradation effects in nanometer CMOS technologies. The methodology is the result of a careful study of measurement and modelling issues involved in modelling of deterministic degradation effects. Two major new techniques were introduced. A true on-the-fly measurement technique allowing to model the effects of time-variant stress voltages characterises both DC and AC degradation effects. And, in addition, a measurement circuit, using a replica design, to model the degradation of transistors under low stress voltages allows to verify and characterise a degradation model under low voltage conditions and avoids large extrapolation errors. The proposed techniques are combined in a very straightforward workflow allowing to end up with efficient and accurate degradation models suited for reliability simulators and modelled in every transistor operating region. Using a digital decoder and an array of the presented test-structures, the user can develop a test-chip with a limited number of bondpads but he can still maintain the ability to stress multiple test structures under different stress conditions.

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