Area-driven optimisation of switched-capacitor DC/DC converters

T.M. Van Breussegeem, M. Wens, E. Geukens, D. Geys and M.S.J. Steyaert

Popular capacitive DC/DC converter topologies are optimised and compared towards the total required capacitance. The analysis shows that from an area point of view the series-parallel, Fibonacci and Dickson topologies perform equally. The voltage doubler topology is proven to be inferior.

Introduction: The chip area and as such the cost of a capacitive DC/DC converter is dominated by the total capacitance of the single chip switched-capacitor DC/DC converter. Therefore four N -stage switched-capacitor DC/DC converter topologies are analysed with respect to the total required capacitance. The utmost important characteristics of a DC/DC converter are its voltage conversion ratio (VCR) and its maximum attainable output current. The VCR is defined as the ratio of its output voltage to its input voltage.

Voltage doubler: The first topology is the voltage doubler topology [1] shown in Fig. 1a. The VCR of this topology will not increase linearly with the number of stages. The ideal VCR is 2^N , in which N is the number of stages. Charge balance techniques [2] are used to determine the output voltage in (1). In order to maximise the output voltage for a certain number of stages N , the second term of this equation is minimised. By means of extrema determination techniques the capacitance values which do this are calculated in (2) and (3). If these capacitance values are substituted in (1), the maximum output voltage is calculated in (4). By substituting: $k = 2^N - 1$ into (4) and isolating C_{tot} from this equation, the total capacitance is given as a function of k instead of N (5). This substitution makes it possible to compare the super linear topologies with the linear ones. $K + 1$ is the VCR of this topology.

$$V_{out} = 2^N V_{in} - \frac{I_{out}}{f} \left(\sum_{i=1}^N \frac{2^{2(N-i)}}{C_i} + \sum_{i=1}^{N-1} \frac{2^{2(N-1-i)}}{C_{oi}} \right) \quad (1)$$

$$C_i = \frac{2^{N-i}}{2^N + 2^{N-1} - 2} C_{tot} \quad (2)$$

$$C_{oi} = \frac{2^{N-i-1}}{2^N + 2^{N-1} - 2} C_{tot} \quad (3)$$

$$V_{out} = 2^N V_{in} - \frac{I_{out}}{f} \frac{(2^N + 2^{N-1} - 2)^2}{C_{tot}} \quad (4)$$

$$C_{tot} = \frac{I_{out}}{f} \frac{(9k^2/4) - (3k/2) - (1/4)}{(k+1)V_{in} - V_{out}} \quad (5)$$

Fig. 1 Topology

- a Fibonacci
- b Series-parallel
- c Voltage doubler
- d Dickson

Fibonacci converter: The Fibonacci topology [3] is shown in Fig. 1a. The VCR of this topology will not increase linearly with N either. The ideal VCR is determined by the $(N+2)$ -th number of Fibonacci. If the charge balance method is applied to the Fibonacci topology, the output voltage is calculated in (6). $Fib(m)$ represents the m th

Fibonacci number and f represents the switching frequency. Again the output voltage can be maximised by minimising the second term of (6). This term is smallest if each i th capacitor is given by (7). After substituting (7) into (6) and isolating C_{tot} , the total capacitance will be given by (8). The following substitution is performed in (8): $k = (fib(N+2) - 1)$. Equation (9) now defines the total capacitance in the function of k and again $k+1$ is the VCR of this topology.

$$V_{out} = fib(N+2)V_{in} - \frac{I_{out}}{f} \sum_{i=1}^N \frac{fib(i)^2}{C_{N+1-i}} \quad (6)$$

$$C_i = \frac{fib(N+1-i)}{\sum_{j=1}^N fib(j)} C_{tot} \quad (7)$$

$$C_{tot} = \frac{I_{out}}{f} \frac{(fib(N+2) - 1)^2}{fib(N+2)V_{in} - V_{out}} \quad (8)$$

$$C_{tot} = \frac{I_{out}}{f} \frac{k^2}{(k+1)V_{in} - V_{out}} \quad (9)$$

Series-parallel converter: When a series-parallel converter [1] is implemented the output voltage increases linearly with the number of stages. Thus the VCR of this N -stage series-parallel converter is $N+1 = k+1$. In Fig. 1b a series-parallel converter is shown. Based on Kirchhoff laws and charge balance techniques, we can derive the output voltage (10) and the charge Q on a single capacitor (11). Substitution of (10) into (11) gives us the total required capacitance (12).

$$V_{out} = V_{in} + \frac{NQ}{C} \quad (10)$$

$$Q = CV_{in} - \frac{I_{out}}{f} \quad \text{and} \quad Q_{tot} = NQ \quad (11)$$

$$C_{tot} = NC = \frac{I_{out}}{f} \frac{N^2}{(N+1)V_{in} - V_{out}} \quad (12)$$

Dickson-converter: Finally the Dickson topology [4] is analysed. Similar to the series-parallel converter, the VCR of this N -stage Dickson converter is $N+1 = k+1$. In Fig. 1d a Dickson-converter is shown. The output voltage of a Dickson converter is defined in [4] and shown in (13). Therefore the total required capacitance to achieve a certain output voltage V_{out} and output current I_{out} at a switching frequency f is calculated in (14).

$$V_{out} = V_{in} + N \left(V_{in} - \frac{I_{out}}{fC} \right) \quad (13)$$

$$C_{tot} = NC = \frac{I_{out}}{f} \frac{N^2}{(N+1)V_{in} - V_{out}} \quad (14)$$

Topology comparison: In fact (9), (12) and (14) are identical. If C_{tot} is differentiated towards k and set equal to zero, the minimum k is found in (15). With the help of substitution formulas the number of stages for each converter can be calculated. If this k_{min} is substituted in C_{tot} , (16) gives the minimum total capacitance of these topologies. Thus the minimum total capacitance will be the same for these three topologies. However the number of stages will be different. The total capacitance of the voltage doubler topology is given in (5). If (5) is differentiated towards k , the minimum k is found (17). If this k_{min} is substituted in (4) we get the minimum total capacitance (18).

Equations (16) and (18) show that if the VCR is higher than 8/5, the voltage doubler topology needs more capacitance than the other topologies. In the observed topologies the VCR is at least two, thus by definition the voltage doubler topology is inferior if optimised towards area.

In Fig. 2 an overview is given of the analysed topologies and the total required capacitance as a function of the number of stages for a typical application. The series-parallel and the Dickson-converter have a coinciding cost function and a minimum at ten stages. The output voltage of the Fibonacci-converter increases super linear according to the numbers of Fibonacci and needs only five stages. However, as has been proven in the analysis above, the total capacitance remains the same. Thus they perform equally well. It is also shown in Fig. 2 that indeed the voltage-doubler topology has the highest total capacitance

and is outperformed by the other topologies.

$$k_{\min, \text{Dick-Fib-SePa}} = 2 \left(\frac{V_{\text{out}}}{V_{\text{in}}} - 1 \right) \quad (15)$$

$$C_{\text{tot}, \min, \text{Dick-Fib-SePa}} = 4 \frac{I_{\text{out}}}{f} \frac{V_{\text{out}} - V_{\text{in}}}{V_{\text{in}}^2} \quad (16)$$

$$k_{\min, \text{VoDo}} = 2 \frac{V_{\text{out}}}{V_{\text{in}}} - \frac{7}{3} \quad (17)$$

$$C_{\text{tot}, \min, \text{VoDo}} = 3 \frac{I_{\text{out}}}{f} \frac{3V_{\text{out}} - 4V_{\text{in}}}{V_{\text{in}}^2} \quad (18)$$

Fig. 2 Minimum total capacitance in function of number of stages for voltage doubler, Dickson, series-parallel and Fibonacci-converter topologies

Conclusion: This analysis determines a mathematical approach for an area driven design of a capacitive DC/DC converter. It is proven that

the Dickson, series-parallel and Fibonacci topologies are equivalent from an area-cost point of view, in contrary to the voltage doubler topology which is clearly inferior from this point of view.

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