Design, construction and control of a quasi-resonant SMPS working at 2 MHz.

S. Uytterhoeven, P. Jacqmaer, and J. Driesen, *Member, IEEE*

Abstract— Switching Mode Power Supplies with higher switching frequencies are, in general, smaller in size for the same power rating. Resonant converters have an advantage over PWM-type converters because they use soft switching, reducing losses and increasing the energy efficiency of the power electronic circuit. In this paper, a converter is designed having a switching frequency more than 2 MHz. The power is regulated and varies between 15 and 50 W, at a constant output voltage of 15 V. An LLC-type topology is chosen as resonant tank, in which the parasitic transformer leakage inductance is efficiently employed. An experimental converter was built, handling 50 W at 1.4 MHz. The efficiency is up to 60 % at full load..

I. INTRODUCTION

Resonant converters inhabit many advantages over traditional hard-switched converters. Higher efficiency combined with smaller passive components can be achieved [1][2]. Resonant converters employ soft switching techniques to minimize switching losses and improve EMI-generation by using sine-shaped waveforms [3]. PWM-type converters use rectangular-shaped waveforms which can be seen as sums of higher order harmonics, according to Fourier's theorem. These higher order harmonics contribute to magnetic losses and create ringing and peak voltages in combination with parasitic components in the circuit. Resonant converters are inherently better armed against these parasitic effects due to the presence of sinusoidal waveforms. Sometimes, even parasitic components can usefully be employed in the circuit, as is the case in this work. That way, EMI-generation can be reduced [4][5].

Soft switching can be achieved by realizing zero-voltage or zero-current switching (ZVS or ZCS). Zero-voltage switching signifies that, during the switching operation,

there is no voltage across the switch [3]. Theoretically, there will be no switching losses, as the product of voltage over and current through the switch remains zero. With MOSFETs, it is of great importance to use Zero-Voltage Switching (ZVS) to avoid the capacitive discharge losses of the MOSFET output capacitance C_{OSS} [6][1]. In this work a half-bridge topology is chosen because the power of the converter is not big enough so that the use of a full bridge is justified. This is represented in figure 1.

Fig. 1. Half bridge LLC topology

The converter must be able to generate a DC power between 15 W and 50 W at the output. The output voltage is 15 V DC, with a voltage ripple not exceeding 30 mVpp and 100 mVpp at low and high powers respectively. Input voltage is 325 V with 10 % variation. This corresponds to a rectified grid voltage and allowed variation on Belgian distribution grids. The switching frequency is minimum 2 MHz. This combination of power level and switching frequency is chosen because it is difficult to realize such a circuit using conventional, hard-switched techniques and implies the use of soft-switching.

A gate driver, employing a 50% duty-cycle, is being used to drive the gates of both MOSFETs. Frequency can be changed in order to adjust the power transfer. A pulse transformer is used in the gate driver to generate two complementary gate signals. The half-bridge topology is connected to a transformer, incorporated in the resonant tank, to scale down the high input voltage. A rectifier circuit with 2 Schottky-diodes is used at the output. The output filter ensures the ripple-specification on the output voltage.

Manuscript received July 15, 2008.

Stijn Uytterhoeven graduated at Katholieke Universiteit Leuven as civil electromechanical engineer, option electrical energy, in 2008. He is now employed at Laborelec, Rodestraat 125, 1630 Linkebeek, Belgium. (stijn.uytterhoeven@laborelec.com)

Pieter Jacqmaer is a doctoral research assistant at Katholieke Universiteit Leuven, faculty of engineering, department of electrical engineering (ESAT), Kasteelpark Arenberg 10, 3001 Heverlee, Belgium (phone: +32 16 32.1023, Pieter.Jacqmaer@esat.kuleuven.be)

Johan Driesen is a full time professor at Katholieke Universiteit Leuven, faculty of engineering, department of electrical engineering (ESAT), Kasteelpark Arenberg 10, 3001 Heverlee, Belgium (phone: +32 16 32.1024, Johan.Driesen@esat.kuleuven.be)

II. LLC-RESONANT TANK VS. LLCC-RESONANT TANK

The basic two-element type resonant tanks, series and parallel loaded, each have some advantages and disadvantages. Series resonant converters have a stable behaviour at a short-circuited output terminal [1][7]. They are more efficient when compared to parallel converters because the circulating current in the resonant tank varies with the output load. Unfortunately, they exhibit a broad regulating area in terms of frequency, which limits the possible load variation. Furthermore, they are not able to handle a no-load situation at the output terminal. [4][1]. Parallel converters, on the contrary, can handle no-load situations and suffer less from influence of parasitic effects due to the output capacitance, C_{oss} , of the MOSFET's [8]. They have a smaller regulating area in terms of frequency, but are less efficient because of a circulating current in the resonant tank, being almost independent from the load. Besides that, they cannot handle short-circuiting at the output terminals.

Multi-resonant tanks combine the advantages of both of these low order resonant tanks, by employing more elements in the resonant tank [9]. The LLC-type converter appeared to have the best behaviour and is being designed in this project. It is possible to employ the parasitic inductance of the transformer efficiently in the resonant tank. This can be seen by inserting the equivalent transformer scheme in the converter topology. The two inductances of the resonant tank can be formed by the leakage inductance L_{sprim} and the magnetizing inductance L_m of the transformer [6][10]. An external resonant capacitor C_s is added to the circuit to form the LLC resonant tank. This can be seen in figure 1.

When considering transformers, one has to keep in mind that there exist capacitive effects due to the construction of the windings of the transformer. When this capacitive nature becomes dominant, the LLC-topology more resembles a LLCC-topology. It is of great importance to keep the influence of the parasitic capacitance, appearing in parallel of L_m , small. This can be done by choosing C_s big compared to C_p . Not doing so can result in loss of ZVS at heavy load [11][15].

A mathematical model of the whole converter was constructed, by calculating an equivalent loading resistor, which inhabits the effects of the rectifier circuit. It was proved that the difference between this mathematical model and simulations incorporating the rectifier, is negligible [12][2][13]. This allowed to do calculations much faster and facilitated the use of extensive iterations upon finding the most optimal configuration.

III. SELECTING THE CORRECT TRANSFORMER CORE

	EFD25	RM8/i	E32
P_{core} [W]	2.5	2.5	2.5
P_v [kW/m ³]	757.6	1025	505.1
B_{peak} [mT]	16.2	18.4	13.7
N_1	26	21	14
L_1 [μH]	108.16	44.1	31.4
C_r at $f_0=1$ MHz [nF]	0.234	0.574	0.807
A_L [nH/turns ²]	A160	A100	E160

TABLE I
DIFFERENT CORE TYPES AT WORST-CASE SCENARIO

A number of different materials for the magnetic core were considered. 3F4-ferrite material, produced by Ferroxcube, appeared to be a good choice in achieving the lowest core-losses [10]. Furthermore, a whole range of core-types where subjected to 3 types of scenarios. The worst-case scenario allowed a core loss of 2.5 W (95 % efficiency). Three different core-types remained as possible candidates for the magnetic core (table 1). In the full paper, an extensive explanation of the selection procedure will be given.

The last type of core in this table is a core that only can be used in planar transformers. These are not considered here. The choice is RM8/i. To limit the core-losses, one has to increase the number of primary windings, as:

$$N_1 = \frac{\psi_{pp}}{\phi_{pp}} \quad (1)$$

$$\phi_{pp} = A_e \cdot B_{pp} \quad (2)$$

$$P_{core} = Cte \cdot f^x \cdot B_p^y \quad (3)$$

The core-losses diminish when the peak-to-peak magnetic induction decreases, which can be achieved with lower peak-to-peak magnetic flux in the core. This means that lower core-losses correspond to a higher number of primary windings, because the magnetic-flux-coupling (better known as Volt-second-product) remains the same.

IV. DESIGN OF THE RESONANT CONVERTER

When considering the gain characteristic of this type of circuit, one can recognize two resonance frequencies. These can be used in the design of the resonant tank, which can be seen in figure 3.

Fig. 3. Gain vs. frequency characteristics of the LLC-tank

The benefit of this choice is the possibility to use step-up mode in the transformer [14][7]. Also the frequency variation can be smaller for the same load variation, and the load-independent point can be used in the regulating area. Step-up mode is useful in this work, because less transformer losses can be obtained, by selecting a higher transformer ratio. It must be noticed that the gain is higher than one in step-up mode which allows for higher transformer ratio for the same input to output ratio. This means choosing a higher number of primary windings for the same number of secondary windings. A transformer ratio of 17 was needed to limit the core losses in this work, and at the same time it was possible to work in the beneficial area between the two resonant frequencies. Another option is to work in the series region, which is located above the highest resonance frequency. Although ZVS can be achieved in this region, several disadvantages appear in this working mode and it is therefore not selected. The position of these resonance frequencies can be influenced by choosing the size of the resonant tank components. According to:

$$f_{r1} = \frac{1}{2\pi\sqrt{C_s L_s}} \quad (4)$$

$$f_{r2} = \frac{1}{2\pi\sqrt{(C_s + C_p) L_s}} \quad (5)$$

it is possible to understand that the leakage-inductance L_s needs to be of a minimal magnitude. Therefore the ratio $m = L_m/L_s$ is chosen between 3 and 8 [14]. Through iterative

MATLAB-simulations applied to the mathematical model of the LLC-circuit, it was seen that a resonant tank consisting of following components would be optimal:

$$L_s = 4\mu H$$

$$L_M = 27\mu H$$

$$C_R = 0.38nF$$

The realized transformer has a RM8/1 – A100 type core, made out of 3F4 material. The measured equivalent circuit is presented in figure 4. Due to the construction of the transformer primary winding, a relative large parasitic capacitance appears at the primary side. PSPICE-simulations showed that the influence of this capacitance is not negligible. In fact, ZVS would not have been attainable at heavy loading. Therefore a bigger series capacitance was chosen, with the accompanying disadvantage of lower switching frequency.

Fig. 4. Measured equivalent scheme of the transformer

A gate driver was designed to generate two complementary signals, each with a 50% duty-cycle, and variable in frequency. Therefore, a voltage controlled oscillator (VCO) is used in combination with a TC4428 driver to generate a rectangular shaped waveform, varying between -10 V and +10 V. To make a complementary signal a pulse transformer was developed. Since the upper MOSFET in the half-bridge topology has a floating source, a gate driver transformer is an obvious choice for these high switching frequencies [20]. The topology is presented in figure 5. The gate driver transformer is realized using an EFD10-3F4-S core, and has 10 turns in each winding.

Fig. 5. Gate driver topology

V. EXPERIMENTAL RESULTS

The realized gate driver was tested in no-load condition and performs well up to 6 MHz. At full load, the gate driver circuit behaves poorly, because of insufficient magnetizing inductance in the gate driver transformer. This results in a significant voltage droop, leading to poor behaviour of the gate driver. This could be solved by choosing a larger transformer core, and applying more turns. Next to that, a shoot-through problem arises because of a duty-cycle being not exactly equal to 50 % and because of a phase shift between the two gate signals. Both of these effects increase the losses in the converter and need to be solved by employing a better gate driver circuit. The difference in behaviour between a loaded and an unloaded gate driver, can be seen in figure 6.

The experimental converter realizes an efficiency up to 60 % at 50 W, which can be attained at 1.4 MHz.

With the adapted configuration, ZVS can be achieved up to 2.25 MHz. The transformer behaves properly and is subject to acceptable heating.

Fig. 6. Gatedriver performance at 2.25 MHz (a) unloaded (b) 15 W

VI. CONCLUSIONS

A resonant converter was designed and built. Soft-switching was implemented in order to diminish switching losses and increase the efficiency. The experimental converter is based on an LLC-topology and has an efficiency up to 60 % at full load. ZVS is reached up to 2.4 MHz. The optimal configuration of the resonant tank is found using a mathematical model and iterative analyses in MATLAB. These analyses will be outlined in the full paper. It was chosen to operate the converter between the two main resonance frequencies, because that working area exhibits many advantages. Lower magnetic core loss is attainable by selecting a higher transformer ratio and using step-up mode. Due to the presence of parasitic capacitances at the transformer primary side, the converter behaves as an LLC-type converter. Therefore, a higher series capacitance was selected to avoid the loss of ZVS.

REFERENCES

- [1] R. Steigerwald, "A comparison of half-bridge resonant converter topologies." IEEE Transactions on Power Electronics Vol. 3 No. 2, pp. 174-182, April 1988.
- [2] J. Lazar en R. Martinelli, "Steady-state analysis of the LLC series resonant converter." IEEE Applied Power Electronics Conference and Exposition, 2001. APEC 2001, Vol. 2, pp. 728-735, 2001.
- [3] B. Mammano, "Resonant mode converter topologies, topic 1." Unitrode Corporation, 2001.
- [4] P. Chetty, "Resonant power supplies: Their history and status." IEEE AES magazine, Vol. 7, Issue 4, pp. 23-29, april 1992.
- [5] H. Chung, S. Hui, en K. Tse, "Reduction of power converter EMI emission using the soft-switching technique." IEEE Transactions on Electromagnetic Compatibility, Vol. 40, No. 3, pp. 282-287, 1998.
- [6] J. Lazar en R. Martinelli, "Steady-state analysis of the LLC series resonant converter." IEEE Applied Power Electronics Conference and Exposition, 2001. APEC 2001, Vol. 2, pp. 728-735, 2001.
- [7] B. Yang en F. Lee, "Topology investigation of front end DC/DC converter for distributed power system." PhD. Dissertation, 2003.
- [8] J. Sabat_e, R. Farrington, M. Jovanovic, en F. Lee, "Effect of FET output capacitance on ZVS of resonant converters." IEEE Transactions on aerospace and electronic systems, Vol. 32, No.1, 1996.
- [9] M. Jovanovic, A. Wojcieh, en F. Lee, "High-frequency offline power conversion using zero-voltage-switching quasi-resonant and multiresonant techniques." IEEE Transactions on Power Electronics, Vol. 4 No. 4, pp. 459-469, 1989.
- [10] H. de Groot, E. Janssen, R. Pagano, en K. Schetters, "Design of a 1-MHz LLC resonant converter based on a DSP-driven SOI half-bridge power MOS module." IEEE Transactions on Power Electronics, Vol. 22, Issue 6,, pp. 2307-2320, 2007.
- [11] P. Nakhost en S. Munk-Nielsen, "50 W resonant SMPS with coreless transformer for AM radio application." Power Electronics Specialists Conference, 2006. PESC 2006. 37th IEEE, pp. 1-7, 2006.
- [12] D. G.D., P. Ranstad, en C. Sadarangari, "Three elements resonant converter: The LCC topology by using MATLAB." IEEE Power Electronics Specialists Conference, 2000. PESC 2000, Vol. 2, pp. 1077-1083, 2000.
- [13] Y. Ang, M. Foster, H. Sewell, C. Bingham, en D. Stone, "Stress analysis of fourth-order LLC resonant converters." IEEE Electronics Letters Vol. 38, No. 24, pp. 1585-1586, 2002.
- [14] "Half-bridge LLC resonant converter design using FSFR-series fairchild power switch." Fairchild Semiconductor Application Note AN4151, 2007.

- [15] C. Chakraborty, M. Ishida, en Y. Hori, "*Novel half-bridge resonant converter topology realized by adjusting transformer parameters.*" IEEE Transactions on industrial electronics, Vol. 49, No. 1, pp. 197-205, 2002.
- [16] M. Xinkui en C. Wei, "*More precise model for parasitic capacitances in high-frequency transformer.*" IEEE Power Electronics Specialists Conference, Vol. 2, pp. 1054 - 1057, 2002.
- [17] H. Lu en J. Zhu, "*Experimental determination of stray capacitances in high frequency transformers.*" IEEE Transactions on power electronics, Vol. 18, No.5, 2003.
- [18] O. Ojo, I. Bhat, en B. Tech, "*Steady-state and dynamic analyses of high-order parallel resonant converters.*" IEE Proceedings-B Vol.140 No. 3, pp. 209-216, 1993.
- [19] G. Hsieh, M. Lai, J. Wang, en M. Lia, "*Realization study of isolated half-bridge zero-voltage switched converter.*" IEEE International Conference on Industrial Electronics, Control and Instrumentation, Vol. 1, pp. 663-668, 1994.
- [20] L. Balogh, "*Design and application guide for high speed MOSFET gate drive circuits.*" Texas Instruments Application Note, 2002.