A Design Approach for Power-Optimized Fully Reconfigurable $\Delta\Sigma$ A/D Converter for 4G Radios

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Abstract—This paper presents a novel design approach for fully reconfigurable low-voltage delta-sigma analog-digital converters for next-generation wireless applications. This approach guides us to find the power-optimal solution corresponding to the specifications of various wireless standards by exploring single-loop feedback and feedforward topologies with different filter order, number of quantizer bits, and oversampling ratios. Unlike previous multimode designs, this approach provides a better power efficiency. Based on this approach, a system-level design of a digitally programmable delta-sigma modulator for 4G radios is presented.

Index Terms—4G radios, analog-digital converter (ADC), continuous time (CT), delta-sigma modulator (DSM), design approach, power optimization, reconfigurable.

I. INTRODUCTION

IN RECENT YEARS, there has been an explosive demand for wireless and portable applications, resulting in more flexible communication systems which can handle various standards in different environments. The 4G systems that are expected to appear in the market by the end of this decade aim to seamlessly integrate the existing and future wireless technologies on a single handset, with fast speed and more functions. A software defined radio (SDR) adopting a fully reconfigurable front-end is believed to be the right answer to realize such a system. Therefore, a fully reconfigurable analog-digital converter (ADC) is needed for the different modes in 4G radios. This switches its resolution and bandwidth depending on the communication mode. Delta-sigma modulators (DSMs) are normally favored in multimode designs due to their low power consumption and inherent tradeoff between speed and accuracy. In the last five years, several semi-flexible DSMs [1], [2] were presented, which can handle up to three fixed modes. A more flexible continuous-time (CT) DSM was presented in [3] which can be switched to 121 modes by using combinations of 11 resistor and 11 capacitor values. All the previous multimode design approaches employ a fixed topology with a reconfigurable passive components array in order to adapt to different wireless modes. This paper presents a more flexible design with a reconfigurable structure to save power.

The paper is organized as follows. First, the specifications of the major standards in 4G radios are given. Then, power-optimal topologies for different specifications are found by ex-

TABLE I
SPECIFICATION FOR MAJOR STANDARDS IN 4G RADIOS

Standards	Signal BW (MHz)	Modulation	Dynamic Range (dB)
GSM	0.2	GMSK	85
UMTS TDD	2	BPSK	74
		64QAM	74
UMTS FDD	4	BPSK	72
		64QAM	72
DVB-H	7.6	BPSK	54
		64QAM	63.5
WLAN 802.11 a	20	BPSK	42
		64QAM	55
WLAN 802.11 n	40	BPSK	42
		64QAM	55

ploring both single-loop feedback (FB) and feedforward (FF) topologies with different filter orders and quantizer bits, for a large range of oversampling ratios (OSRs). In Section IV, a system-level reconfigurable design for 4G radios is presented based on the results from the previous sections. Section V concludes this paper.

II. SPECIFICATIONS FOR ADCS IN 4G RADIOS

The input signals of the ADCs in 4G radios cover a wide range of standards ranging from the newest wireless local area network (WLAN) 802.11n to the widely used GSM mode. Table I summarizes the main foreseen specifications in 4G radios. In order to meet all the specifications, a flexible base-band ADC needs to cover a wide range of signal bandwidths from a few hundreds of kilohertz up to 40 MHz, and dynamic range (DR) performance also needs to be scaled from 85 dB for GSM down to 55 dB for WLAN.

III. TOPOLOGY EXPLORATION BASED ON POWER CONSIDERATIONS

Like most of the previous multimode designs [1]–[3], the single-loop DSM topology becomes our choice because of its robustness to nonidealities of circuit components. Furthermore the relatively simple structure makes it more suitable for the complex reconfigurable circuit design.

The ideal performance of the single-loop DSM is determined by the number of quantizer bits, the modulator order, and the OSR. Different combinations of these parameters can be used to achieve the same DR. Each combination forms a design solution. However, which combinations give the best power efficiency for various modes has not been thoroughly discussed in the past. Thus, a power optimization process was carried out, in the following subsections.

A. Power Considerations on System Level

Stability is one of the key factors which influence the actual performance of a DSM. For the single-bit quantizer case, the infinity norm $\|H\|_\infty$ is traditionally chosen to be 1.5 as rule of

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Fig. 1. SNR and OL versus the $\|H\|_\infty$ of the NTF for third-order 2-bit DSM case.

TABLE II

OPTIMAL INFINITY NORM OF THE NTF FOR DSM FROM SECOND- TO FIFTH-ORDER WITH NUMBER OF QUANTIZER BITS FROM 1 TO 5

	1 bit	2 bits	3 bits	4 bits	5 bits
Order 2	2	2.5	3	3.5	3.5
Order 3	1.5	2	3	3.5	4
Order 4	1.5	2	2.5	3.5	4
Order 5	1.5	2	2.5	4	5

TABLE III

OL LEVEL FOR DSM FROM SECOND- TO FIFTH-ORDER WITH NUMBER OF QUANTIZER BITS FROM 1 TO 5 CORRESPONDING TO $\|X\|_\infty$ VALUES IN TABLE II

	1 bit	2 bits	3 bits	4 bits	5 bits
Order 2	-1 dB	-1 dB	-1 dB	-1 dB	-1 dB
Order 3	-2 dB	-2 dB	-2 dB	-1 dB	-1 dB
Order 4	-4 dB	-3 dB	-3 dB	-2 dB	-1 dB
Order 5	-5 dB	-5 dB	-3 dB	-2 dB	-1 dB

thumb to ensure stability [5]. In the case of a multibit quantizer, $\|H\|_\infty$ can be increased to improve the signal-to-quantization noise ratio (SQNR). However, this can not be pushed too far, because the overload level (OL) then starts to decrease. The maximum input voltage swing is the product of the OL and V_{ref} (reference voltage), where V_{ref} is limited by the supply voltage and the specific circuit implementation. Therefore, the optimal $\|H\|_\infty$ should be chosen to maximize the SQNR and meanwhile, to minimize the decrease of the OL. As example, Fig. 1 shows the SNR performance of a third-order modulator with a 2-bit quantizer (OSR = 128). The optimal $\|H\|_\infty$ is around 2 here since the SQNR increases very slowly when $\|H\|_\infty$ is larger than 2. Further increase of the $\|H\|_\infty$ leads to the rapid decrease of the signal power, which in turn increases the power consumption budget used to reduce the thermal noise for the same DR. Similarly, balancing between OL and SNR, the optimal $\|H\|_\infty$ for different filter orders and quantizer bits has been decided as listed in Table II. With these values, the optimal noise transfer function (NTF) can be determined using the *synthesizeNTF* function in [4], and, the corresponding OL values are listed in Table III. It is notable that the OL also depends on the input test frequency, so only worst case OL values (when a near-dc test tone is applied [5]) are taken into account here. Finally, long-term transient simulations are used to verify the stability.

Except for the OL level, the integrator gain coefficient is another factor which influences the power consumption. Normally, the coefficient values are directly related to the filter structure. For single-loop DSMs, there are mainly two types: the FB and the FF topologies (shown in Fig. 2). Both these types can be used to implement the same NTF. The major difference between the

Fig. 2. Topology with (a) compensation and (b) FF compensation.

TABLE IV

COEFFICIENTS OF THE FIRST INTEGRATOR FOR SECOND- TO FIFTH-ORDER FB AND FF DSMs WITH QUANTIZER BITS FROM 1 TO 5

FB	1 bit	2 bits	3 bits	4 bits	5 bits
Order 2	0.3	0.45	0.55	0.65	0.65
Order 3	0.15	0.3	0.35	0.43	0.46
Order 4	0.1	0.15	0.2	0.25	0.28
Order 5	0.07	0.1	0.15	0.2	0.2
FF	1 bit	2 bits	3 bits	4 bits	5 bits
Order 2	0.3	0.5	0.9	1.6	2.5
Order 3	0.3	0.5	0.9	1.6	2.5
Order 4	0.3	0.5	0.9	1.6	2.5
Order 5	0.3	0.5	0.9	1.6	2.5

FF and FB topologies is the output voltage swings of the integrators, especially the first integrator. Due to the FF paths, the output swing of the first integrator of the FF topology is much smaller than that of the FB topology when the same integrator coefficients are used. In other words, a much larger coefficient can be used for the first integrator to achieve the same output swing in the FF topology. On the other hand, a fast amplifier is usually needed for the summing stage before the quantizer of the FF topology. Luckily, this power-hungry amplifier can be omitted by using capacitor FF summation at the last integrator [6]. To allow a fair comparison, the same initial NTFs derived from Table II are used here to implement both CT FF and FB topologies. The swings of the first integrators are scaled for linearity reasons. The final coefficients of the first integrator for FB and FF topologies with different modulator order and quantizer bits are listed in Table IV. It can be seen from the tables that the coefficient for the FB case is scaled down as the modulator order increases to guarantee stability and a reasonable output swing. For the FF case, the coefficient of the first integrator is mainly determined by the number of quantizer bits, since the quantization noise dominates the output in this case. Due to the coefficient difference, the FF topology shows better power and area efficiency, as will be analyzed in detail in the following sections.

B. Power Considerations on Circuit Level

In this subsection, the performance and power tradeoff at circuit level are discussed in detail for low supply voltages. There are mainly three parts in a DSM: the loop filter which is composed of integrators, the quantizer and the DAC in the path.

1) *Integrator*: For supply voltages smaller than $1V_t$, the room left for the input range is seriously limited, when the G_m -C integrator is used, which directly degrades the DR. In an RC integrator, the input of the amplifier is fixed to virtual ground, and the input signal only faces a resistor. Hence, a larger input range can be used. Besides, the G_m -C integrator is not suitable for very high linearity specifications and we want to reuse the integrator for accuracies ranging from 9 to 14 bits, according to Table I. Therefore, the RC integrator becomes a better choice for our reconfigurable low-voltage application.

Fig. 3. OTA-RC integrator with current-steering DAC and Miller OTA.

The DR calculation takes into accounts both quantization noise and thermal noise

$$\text{DR} \approx \frac{1}{2} \frac{V_{\text{in,range}}^2}{N_q + N_{\text{th}}} = \frac{1}{2} \frac{(\text{OL} \cdot V_{\text{ref}})^2}{N_q + N_{\text{th}}} \quad (1)$$

$$N_{\text{th}} = 2 \cdot (4kTR_{\text{in}} + N_{\text{th,DAC}}) \cdot \text{BW} \quad (2)$$

$$N_{\text{th,DAC}} = \frac{32}{3} kT \frac{I_{\text{DAC}}}{V_{\text{gst,DAC}}} R_{\text{in}}^2 \text{BW} \quad (3)$$

with N_q the quantization noise; N_{th} the input equivalent thermal noise; R_{in} the resistance of the RC integrator (shown in Fig. 3); k Boltzmann's constant; T the temperature; $N_{\text{th,DAC}}$ the thermal noise from the DAC (current-steering DAC is used for high speed); BW the signal bandwidth; gm_{DAC} the sum of the transconductance of the transistor $M_1 - M_N$ of the DAC (shown in Fig. 3). The thermal noise of the amplifier itself is neglected here, due to little contribution to the overall thermal noise. As V_{ref} is the product of I_{DAC} and R_{in} , (3) can be written as

$$N_{\text{th}} = 2 \cdot \left(4kT + \frac{16}{3} kT \frac{V_{\text{ref}}}{V_{\text{gst,DAC}}} \right) R_{\text{in}} \text{BW} \quad (4)$$

with $V_{\text{gst,DAC}}$ the overdrive voltage of the transistor $M_1 - M_N$ of the DAC. In a low-voltage design, thermal noise dominates the noise budget, so the R_{in} can be found from (1) and (4) as

$$R_{\text{in}} \approx \frac{3}{16} \frac{(\text{OL} \cdot V_{\text{ref}})^2 V_{\text{gst,DAC}}}{kT \cdot \text{DR} \cdot \text{BW} (3V_{\text{gst,DAC}} + 4V_{\text{ref}})}. \quad (5)$$

The corresponding integration capacitance C_{int} is given by

$$C_{\text{int}} = \frac{8kT}{3} \frac{\text{DR} (3V_{\text{gst,DAC}} + 4V_{\text{ref}})}{V_{\text{gst,DAC}} (\text{OL} \cdot V_{\text{ref}})^2 \cdot a \cdot \text{OSR}} \quad (6)$$

with a the scaling coefficient defined in Table IV. As indicated in (6), C_{int} increases as a scales down, which makes the FF topology more area efficient than the FB type for the same DR. On the other hand, C_{int} is the major contributor to the load capacitance of the amplifier

$$C_{\text{load}} = \alpha C_{\text{int}} + C_{\text{mos}} + C_{\text{wire}} \quad (7)$$

with C_{mos} and C_{wire} the parasitic capacitance from the MOS transistors and connection wires, respectively. α is usually in the order of 10% when metal-oxide-metal capacitors are used.

For low supply voltage, the two-stage amplifier is preferred for larger output swing. The standard Miller operational transconductance amplifier (OTA) shown in Fig. 3 is used here

to estimate the power consumption. The power consumption of the integrator can be found to be

$$P_{\text{int}} = 2(I_{\text{in}} + I_{\text{out}})V_{\text{DD}} \quad (8)$$

with I_{in} and I_{out} the bias quiescent currents of the input and output branch, respectively. Normally the I_{in} value is a small fraction of I_{out} . The I_{out} in the output branch should be selected to meet both the stability and slew rate requirements

$$\frac{2I_{\text{out}}}{V_{\text{gst,out}} 2\pi C_{\text{load}}} = \frac{gm_{\text{out}}}{2\pi C_{\text{load}}} \geq 2 \cdot \text{GBW} \geq c \cdot Fs \quad (9)$$

$$I_{\text{out}} \geq 2I_{\text{DAC}} \quad (10)$$

with gm_{out} the transconductance of M_{out} in Fig. 3. c is normally less than 2 in the CT DSM case. Equation (9) guarantees the stability of the two-stage operational transconductance amplifier (OTA) and a stable DSM. The GBW represents the open-loop gain bandwidth of the OTA. Besides, the OTA in the integrator needs to sink both the input current and DAC current, thus the I_{out} needs to be at least twice the I_{DAC} as shown in (10) to provide enough slew rate. By putting (6), (7) into (9) and (10), we have

$$I_{\text{out}} \geq 2\pi cFs \left(\frac{8}{3} kT \frac{\alpha \text{DR} (3V_{\text{gst,DAC}} + 4V_{\text{ref}})}{a \cdot (\text{OL} \cdot V_{\text{ref}})^2 \cdot V_{\text{gst,DAC}} \text{OSR}} + C_{\text{mos}} + C_{\text{wire}} \right) V_{\text{gst,out}} \quad (11)$$

$$I_{\text{out}} \geq \frac{32}{3} kT \frac{(3V_{\text{gst,DAC}} + 4V_{\text{ref}}) \text{DR}}{\text{OL}^2 \cdot V_{\text{ref}} \cdot V_{\text{gst,DAC}}} \text{BW}. \quad (12)$$

As discussed in the previous subsection, the optimal OL and a can be determined once the corresponding system-level filter topology is fixed. To minimize the power consumption, parameters V_{ref} , $V_{\text{gst,DAC}}$ can be increased while the $V_{\text{gst,out}}$ should be minimized. The final I_{out} depends on the larger value from (11) and (12). By using Table II–IV, and (11)–(12), the power consumption of the first integrator for both FB and FF DSMs with different filter order and number of quantizer bits can be estimated for a given DR. To make better estimation, at least 6-dB margin of the DR should be taken into account.

Compared to the first one, the other integrators can be scaled to save power since both their noise and nonlinearity are suppressed by the gain of the first stage. Unlike in discrete-time (DT) DSMs, large capacitor arrays are used not only to reconfigure between different modes but also to compensate the process variations in CT DSMs. In order not to be influenced by parasitic capacitance, the minimum capacitor in the array is lower bounded which is one of the fundamental limitations in the reconfigurable design.

2) *DAC*: The first DAC's power is given by $V_{\text{DD}} I_{\text{DAC}}$ with I_{DAC} determined by (5). In the FB topology, power of the other DACs can be scaled in the same way as the integrators.

3) *Quantizer*: Its power consumption is estimated by using a power estimator proposed in [8]

$$P_Q = (2^b - 1) \frac{0.5V_{\text{DD}} - 0.3V_{\text{sw}}}{32.1 \times 10^3} V_{\text{DD}} L_{\text{min}} Fs + P_X \quad (13)$$

where b is the quantizer resolution, V_{swing} is the input signal swing, L_{min} is the gate length for the used technology, P_X is the

Fig. 4. Power estimation results for both FB and FF topologies. (a) GSM mode BW = 0.2 MHz DR = 85 dB. (b) UMTS mode BW = 2 MHz DR = 74 dB. (c) WLAN mode BW = 20 MHz DR = 55 dB.

encoder power (which not taken into account here). So, to save power, V_{swing} should be maximized for a given supply voltage and V_{ref} .

C. Power Estimation

The total power of a DSM can be estimated as the sum of the three parts: integrator, DAC and quantizer. By optimizing the power consumption both at system and circuit level, the optimal power consumption can be found for a certain design solution.

For a 90-nm CMOS technology with 1-V V_{DD} , the estimated power consumptions for both the FB and FF topologies with second- to fifth-order loop filter and number of quantizer bits from 1 to 5 are shown in Fig. 4. The results show that, in GSM mode, second- and third-order DSMs consume less power both in FB and FF topologies. This is because the total power budget is dominated by the integrator part in the GSM mode. In this case, the total power is mainly determined by (11) and (12), so DSMs with higher OL value have better power efficiency. When increasing the number of quantizer bits, the power consumption of the higher order DSMs goes down due to the increased OL level. It should be mentioned that the power estimations here do not take into account the power used in the linearity enhancement when multibit is used. When switching gradually from the GSM to the WLAN mode, the power of the second-order DSMs increases faster compared to the other orders. The reason is the rapid increase of the quantizer power for increasing signal bandwidth, while the integrator power increases at a slower rate due to the lowered DR specification. Since the lower order DSMs need a higher sampling speed to achieve the same DR, the lower order DSMs become less power-efficient in the WLAN mode.

Fig. 5. Power estimation for WLAN with reconfigurability consideration.

For linearity reasons, the switches of the capacitors should be connected to the virtual ground side and the output node of the OTA is directly connected to the capacitor array. Therefore, the load capacitance should take into account the total parasitic capacitance of the capacitor arrays. From (6), the largest capacitor in a reconfigurable DSM is determined by the specification with the lowest sampling frequency and the highest DR. Thus, the GSM mode determines the area budget and the major parasitic capacitance. When taking into account the large capacitor for the GSM mode, the plots for the WLAN case are different as they are influenced dramatically by the new consideration due to the increased load capacitance. The major change in Fig. 5 is that the power-optimal points shift from the single-bit to two-bit solutions, due to the reduced OTA GBW. However, further increasing the number of quantizer bits cannot save more power, as the quantizer power goes up quickly when the number of quantizer bits is larger than 3. Therefore, it is advisable to choose a third- to fifth-order DSM with 2–3 bit quantizer for WLAN.

A similar conclusion can be drawn for the results of the DVB-H and UMTS mode. For the GSM mode, the extra consideration does not influence the result. The second- to third-order DSMs with 1- to 3-bit quantizer consume less power.

IV. PROPOSED RECONFIGURABLE DSM

Inspired by the above observations, we found that a power- and area-optimal reconfigurable DSM for 4G radios can be realized by reconfiguring its filter order and even the number of quantizer bits. It seems that both FB and FF topologies can be used to achieve this goal. However, for comparable power consumption, a FB topology needs a larger signal swing which decreases the linearity. Furthermore, as indicated in (6), the corresponding capacitor would be much larger compared to the FF topology and this directly increases the power consumption for the WLAN case, as shown in Fig. 5. All these considerations result in the power-optimal fully reconfigurable DSM shown in Fig. 6. The extra DAC2 is added to compensate the quantizer delay [11]. To ease the design of the high-GBW OTA in the WLAN mode, the flexible DSM uses all four integrators and two local paths to create two resonators for further suppressing the quantization noise [5]. The 2-bit quantizer is used in this mode for better power efficiency according to Fig. 5. Besides, if 1-bit would be used in the WLAN mode, sampling frequency would have to be higher than 1 GHz to achieve the same performance, which is unpractical for the OTA design. For the DVB-H and UMTS mode, the fourth-order loop filter and 2-bit quantizer are still used, but only one resonator is used to save the large resistor in the local path, while still providing enough suppression on the quantization noise (see Fig. 6). In GSM mode, both g_1 and g_2 are set to zero for the same reasons. Besides, the fourth integrator is powered off and the coefficients are adapted

Fig. 6. Reconfigurable DSM topology for different modes.

Fig. 7. Flexible OTA array.

TABLE V
SIMULATED PERFORMANCE FOR DIFFERENT STANDARDS

	BW (MHz)	OSR	SNR (dB)	Jitter tolerance	Estimated Power*
WLAN	20	16	59	10 ps	8 mw
DVB-H	3.8	24	68.5	12 ps	3.5 mw
UMTS	2	32	77	9 ps	3 mw
GSM	0.2	128	84.5	5 ps	2 mw

* CMFB power is included.

correspondingly. Thanks to the FF topology, no extra bypass circuits are needed. In the quantizer, only one comparator is used as a single-bit quantizer to provide high linearity and to reduce the largest integration capacitor. The binary scaled resistor arrays and capacitor arrays are used to reconfigure the gain of each integrator according to the specifications of different standards. The g_1 and g_2 are tuned by the binary scaled resistor array in the local paths and can be set to zero by switching off the whole resistor array. The FF coefficients b_i stays the same in the WLAN/UMTS/DVB-H modes, but needs to be reconfigured for the GSM mode. DAC2 is also made tunable to compensate a wide range of quantizer delay.

The optimal power efficiency can only be achieved by using a flexible OTA which can adapt its GBW to different specifications. To allow fully digital control, the concept of switchable opamp (SOA) [10] is used here to implement the OTA in the RC integrator. Each SOA can be powered on or off by switching the voltage at the gate of all the transistors in the two-stage Miller OTA simultaneously. By reusing a basic robust unit, the design complexity is reduced and fully digital control is available. By connecting the SOAs in a binary scale as shown in Fig. 7, a fully reconfigurable OTA is obtained.

To verify the presented system solution, the finite gain and GBW of the OTA, parasitic capacitance, loop delay, clock jitter, etc., have been taken into account. The simulated performances using Matlab are summarized in Table V. Compared to the multimode designs in [2], [3], [9], the results listed in Table V show better power efficiency especially in WLAN mode, which verifies the effectiveness of the design approach described above.

TABLE VI
REPORTED STATE OF ART OF DSMs' PERFORMANCE

	BW (MHz)	OSR	SNR (dB)	Reported Power	CMOS Technology
WLAN	20	16	76	20 mW [11]	0.13 μ m
DVB	4	25	73	19 mW [12]	0.18 μ m
UMTS	1.92	12	65	3.5 mW [9]	0.13 μ m
GSM	0.2	65	82	1.44 mW [3]	90 nm

The state of the art of reported DSMs' performance (including single-mode DSMs reported in literature) for different modes is also listed in Table VI for comparison.

V. CONCLUSION

A digitally controllable, fully reconfigurable CT delta-sigma modulator is presented at the system level for low-voltage 4G applications. Both the FF and FB topologies have been explored towards low power with different combinations of design parameters in the design space for different specifications leveraging reconfigurability. The simulation results have confirmed that both power and area are saved compared to traditional fixed-topology, multimode designs by reconfiguring the filter order and number of quantizer bits at topology level and the OTA transconductance at the circuit level.

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