17.3 A 1.75GHz GSM/EDGE Polar Modulated CMOS RF Power Amplifier

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Up till now, most wireless modulation schemes, such as GSM and Bluetooth, only apply phase modulation to the RF carrier. To increase the data rate, recent modulation schemes, including EDGE and WLAN, also use amplitude or envelope variations of the phase modulated RF carrier. These envelope variations require either a linear or a linearized power amplifier (PA). A linear PA, such as a class A or AB amplifier, has the drawback of lower efficiency and hence reduced battery lifetime. In this work, a fully integrated CMOS nonlinear class E amplifier is linearized based on a polar modulation scheme. The amplifier is optimized for transmitting EDGE signals at 1.75GHz. The output matching network, RF inductors, and the polar modulator are all integrated on a single 0.18 μ m CMOS die.

In CMOS, the class E power amplifier has proven its capability as a highly efficient PA [1]. Because of the low supply voltage in deep sub-micron technologies, the amplifier requires a matching network to transform the 50 Ohm antenna impedance to a lower value. Besides this matching network, a tuning network is also required to meet the Class E conditions. In most realizations, either bondwires or off-chip striplines are used for output matching and voltage shaping [1,2]. Although the quality factor, and hence the efficiency of these techniques is higher compared to on-chip spiral inductors, a more complex and expensive packaging process is required. In this work, on-chip spiral inductors are used for both matching and voltage shaping. Consequently, the performance of the power amplifier is less sensitive to packaging, enabling a small and compact amplifier.

Figure 17.3.1 shows the simplified schematic of the fully integrated three-stage RF amplifier. An on-chip inductor tunes the gate capacitance of each RF nMOS transistor. This requires less power in the driving stages and increases the overall power added efficiency (PAE). The differential structure reduces the AC current through the power-supply and ground bondwires and reduces the value of the on-chip decoupling capacitors. Due to the highly efficient class E operation of the output stage, the voltage at the drain of the corresponding transistor will be approximately 2.56 times the supply voltage. This may cause reliability problems if no precautions are taken. In this implementation, a thick gate oxide transistor with a gate length of 0.35 μ m is used in the last stage to overcome these problems. Also, the supply voltage of each RF stage is regulated on-chip to avoid excessive voltage peaks at the transistor terminals. The fully integrated amplifier requires an input power of only -3dBm, relaxing the specifications of the preceding mixer stage. The measured output power is 27dBm at 1.75GHz. The measured PAE of the integrated amplifier is 34%, taking into account the power dissipation of the driving stages.

To linearize the switching amplifier, the supply voltage of the last stage is varied by means of an amplitude modulator, integrated on the same chip as the RF amplifier (Fig 17.3.1). Since the envelope of the output RF carrier is directly related to the supply voltage of the last stage, the AM-AM distortion is reduced and therefore, the AM-PM distortion is the main cause of distortion in this polar linearization scheme [3]. The cause of the AM-PM distortion is twofold. The first reason is the nonlinear behavior of the drain-bulk junction capacitance C_j (Fig. 17.3.1). As the supply voltage is reduced, the junction capacitance will increase and the

waveform at the drain of the output transistor will slightly deviate from the ideal class E operation. Since the deviation is small, the efficiency will remain high but the phase of the output RF signal will change. Second, the feedthrough from the driver stage to the output stage is more pronounced when the last stage operates at a lower supply voltage. Figure 17.3.2 shows the measured AM-PM distortion of the amplifier. In this measurement, an unmodulated carrier is applied to the RF amplifier and the envelope signal is slowly varied. As can be seen, the AM-PM distortion becomes severe as the supply voltage goes to zero. The distortion has been measured for different samples and temperatures ranging from 20°C to 70°C. All this data is plotted on Fig. 17.3.2, but only little variation can be noticed. With the amplitude modulator, the output power can be dynamically adjusted. Figure 17.3.3 shows the measured efficiency of the amplifier and the transmitter for different power levels. The amplifier itself (η_{PA}) maintains its high efficiency of 40% over the entire power range. When the power consumption of the RF driver stages is taken into account (η_{PA+DRV}), the efficiency drops to 34%. Due to the voltage drop across the amplitude modulator ($\eta_{PA+DRV+AM-MOD}$), the efficiency becomes 30%.

The transmitter is designed for the EDGE standard operating at 1.75GHz, which is a follow-up of the DCS1800 standard. The 1MHz bandwidth of the amplitude modulator is sufficiently large to avoid distortion of the EDGE envelope signal. The phase signal is upconverted by an external quadrature mixer and the envelope signal is directly applied to the integrated amplitude modulator. No delay adjustment between amplitude and phase is necessary; this is due to the wide bandwidth of the amplitude modulator and the small delay in the upconverter. In EDGE mode, the amplifier achieves a measured average output power of 23.8dBm with an average PAE of 22%. Figure 17.3.4 shows the output spectrum of the RF EDGE signal at 1.75GHz, which is in agreement with the spectral mask. At 400kHz and 600kHz frequency offset, the ACPR is -56.7dBc and -64dBc, respectively. Power control is implemented by reducing the envelope signal at the input of the amplitude modulator. The EVM-rms requirements are met over a wide range of different power control levels, as can be seen in Fig. 17.3.5. Reducing the RF envelope will increase the AM-PM distortion (Fig. 17.3.2), which in turn increases the distortion at lower output power. The measured AM-PM distortion of Fig. 17.3.2 is used to implement a digital predistorter, that approximates the average AM-PM curve by eight straight lines. Applying this piece-wise linear predistortion will reduce the EVM-rms at lower power levels.

The performance of the PA is summarized in Fig. 17.3.6. Figure 17.3.7 shows a micrograph of the fully integrated amplifier. The total chip area measures 1.8x3.6mm².

References:

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- [2] T. Sowlati and D. Leenaerts, "A 2.4GHz 0.18 μ m CMOS Self-Biased Cascode Power Amplifier with 23dBm Output Power," *ISSCC Dig. Tech. Papers*, pp. 294-295, Feb., 2002.
- [3] D. Su and W. McFarland, "An IC for Linearizing RF Power Amplifiers using Envelope Elimination and Restoration," *ISSCC Dig. Tech. Papers*, pp. 54-55, Feb., 1998.

Figure 17.3.1: Simplified schematic of the linearized RF amplifier.

Figure 17.3.2: Measured AM-PM distortion of the linearized RF amplifier.

Figure 17.3.3: Measured efficiency of the linearized RF amplifier.

Figure 17.3.4: Measured EDGE output spectrum at 23.8dBm average output power.

Figure 17.3.5: Measured EVM-rms for different power levels.

technology	0.18μm CMOS	
frequency	1.75GHz	
area	1.8 x 3.6mm ²	
constant envelope performance	measured	
input power	-3dBm	
output power	27dBm	
PAE	34 %	
linearized performance	measured	Class E3 EDGE specifications
average linear output power	23.8dBm	22dBm
average PAE	22 %	
EVM-rms	1.67 %	< 9 %
ACPR @ 400 kHz	-56.7dBc	< -54dBc
ACPR @ 600 kHz	-64dBc	< -60dBc

Figure 17.3.6: Performance summary.

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Figure 17.3.7: Micrograph of the linearized CMOS RF power amplifier.