A 10-bit 250-MS/s Binary-Weighted Current-Steering DAC

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Abstract—This paper studies the impact of segmentation on current-steering digital-to-analog converters (DACs). Segmentation may be used to improve the dynamic behavior of the converter but comes at a cost. A method for reducing the segmentation degree is given. The presented chip, a 10-bit binary-weighted current-steering DAC, has >60 dB SFDR at 250 MS/s from DC to Nyquist. At 62.5 MHz signal frequency and 250 MS/s, we operated the device in 9-bit unary, 1-bit binary-weighted mode. The obtained 60 dB SFDR in this measurement demonstrates that the binary nature of the converter did not limit the SFDR. The chip draws 4 mW from a dual 1.5 V/1.8 V supply plus load currents. The active area is less than 0.35 mm^2 in a standard 1P-5M $0.18\text{-}\mu\text{m}$ 1.8-V CMOS process. Both INL and DNL are below 0.1 LSB.

Index Terms—Binary weighted, digital-to-analog converters, low power.

I. INTRODUCTION

CURRENT-STEERING digital-to-analog converters (DACs) are well suited to generate broadband signals for single-hop transmitters. They are fast and able to offer high spurious-free dynamic range (SFDR) up till high frequencies. This high level of performance can be achieved since no internal nodes with large capacitances must be charged or discharged. It has been shown that segmentation, that is, weighting the MSB current-sources unary and the LSB current-sources binary, is important for dynamic performance. In [1] and [2], for example, two similar structures are used for the DAC. The main difference between both is that the converter in [1] uses 5-bit unary plus 5-bit binary-weighted segmentation, while [2] uses full binary-weighted decoding. The segmented converter achieves 10-bit dynamic accuracy up to the Nyquist frequency for a sample rate of 1 GS/s. The binary-weighted converter, however, achieves 10-bit dynamic accuracy up to the Nyquist frequency for only a sample rate of 30 MS/s. However, high degrees of segmentation do come at a price. Segmentation adds to the power consumption, complexity and size of the converter. Too much segmentation can worsen the performance rather than improve it; the big dynamic core deteriorates timing and increases the digital noise. The correct timing of a converter with a big dynamic core can become challenging as the distances between the various segments is increased and the large portion of logic adds more load to the clock line. Therefore, making the assumption that increasing segmentation is the best

way to boost dynamic performance [3] may ignore better ways of dealing with dynamic nonlinearities.

Reducing the segmentation degree may thus be advantageous for the overall performance of the converter. Although some papers discuss the importance of segmentation [3], it is still poorly understood. Rather than assuming that extra segmentation improves the performance, we tried to separate the effects caused by segmentation from the effects caused by other mechanisms. Soon we realized that very few mechanisms for generating spurious signals are strongly related to the segmentation. Addressing these mechanisms could thus yield a binary-weighted DAC with high SFDR at high signal and clock frequencies. So, we designed a binary-weighted converter rather than a segmented one. We see that the binary-weighted converter is still less tolerant to poor design than the segmented one, so we chose, for simplicity, to use generous margins on all parameters.

II. STATIC PERFORMANCE

An N -bit binary-weighted converter has only N current sources with sizes ranging from one times the LSB current to 2^N times the LSB current. This can lead to large linearity errors at the major code transitions. It is important to limit the linearity errors at these major code transitions, otherwise they can reduce the obtained SFDR. Therefore, we take a closer look at this. Our design specifications are as follows:

- $\text{INL} < 0.5 \text{ LSB}$
- $\text{DNL} < 1 \text{ LSB}$.

A DNL smaller than 1 LSB ensures that the converter is monotonic: every increase of the digital input code leads to an increase of the analog output value. The DNL is always smaller than 1 LSB if the INL is smaller than 0.5 LSB. An INL smaller than 0.5 LSB guarantees that the maximum linearity error is smaller than the maximum quantization error. We thus design for an INL smaller than 0.5 LSB, a common specification for DACs. Via Monte Carlo simulations, we obtain the plot of Fig. 1, which shows the yield in function of the standard deviation for both unary and binary decoding. We aim for a 3σ yield, meaning that 99.7% of the converters must have an INL smaller than 0.5 LSB. For a 3σ yield, the required area is comparable in both cases. Simulations show that the expected DNL is higher for a binary-weighted converter than for a segmented one. However, our simulations and calculations indicate that this does not pose a problem for reaching 10-bit accuracy as long as we meet the mentioned INL and DNL specifications.

Fig. 1 is only correct if all basic current sources have the same physical dimensions. In many segmented converters this is not

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Fig. 1. Yield as a function of the standard deviation σ on the current sources for both unary and binary-weighted converters.

the case. The use of different basic types of current-source transistors, e.g., transistors with widths equal to $1\ \mu\text{m}$ and transistors with widths equal to $16\ \mu\text{m}$, often leads to systematic errors and hence reduces static performance. We will take a look at the different options for the current-source array.

A. Unary-Weighted Current Sources

An N -bit converter can generate $2^N - 1$ different output codes. In a pure unary implementation of the current-source array, $2^N - 1$ equal current sources are used. Only identical current sources are used, as one transistor with double the width will behave slightly differently than two transistors in parallel. The segmentation level of the current-source array can be shielded from the segmentation level of the decoder by putting the correct number of unary-weighted current sources in parallel, as is explained below.

B. Split Structures for MSB and LSB Current Sources

The current-source array of a 10-bit converter needs 1023 basic current sources in a pure unary implementation. This amount of current sources requires more area and interconnects than an implementation with fewer individual current sources. Therefore, many designers use two different structures for the MSB and LSB parts. This adds an additional matching requirement between the biasing currents. Also, care must be taken to cancel out the differences in systematic errors between the two structures, to avoid further matching errors.

C. Division of the Current of One MSB Current Source in LSB Currents

In this case, the current-source array consists of MSB units only. The current of one unit is further split into smaller currents. This guarantees that the total current of all LSB sources matches well to the rest of the structure, as in [4]. The transistors that split this MSB current have relatively relaxed matching specifications. They require extra voltage to maintain adequate headroom, so this technique is less suited for low-voltage design.

15	12	10	11	13	14	7	9	2	5	1	6	0	3	8	4
5	0	4	8	3	2	6	1	12	13	9	14	7	15	11	10
1	6	2	3	8	4	0	5	10	11	15	7	14	9	13	12
9	7	14	13	11	10	12	15	4	8	3	0	6	1	5	2
13	14	7	9	15	12	10	11	0	3	8	4	2	5	1	6
3	2	6	1	5	0	4	8	7	15	11	10	12	13	9	14
8	4	0	5	1	6	2	3	14	9	13	12	10	11	15	7
11	10	12	15	9	7	14	13	6	1	5	2	4	8	3	0
2	5	1	6	0	3	8	4	15	12	10	11	13	14	7	9
12	13	9	14	7	15	11	10	5	0	4	8	3	2	6	1
10	11	15	7	14	9	13	12	1	6	2	3	8	4	0	5
4	8	3	0	6	1	5	2	9	7	14	13	11	10	12	15
0	3	8	4	2	5	1	6	13	14	7	9	15	12	10	11
7	15	11	10	12	13	9	14	3	2	6	1	5	0	4	8
14	9	13	12	10	11	15	7	8	4	0	5	1	6	2	3
6	1	5	2	4	8	3	0	11	10	12	15	9	7	14	13

Fig. 2. One quarter of the switching scheme used. Current sources with numbers 1 to 15 are used for the pseudo-segments. Current sources with number 0 are used for the LSB part. The scheme is tolerant to gradient errors and reduces the impact of the edges of the current-source array.

D. Implementation of the Current-Source Array

We opted for unary-weighted basic current sources. These basic current sources are connected in parallel to weight them binary. There is no distinction between MSB and LSB basic sources, eliminating this systematic error. The large number of basic sources is used to reduce the gradient errors [5]. It is also used to reduce the influence of the errors on the current sources close to the edge of the array [6]. Dummies around the current-source array further reduce the linearity degradation caused by the edges.

One quarter of the switching sequence is shown in Fig. 2. Our converter is binary-weighted, but we design it as if it were a 4-bit unary, 6-bit binary segmented converter. Then we replace the 4-bit thermometer decoder by a binary-weighted decoder. We call this approach “pseudo-segmentation.” The pseudo-segmentation is reflected in the switching scheme. The current sources with numbers 1 to 15 form the 15 pseudo-unary current sources. The current sources with number 0 are used to form the LSB current sources. This pseudo-segmentation is mainly used for the dynamic behavior and will be discussed later.

The measurements of our binary-weighted DAC show that the current-source array has good static linearity. We have an INL and DNL both smaller than 0.1 LSB. As we stated in the beginning of this section, an INL smaller than 0.5 LSB is sufficient for the dynamic performance.

III. DYNAMIC PERFORMANCE

In the previous section, we have shown that the static behavior is not responsible for the low dynamic performance of most binary-weighted DACs; the difference in performance between segmented and binary-weighted converters must be found somewhere else. We track it by comparing the difference in structure between a unary-weighted and a binary-weighted converter.

A. Pseudo-Segmentation

Segmented current-steering DACs perform well at high frequencies, but the published binary-weighted converters in the literature do not. Ideally, the only difference between both structures is located in the digital part: the bits are decoded in another

Fig. 3. Scheme for a segmented converter. The converter has a decoding stage, a switching core with the switches, cascodes and latches, and a current-source array.

Fig. 4. The thermometer decoder seen in Fig. 3 is replaced by a binary-weighted one, shown here, in order to obtain a fully binary-weighted converter.

way. We believe, therefore, that the best way to design a binary-weighted converter is to design a segmented one, replacing the 4-bit thermometer decoder by a binary-weighted decoder. In this way, we modify the converter just enough to make it binary-weighted. We call this approach “pseudo-segmentation”. It is indeed very tempting to scale some parts of the design if they seem to be oversized. This scaling, however, may for example generate different delays for the different bits. We also narrow the design space. Fig. 3 shows the outcome of the first step, the design of a general segmented converter. Then, we replace the thermometer decoder by the decoder shown in Fig. 4. The “switching core” holds all the switches, latches, cascodes and cascodes above the switches.

B. Glitch Energy

The glitch energy is the energy difference between the ideal transition and the real transition, as Fig. 5 shows. The major code transitions have the biggest glitch energies. Fig. 5 shows that most of the energy is due to the slower-than-ideal transition. This is not an issue to most designers, as this happens for all transitions and does not affect linearity. Therefore, most glitch measurements show the major $011111111 \rightarrow 100000000$ transition.

However, for time-domain applications such as video DACs, such waveform distortion from transitions is undesired. This

Fig. 5. The glitch energy equals to the energy difference between the ideal transition and the real transition. Most of the energy is due to the slower than ideal transition.

distortion shows up in the video image. For frequency-domain applications, the effect of transitions on the SFDR and SNDR in the frequency-band of interest is more important. In this work, we focus on DACs with high SFDR.

C. Glitch Energy and Unary Decoding

In a unary-decoded DAC, exactly $\text{code}(i) - \text{code}(i-1)$ switches are switched on or off for a code transition from $\text{code}(i-1)$ to $\text{code}(i)$. Ignoring the quantization, the code change is the derivative of the signal to the time.

The signal can be represented by its frequency components. Each frequency component is a sine wave with a certain amplitude and phase. The derivative of each sinusoidal component is a sinusoid with the same frequency. If all transitions are equal and proportional to the code change, then the code transitions generate spurs at the signal frequencies themselves, creating no distortion components [3].

However, the condition that all transitions are equal is often not fulfilled; the up-transitions may differ from the down-transitions. The transitions are also dependent on the output voltage. Both effects lead to signal dependencies of the glitch and thus cause dynamic nonlinearities even for unary-decoded converters.

D. Glitch Energy and Binary Decoding

In a binary-decoded DAC, at least $\text{code}(i) - \text{code}(i-1)$ switches are switched on or off for a code transition from $\text{code}(i-1)$ to $\text{code}(i)$. Another y switches are switched simultaneously on and off. During switching we have thus a superposition of (a) the transient effect of the unary-decoded converter, and (b) the transient effect of the y switches that are switched simultaneously on and off. Therefore, the dynamic nonlinearities are a superposition of the dynamic nonlinearities of a unary-decoded converter and the additional dynamic nonlinearities of the binary-decoded converter. This is in line with

Fig. 6. Basic buffer-latch-switch structure.

the common belief that binary-weighted converters produce more spurs than segmented ones.

Fig. 6 shows the basic buffer-latch-switch structure. If the sum of the currents through the switches M7–M8 remains constant at all times, then the additional dynamic nonlinearities from the binary switching are not seen. For example, in the transition from code 511 to code 512, there are 511 switches switched off and 512 switches switched on. If the sum of the currents through the switches M7–M8 remains constant at all times, then the 511 currents that are switched off are perfectly compensated by another 511 currents that are switched on. These 511 simultaneous up and down transitions are then not seen. Only the one additional switch that is switched on is seen at the output. The converter then behaves as a unary-decoded one. Note that this condition requires that all transitions are equal and signal independent. In other words, if we can make a binary-weighted DAC that performs as well as a segmented converter, then we can control the additional nonlinearities. This can only be achieved by reducing the signal dependencies during switching, making the binary-weighted DAC the ideal test case to verify if the switching is well controlled or not.

IV. MODELING THE BINARY-WEIGHTED CONVERTER

In the previous section, we qualitatively discussed the glitch energy and its relation to segmentation. Here, we model it to get quantitative results. We only model two effects: the effect of the different up and down transitions, and the influence of the output voltage on the switching time. In [7], the impact of time skew and jitter on binary and unary-weighted structures is modeled. The models show that the binary-weighted architectures have slightly smaller SFDR due to timing differences than the unary architectures. We agree with this, but add that the time

Fig. 7. Exponential up and down transitions with different time constants.

differences often are smaller in the binary-weighted converters as these devices are simpler and smaller structures.

A. Different Up and Down Transitions

We define both transitions to be exponential functions with different time constants. They are plotted in Fig. 7. Example time waveforms for a unary and a binary-decoded 16-bit converter are shown in Fig. 8. The input code is a step function with a step size of 2048 LSB.

Fig. 9 shows the simulated SFDR as a function of the relative frequency for both unary and binary-weighted converters, single-ended. At $f_{\text{sig}}/f_{\text{sample}} = 0.25$ the in-band distortion caused by these effects is located at the same frequency as the signal, explaining the irregularity in the plot. We see that the different up and down transitions have more impact at low frequencies in the binary-weighted converter. At high frequencies, the

Fig. 8. Example waveforms for unary and binary-decoded 16 bit converters. Between times 4000 and 5000, a major glitch is seen in the binary-decoded signal due to the transition of the MSB.

Fig. 9. Simulation of the SFDR as a function of frequency with different up and down transitions, single-ended. (upper plot) Unary-weighted converter. (lower plot) Binary-weighted converter.

unary-decoded converter is more susceptible to this effect. The effect of the different up and down transitions has even-order distortions only. Therefore, it is not necessary to simulate the differential case.

B. Influence of the Output Voltage on the SFDR

A high output voltage is preferred as it increases the signal power. The output voltage, however, is likely to influence the transitions from one code to another. Transistors M7–M10 in Fig. 6 are operated in the saturation region. They act as cascodes between nodes N7, N8, and N9. Due to the finite gain of the transistors some part of the output voltage is seen on node N5–N6 and N9. This influences the timing of the switching. In our model, we define the transition waveforms to be exponential functions that have time constants that are dependent on the output voltage. If the input code is increasing, then the rise time

Fig. 10. Simulation of the influence of the output voltage on the SFDR, single-ended. (upper plot) Unary-weighted converter. (lower plot) Binary-weighted converter.

Fig. 11. Simulation of the influence of the output voltage on the SFDR, differential-ended. (upper plot) Unary-weighted converter. (lower plot) Binary-weighted converter.

is modeled to be dependent on the mean value of the output before and after switching. We make this assumption because we believe the rise time is dependent on both the output voltage at the beginning of the transition and on the output voltage at the end of the transition. If the code is decreasing, we make the fall time dependent on the output voltage of the complementary output in order to keep the fully differential nature of the structure.

Fig. 10 shows the influence of the output voltage on the SFDR for the single-ended case. The spurious signals caused by the output voltage are even and odd order. The results for the differential case are shown in Fig. 11. Here again, we see that the unary-decoded converter outperforms the binary-decoded at low

frequencies, but has poorer worst-case performance over the entire Nyquist range.

C. Influence of the Transition Time

In the previous subsection, we modeled the transition time to be dependent on the output voltage. In this subsection, we make the assumption that slow transitions align with larger time differences due to the output voltage. In other words, we assume that the influence on the transition time is relative to the total transition time.

We resimulated the influence of the output voltage with twice as large time constants and equal relative impact on these time constants. On average, the SFDR is over 8 dB worse. It is thus important to have transitions that are as fast as possible.

V. IMPLEMENTATION

Our analysis (and the analysis in [7]) both indicate that there is no clear reason why a unary (or segmented) converter outperforms a binary-weighted converter by an order of magnitude in published designs. We also showed that transition times must be as fast as possible. We therefore opt to make a pseudo-segmented converter with as fast as possible transition times. A pseudo-segmented converter is identical to a segmented one, except that the bits at the input of the segments are decoded binary instead of unary.

A. Differences Between Segmented and Pseudo-Segmented Structures

The converter can be split into two parts. The decoder transforms the binary input code into a number of bits used by the analog part. The analog part takes these digital signals as inputs and generates the appropriate output current. The only difference between a segmented and a pseudo-segmented converter is how the digital part decodes the input code. This difference has been modeled in the previous section and does not seem to reduce the SFDR over the Nyquist range. However, the interface between the digital and the analog structure is often carried out differently.

For example, the same driver is used for the MSB as for the smaller bits. More subtle differences do exist. The digital part of the segmented converter often has a large driving capability whereas the binary-weighted converter often has a minimum-size digital connection to the analog part.

B. Basic Structure

The basic schematic for a pseudo-segment is depicted in Fig. 6. The input buffer, latch, the David–Goliath inverters, and parasitic capacitances are depicted in Fig. 12. Note that we transform the differential schematic from Fig. 6 to an equivalent single-ended schematic in Fig. 12. Inverters I1 and I2 are the differential David inverters, and transistors M2 to M5 form the differential Goliath inverters. Nodes N10 and N11 in Fig. 12 match with nodes N1 and N2 for the left side of the differential structure seen in Fig. 6, and with nodes N4 and N3 for the right side of the schematic. Inverter I3 is composed by transistors M11 and M12 for the left part of the differential circuit and by transistors M13 and M14 for the right part. Inverter I3 acts as

Fig. 12. Simplified schematics of the basic buffer-latch structure.

Fig. 13. Example simulated waveform when the clock turns high.

an inverting buffer, buffering the digital input. Capacitance C2 holds the current state of the segment. Capacitance C1 holds the next state. The David–Goliath structure is used to regenerate the node while the clock is low.

If the clock is switched to high, then nodes N10 and N11 are shorted. If both states differ, then the two nodes with different voltages are shorted. A capacitive division between C1 and C2 occurs. This can temporarily flip the digital value stored on node N10. This transition can take a long time depending on the driving strength of inverter I3, the parallel capacitance of C1 and C2 and the strength of the David inverter. Example waveforms are shown in Fig. 13 when the clock turns high. Note that this simulation still assumes a reasonably big capacitance C1 and driving inverter I3. Increasing the driving strength of inverter I3 and the capacitance on node N10 from minimum sizes to 30 times the minimum size increases the simulated SFDR in Spice by roughly 20 dB. This increase in SFDR is mainly attributed to the increased switching speed. To be more precise, we increased the dimension of the nMOS transistor from minimum size to 30 times the minimum size. We increased the dimension of the pMOS transistor from 2 times the minimum size to 60 times the minimum size. This increases the power consumption, but the total power consumption still remains small. The waveforms plotted in Fig. 13 are simulated with an inverter I3 that has four times the minimum dimensions.

C. Power Savings of the Design

It is clear that a binary-weighted converter has a very simple decoder. This far less complex decoder consumes only a small amount of power. Furthermore, we have a very regular structure. In the layout, we only use parallel instances of the switching

Fig. 14. Unoptimized layout of parallel inverter instances.

Fig. 15. Mirrored layout of parallel inverter instances reduces the area requirements and the parasitic capacitances.

core segments. Fig. 6 shows the schematic of the switching core segments together with the current source. For the 4 MSB, the blocks are identical, that is, for the MSB 8 of those blocks are placed in parallel. For the second MSB 4 of those blocks are used in parallel. For the 6 LSB, the switching core segments are almost identical. They only differ in the sizing of the switches, the cascodes and the cascodes above the switches. As these transistors have smaller sizes, they still fit in the same area as the basic layout.

The “binary decoder” is just a number of parallel buffers. We call these buffers the decoder buffers. These buffers are simple blocks that fit easily in a very regular layout. Combining the switching core segments and the decoder buffers we have a very regular basic block and layout instance. We place these instances in a mirrored fashion on the layout. We then can share power supplies, wells and sources of the transistors connected to the power supplies. Sharing these layout features reduces the pitch of the instances quite a bit.

An example layout for a simple inverter is given in Fig. 14 before and in Fig. 15 after sharing the layout features. The result of using very regular, layout-optimized and mirrored basic instances is that we have a very regular and compact decoder and switching core with a high fill factor. We use only very short connections between all devices. This results in minimal parasitic capacitances. Due to these small connections, it is easy to control the delay differences. This reduces the need to oversize the devices driving these lines. Furthermore, the clock line is small and has a small load. This decreases the power consumption of the clock, maintaining the desired sharp clock edges.

The removal of the thermometer decoder requires precaution. Our simulations showed that two things are critical to make high-performance binary-weighted DACs: all segments must be as close to equal as possible, and the switching must be as fast as possible. As explained in Section V-B, the switching speed is strongly increased if we increase the size of the buffer. We thus traded the accuracy of the latch for speed. Compared to the latch presented in [1], our latch is simpler, faster, and consumes less power. Because we traded accuracy for speed, we do not need any correction on the operating point [8]. We therefore avoid the associated power consumption. Because we used a good switching sequence for reducing the systematic errors [6], we did not need background calibration [9] or dynamic av-

Fig. 16. Measured INL and DNL.

Fig. 17. Measured spectrum for a 122.5-MHz signal at 250 MS/s.

eraging [10] of the current sources, again reducing power consumption. In the entire converter, we do not use power-hungry operational amplifiers nor gain-boosting [4]. All the simplicity in the design thus allowed us to have low power consumption while the optimization of the latches allowed us to have good dynamic performance.

Fig. 18. SFDR plot for measured frequencies. The sample rate is 250 MS/s.

Fig. 19. Two-tone measurement. Tones are at 100 and 102.5 MHz. The SFDR in the shown band is 66.76 dB.

VI. MEASUREMENT RESULTS

All measurements are done at 250 MS/s with 10-mA load current unless explicitly stated otherwise. Fig. 16 shows the measured INL and DNL, which are both within 0.1 LSB. Fig. 17 shows the spectrum for a 122.5-MHz single-tone signal. The SFDR is 62.3 dB in the Nyquist band. The measurements are differential, but still we have large parts of second-order distortion in the measurement results. Fig. 18 summarizes the spectral performance for the full-scale single-tone signals. The SFDR is over 60 dB for all measured frequencies. We also measured the DAC with a load current of 5 mA, because many published results stress that it is important to have a good crossing point [8]. By using only half of the current that the converter is designed for, we operate it far from the optimal crossing point. This leads to a less than 3-dB SFDR drop over the Nyquist band. This demonstrates that our buffer-latch combination is insensitive to the exact crossing point. We have thus successfully traded precision for speed in the latch, easing deep-submicron integration.

 Fig. 20. Measured spectrum for a $0.01 \times$ full-scale signal around the midcode.

 Fig. 21. Measured SFDR for $0.01 \times$ full-scale signals +40 dB. The SFDR for full-scale signals is plotted for comparison.

Two-tone tests and small-signal tests around the middle code are important for a binary-weighted converter. Fig. 19 shows a two-tone test with sine waves at 100 and 102.5 MHz. The SFDR in a 17.5-MHz wide band is 67.8 dB. Fig. 20 shows the spectrum for a small signal that has only codes ranging from 506 to 517 around the middle code. So, we positioned the signal around the major $0111111111 \rightarrow 1000000000$ transition, the worst possible location. Fig. 21 shows the measured SFDR for the $0.01 \times$ full-scale signals plus 40 dB. The plot shows that the spurious do not get worse for smaller signals. Therefore, the dynamic range is not compromised by the binary structure.

We also measured the $0000000001 \rightarrow 1000000000 \rightarrow 1111111111 \rightarrow 1000000000 \rightarrow 0000000001 \dots$ sequence. With this dataset, the converter actually works as if it were a 9-bit unary 1-bit binary segmented converter. This one sequence allows us to have an idea about the performance that an equivalent segmented converter would have. The measured

TABLE I
SPECIFICATIONS

Technology	1.8 μm
Supply	1.8 V
INL, DNL	< 0.1 LSB
Active area	< 0.35 mm^2
Sample rate	250 MS/s
SFDR ($I_{\text{load}} = 10 \text{ mA}$)	> 60 dB
SFDR ($I_{\text{load}} = 5 \text{ mA}$)	> 57.8 dB
Glitch energy	2.64 pV.s
Power@Nyquist	4 mW + $I_{\text{load}} \times 1.8 \text{ V}$

Fig. 22. Chip photograph. The current-source array and the drivers, switches, and latches are indicated. The chip is bond-path limited. Most of the area is filled with dummies.

SFDR here is also 60 dB, indicating that the binary weighting of the converter did not limit the SFDR and that the two modeled effects in Section IV are not dominant.

Table I summarizes the specifications. The clock buffer and the buffers that we placed at the bond-paths for regenerating the signal strength of the input signals consume 2 mW out of 4 mW. Fig. 22 shows a die photograph. The chip area is bond-path limited. The active area is less than 0.35 mm^2 . Due to the highly regular binary structure, the drivers, switches, and latches require only a minimal amount of area. They are denoted as the switching core in Fig. 22.

VII. COMPARISON WITH OTHER BINARY-WEIGHTED DACS

In [11], a 14-bit binary-weighted and calibrated DAC is presented. It has 84 dB of SFDR at low signal frequencies but it drops fast as the signal frequency is increased. The converter in [2] had the highest SFDR at high frequencies for a binary-weighted converter known to the authors. Our converter has 60 dB SFDR at 5 times higher sample rate and at 8 times higher signal frequencies. The frequency behavior of each design is shown in Fig. 23 and Table II compares specifications.

Fig. 23. SFDR of published binary-weighted converters.

TABLE II
COMPARISON WITH OTHER BINARY-WEIGHTED DACS

	[11]	[2]	This work
Number of bits	14	10	10
Max sample rate	100MS/s	50MS/s	250MS/s
Best SFDR	84dB@0.1MHz 45dB@25MHz	61dB@15MHz	>60dB@122.5MHz
Technology	0.18 μm CMOS	0.35 μm CMOS	0.18 μm 1P5M CMOS
Power consumption	20mW	1mW digital @30MS/s	4mW+10mA*1.8V @250MS/s
Area	1mm ² calibrated	0.23mm ² core area	0.35mm ² core area

VIII. CONCLUSION

In the presented work we studied the differences between unary-weighted and binary-weighted converters. The work presented in [2] and in [7] and our modeling here indicated that it had to be possible to build binary-weighted DACs with high dynamic performance. We discovered that the boundary between the decoder and the latch is critical as the signals there are both analog and digital. This problem can be alleviated by increasing the capacitance on this node and by making all buffer-latch structures identical. Using this approach, we managed to design and measure a 250-MS/s 10-bit binary-weighted current-steering DAC with over 60 dB SFDR over the entire Nyquist bandwidth. Specific codes exist where the spectral behavior is identical to the one of a highly segmented converter. At these codes, the performance did not increase. The binary nature of the converter thus did not pose limits to the SFDR. The performance drop while operating the device far outside the nominal operating point was limited, showing that the accuracy in the latch can be traded with speed. These new insights allow for

fast and compact current-steering converters that scale well in deep-submicron technologies.

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